ANALOG DEVICES

System Monitor and Fan Controller For Low-Noise PCs*

Preliminary Technical Data

ADM1027

FEATURES

Monitors Up to 5 Supply Voltages
Monitors up to 4 Fan Speeds
Monitors 2 Remote And 1 On-Chip Temperature Sensor
Monitors Processor VID Bits
Automatic Fan Speed Control
Enhanced Acoustic Mode
Monitors CPU $\overline{\text{PROCHOT}}$ output
2-wire and 3-wire Fan Speed Measurement
Limit Comparison of all Monitored Values
PWM Fan Speed Control Outputs
Serial System Management Bus (SMBus) Version 1.1 Compliant
Meets SMBus 2.0 Electrical Specifications

APPLICATIONS

Low Acoustic Noise Desktop PCs

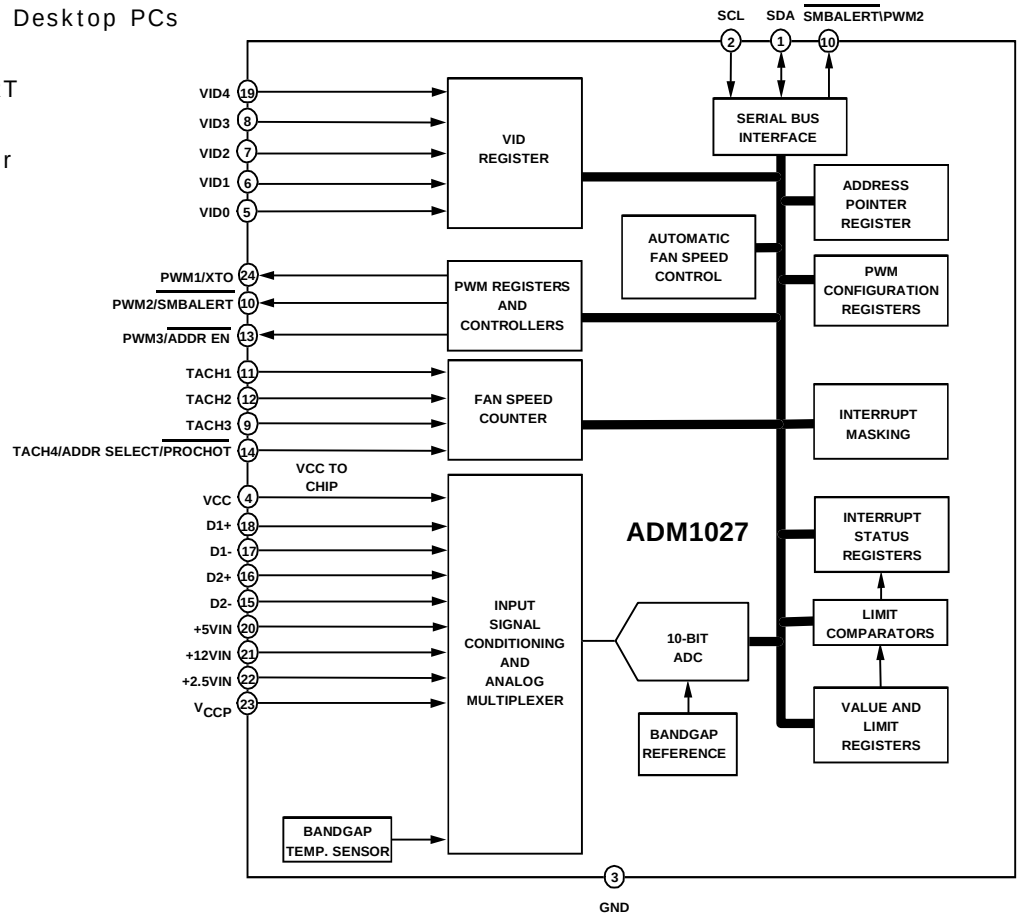
SOFTWARE SUPPORT

LDCM
Intel® Active Monitor

GENERAL DESCRIPTION

The ADM1027 is a complete systems monitor and multiple fan controller for desktop PCs. It can monitor +12V, +5V, CPU supply voltage and chipset supply voltage, plus its own supply voltage. It can monitor the temperature of up to 2 remote sensor diodes, plus its own internal temperature. It can measure the speed of up to 4 fans and control the speed of up to 4 fans so that they operate at the lowest possible speed for minimum acoustic noise. The Automatic Fan Speed Control Loop optimizes fan speed for a given temperature. Measured values can be read out via a serial System Management Bus, and values for limit comparisons can be programmed in over the same serial bus. The high-speed successive-approximation ADC allows frequent sampling of all analog channels to ensure a fast interrupt response to any out-of-limit measurement.

FUNCTIONAL BLOCK DIAGRAM



*Patent #US6188189

*Patents Pending

REV. PrJ 5/01

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ADM1027–SPECIFICATIONS

($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
POWER SUPPLY					
Supply Voltage	3.0	5.0	5.5	V	
Supply Current, I_{CC}		1.4	2.5	mA	Interface Inactive, ADC Active
		32	100	µA	Standby Mode
TEMP.-TO-DIGITAL CONVERTER					
Local Sensor Accuracy		±1	±3	°C	
Resolution		0.25		°C	
Remote Diode Sensor Accuracy		±2	±3	°C	$+60°C \le T_D \le +100°C$
Resolution		0.25		°C	
Remote Sensor Source Current		180		µA	High Level
		11		µA	Low Level
ANALOG-TO-DIGITAL CONVERTER (INCLUDING MUX AND ATTENUATORS)					
Total Unadjusted Error, TUE		±1	±2	%	Note 3
Differential Non-Linearity, DNL			±1	LSB	
Power Supply Sensitivity		±1		%/V	
Conversion Time (Voltage Input)		11.38	11.72	ms	See Note 4
Conversion Time (Local Temperature)		22.76	23.44	ms	See Note 4
Conversion Time (Remote Temperature)		68.27	70.31	ms	See Note 4
Total Monitoring Cycle Time		216.2	222.68	ms	
Input Resistance	100	140	200	kΩ	
FAN RPM-TO-DIGITAL CONVERTER					
Accuracy			±3	%	
Full-Scale Count			65,535		
Nominal Input RPM		109		RPM	Fan Count = 0xBFFF
		329		RPM	Fan Count = 0x3FFF
		5000		RPM	Fan Count = 0x0438
		10000		RPM	Fan Count = 0x021C
Internal Clock Frequency	87.3	90	92.7	kHz	
OPEN-DRAIN DIGITAL OUTPUTS, PWM1-PWM3, XTO					
Current Sink, I_{OL}			8.0	mA	
Output Low Voltage, V_{OL}			0.4	V	I_{OUT} = -8.0mA, V_{CC} = 3.3V
High Level Output Current, I_{OH}		0.1	1	µA	$V_{OUT} = V_{CC}$

Specifications (Continued)

Parameter	Min	Typ	Max	Units	Test Conditions/Comment
OPEN-DRAIN SERIAL DATA BUS OUTPUT (SDA)					
Output Low Voltage, V_{OL}			0.4	V	I_{OUT} = -4.0mA, V_{CC} = 3.3V
High Level Output Current, I_{OH}		0.1	1	µA	V_{OUT} = V_{CC}
SMBUS DIGITAL INPUTS (SCL, SDA)					
Input High Voltage, V_{IH}	2.0			V	
Input Low Voltage, V_{IL}			0.4	V	
Hysteresis		500		mV	
DIGITAL INPUT LOGIC LEVELS (VID0-4)					
Input High Voltage, V_{IH}	2.0			V	
Input Low Voltage, V_{IL}			0.4	V	
DIGITAL INPUT LOGIC LEVELS (TACH INPUTS)					
Input High Voltage, V_{IH}	2.0			V	
			5.5	V	Maximum input voltage
Input Low Voltage, V_{IL}			0.8	V	
	-0.3			V	Minimum input voltage
Hysteresis		0.5		V p-p	
DIGITAL INPUT LOGIC LEVELS ($\overline{\text{PROCHOT}}$) AGTL+					
Input High Voltage, V_{IH}		0.75*Vccp		V	
Input Low Voltage, V_{IL}			0.4	V	
DIGITAL INPUT CURRENT					
Input High Current, I_{IH}	-5			µA	V_{IN} = V_{CC}
Input Low Current, I_{IL}			5	µA	V_{IN} = 0
Input Capacitance, C_{IN}		20		pF	
SERIAL BUS TIMING					
Clock Frequency, f_{SCLK}	10		100	kHz	See Figure 1
Glitch Immunity, t_{SW}			50	ns	See Figure 1
Bus Free Time, t_{BUF}	4.7			µs	See Figure 1
Start Setup Time, $t_{SU;STA}$	4.7			µs	See Figure 1
Start Hold Time, $t_{HD;STA}$	4.0			µs	See Figure 1
SCL Low Time, t_{LOW}	4.7			µs	See Figure 1
SCL High Time, t_{HIGH}	4.0		50	µs	See Figure 1
SCL, SDA Rise Time, t_r			1000	ns	See Figure 1
SCL, SDA Fall Time, t_f			300	µs	See Figure 1
Data Setup Time, $t_{SU;DAT}$	250			ns	See Figure 1
Data Hold Time, $t_{HD;DAT}$	300			ns	See Figure 1
Detect Clock Low Timeout, $t_{TIMEOUT}$	25		35	ms	Can be optionally disabled

NOTES

1 All voltages are measured with respect to GND, unless otherwise specified

2 Typicals are at T_A=25°C and represent most likely parametric norm.

3 TUE (Total Unadjusted Error) includes Offset, Gain and Linearity errors of the ADC, multiplexer and on-chip input attenuators

4 Total analog monitoring cycle time is nominally 216.2ms, made up of 5 × 11.38ms measurements on voltage inputs, 22.76ms for local temperature channel, and 2 × 68.27ms measurements on external temperature channels.

5 Logic inputs will accept input high voltages up to 5V even when device is operating at supply voltages below 5V.

6 Timing specifications are tested at logic levels of V_{IL} = 0.8V for a falling edge and V_{IH} = 2.0V for a rising edge.

ADM1027

ABSOLUTE MAXIMUM RATINGS*

Positive Supply Voltage (V_{CC}) ..... 6.5 V
Voltage on $12V_{IN}$ Pin ..... +20V
Voltage on Any Other Input or Output Pin ..-0.3V to 6.5V
Input Current at any pin ..... ±5mA
Package Input Current ..... ±20mA
Maximum Junction Temperature ($T_J$max) ..... 150 °C
Storage Temperature Range .....–65°C to +150°C
Lead Temperature, Soldering
Vapor Phase 60 sec ..... +215°C
Infra-Red 15 sec ..... +200°C
ESD Rating ..... 2000 V

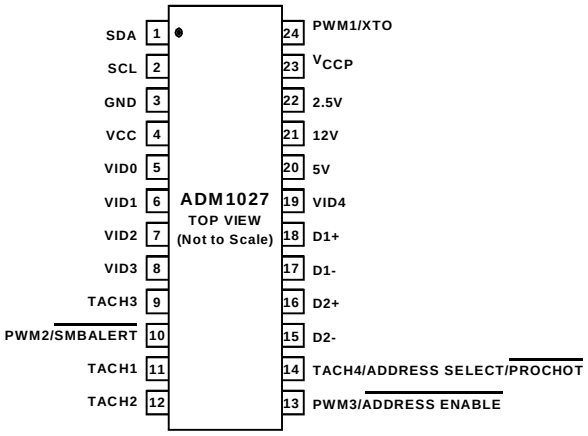
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS
24-Pin QSOP Package:
θ_{JA} = 105°C/Watt, θ_{JC} = 39°C/Watt

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADM1027ARQ	0°C to +100°C	24-Pin QSOP	RQ-24

PIN CONFIGURATION



RQ-24

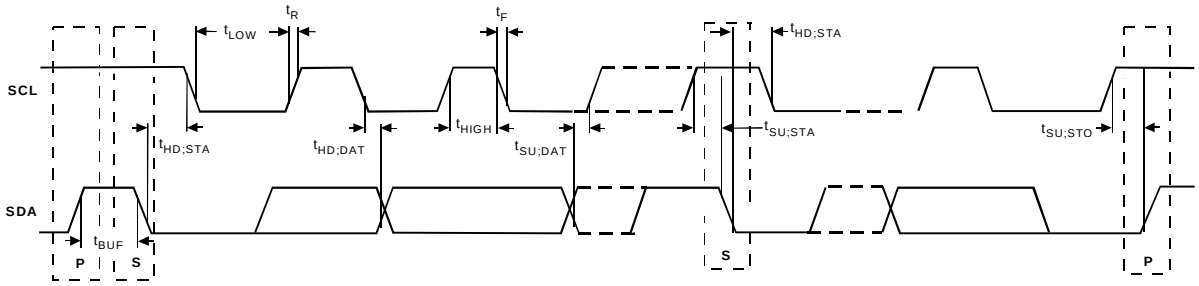


Figure 1. Diagram for Serial Bus Timing

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	SDA	Digital I/O (open drain). SMBus bidirectional serial data. Requires SMBus pullup.
2	SCL	Digital Input (open drain). SMBus serial clock input. Requires SMBus pullup.
3	GND	Ground pin for the ADM1027.
4	V_{CC}	Power Supply. Can be powered by +3.3V standby if monitoring in low power states is required. Vcc is also monitored through this pin. The ADM1027 can also be powered from a +5V supply. Setting bit 7 of Configuration Register 1 (Reg. 0x40) rescales the V_{CC} input attenuators to correctly measure a +5V supply.
5	VID0	Digital Input (open drain). Voltage Supply Readouts from CPU. This value is read in to the VID Status Register.
6	VID1	Digital Input (open drain). Voltage Supply Readouts from CPU. This value is read in to the VID Status Register.
7	VID2	Digital Input (open drain). Voltage Supply Readouts from CPU. This value is read in to the VID Status Register.
8	VID3	Digital Input (open drain). Voltage Supply Readouts from CPU. This value is read in to the VID Status Register.
9	TACH3	Digital Input (open drain). Fan tachometer input to measure speed of FAN 3.
10	PWM2/ $\overline{\text{SMBALERT}}$	Digital Output (open drain). Requires 10kΩ typical pullup. Pulse width modulated output to control FAN 2 speed. Digital Output (open drain). This pin may be reconfigured as an $\overline{\text{SMBALERT}}$ interrupt output to signal out-of-limit conditions.
11	TACH1	Digital Input (open drain). Fan tachometer input to measure speed of FAN 1.
12	TACH2	Digital Input (open drain). Fan tachometer input to measure speed of FAN 2.
13	PWM3/ $\overline{\text{Address}}$ $\overline{\text{Enable}}$	Digital I/O (open drain). Pulse width modulated output to control FAN 3/4 speed. Requires 10kΩ typical pullup. If pulled low on powerup, this places the ADM1027 in to address select mode, and the state of pin 14 will determine the ADM1027's slave address.
14	TACH4/ Address Select/ $\overline{\text{PROCHOT}}$	Digital Input (open drain). Fan tachometer input to measure speed of FAN 4. If in Address Select Mode, this pin determines the SMBus device address. Alternatively, may be reconfigured as an input to monitor and time assertion of CPU $\overline{\text{PROCHOT}}$ signal.
15	D2-	Cathode connection to 2nd thermal diode.
16	D2+	Anode connection to 2nd thermal diode.
17	D1-	Cathode connection to 1st thermal diode.
18	D1+	Anode connection to 1st thermal diode.
19	VID4	Digital Input (open drain). Voltage Supply Readouts from CPU. This value is read in to the VID Status Register.
20	+5VIN	Analog Input. Monitors +5V power supply.
21	+12VIN	Analog Input. Monitors +12V power supply.

22	+2.5VIN	Analog Input. Monitors +2.5V supply, typically a chipset voltage.
23	V_{CCP}	Analog Input. Monitors processor core voltage (0 – 3V).
24	PWM1/ XTO	Digital Output (open drain). Pulse width modulated output to control FAN 1 speed. Requires 10kΩ typical pullup. Also functions as the output from the XOR tree in XOR Test Mode.

TPC 1. Temperature Error vs. PCB Track Resistance

TPC 4. Pentium 4 Temperature Measurement vs. ADM1027 Reading

TPC 2. Temperature Error vs. Power Supply Noise Frequency

TPC 5. Temperature Error vs. Capacitance Between D+ and D-

TPC 3. Temperature Error vs. Common-Mode Noise Frequency

TPC 6. Standby Current vs. Clock Frequency

TPC 7. Temperature Error vs. Differential-Mode Noise Frequency

TPC 10. Local Sensor Temperature Error vs. Power Supply Noise Frequency

TPC 8. Standby Supply Current vs. Supply Voltage

TPC 11. ADM1027 Response to Thermal Shock

TPC 9. Supply Current vs. Supply Voltage

TPC 12. Remote Temperature Error

TPC 13. Local Temperature Error

FUNCTIONAL DESCRIPTION

GENERAL DESCRIPTION

The ADM1027 is a complete systems monitor and multiple fan controller for microprocessor-based systems. The device communicates with the system via a serial System Management Bus. The serial bus controller has an optional address line for device selection (pin 14), a serial data line for reading and writing addresses and data (pin 1), and an input line for the serial clock (pin 2). All control and programming functions of the ADM1027 are performed over the serial bus. In addition, one of the PWM outputs can be reconfigured as an $\overline{\text{SMBAlert}}$ output to indicate out-of-limit conditions.

MEASUREMENT INPUTS

The device has six measurement inputs, four for voltage and two for temperature. It can also measure its own supply voltage and can measure ambient temperature with its on-chip temperature sensor.

Pins 20 through 23 are analog inputs with on-chip attenuators, configured to monitor +5V, +12V, +2.5V and the processor core voltage (2.25V input), respectively.

Power is supplied to the chip via pin 4 and the system also monitors V_{CC} through this pin. In PCs, this pin is normally connected to a 3.3V standby supply.

Remote temperature sensing is provided by the D1+/- and D2+/- inputs, to which diode-connected, external temperature-sensing transistors such as a 2N3904 or CPU thermal diode may be connected.

The ADC also accepts input from an on-chip bandgap temperature sensor that monitors system ambient temperature.

SEQUENTIAL MEASUREMENT

When the ADM1027 monitoring sequence is started, it cycles sequentially through the measurement of analog inputs and the temperature sensors. Measured values from these inputs are stored in Value Registers. These can be read out over the serial bus, or can be compared with programmed limits stored in the Limit Registers. The results of out of limit comparisons are stored in the Status Registers, which can be read over the serial bus to flag out of limit conditions.

PROCESSOR VOLTAGE ID

Five digital inputs (VID0 to VID4 - pins 5 to 8 and 19) read the processor Voltage ID code and store it in the VID register, from which it can be read out by the management system over the serial bus.

ADM1027 ADDRESS SELECTION

Pin 13 is the dual function PWM3/$\overline{\text{Address Enable}}$ pin. If pin 13 is pulled low on power-up, the ADM1027 will read the state of pin 14 (TACH4/Address Select/$\overline{\text{PROCHOT}}$ pin) to determine the ADM1027's slave address. If pin 13 is high on power-up, then the ADM1027 will default to SMBus slave address 0x5C. This function is described in more detail later.

INTERNAL REGISTERS OF THE ADM1027

A brief description of the ADM1027's principal internal registers is given below. More detailed information on the function of each register is given in Tables 14 to 47.

Configuration Registers: Provides control and configuration of the ADM1027.

Address Pointer Register: This register contains the address that selects one of the other internal registers. When writing to the ADM1027, the first byte of data is always a register address, which is written to the Address Pointer Register.

Status Registers: These registers provide status of each limit comparison and are used to signal out-of-limit conditions on the temperature, voltage or fan speed channels. If pin 10 is configured as $\overline{\text{SMBALERT}}$, then this pin will assert low whenever a status bit gets set.

Interrupt Mask Registers: Allows each interrupt status event to be masked when pin 10 is configured as an $\overline{\text{SMBALERT}}$ output.

VID Register: The status of the VID0 to VID4 pins of the processor can read from this register.

Value and Limit Registers: The results of analog voltage inputs, temperature and fan speed measurements are stored in these registers, along with their limit values.

Offset Registers: Allows each temperature channel reading to be offset by a 2's complement value written to these registers.

PROCHOT Status Register: Allows the ADM1027 to monitor and time any $\overline{\text{PROCHOT}}$ events.

T_{MIN} Registers: Programs the starting temperature for each fan under Automatic Fan Speed Control.

T_{RANGE} Registers: Programs the temperature-to-fan speed control slope in Automatic Fan Speed Control Mode for each PWM output.

Enhance Acoustics Registers: These registers allow each PWM output controlling fans to be tweaked to enhance the system's acoustics.

SERIAL BUS INTERFACE

Control of the ADM1027 is carried out using the serial System Management bus (SMBus). The ADM1027 is connected to this bus as a slave device, under the control of a master device or master controller.

The ADM1027 has a 7-bit serial bus address. When the device is powered up with pin 13 (PWM3/$\overline{\text{Address Enable}}$) high, the ADM1027 will have a default SMBus address of 0101110 or 0x5C. If more than one ADM1027 is to be used in a system, then each ADM1027 should be placed in to Address Select Mode by strapping pin 13 low on power-up. The logic state of pin 14 then determines the device's SMBus address.

TABLE 1. ADM1027 ADDRESS SELECT MODE

Pin 13 State	Pin 14 State	Address
0	Low (10kΩ to Gnd)	0101100 (58h)
0	High (10kΩ pullup)	0101101 (5Ah)
1	Don't Care	0101110 (5Ch) (default)

The device address is sampled and latched on the 1st valid SMBus transaction, so any attempted addressing changes made thereafter will have no immediate effect.

The facility to make hardwired changes to the SMBus slave address allows the user to avoid conflicts with other devices sharing the same serial bus, for example if more than one ADM1027 is used in a system.

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, defined as a high to low transition on the serial data line SDA while the serial clock line SCL remains high. This indicates that an address/data stream will follow. All slave peripherals connected to the serial bus respond to the START condition, and shift in the next 8 bits, consisting of a 7-bit address (MSB first) plus a R/$\overline{\text{W}}$ bit, which determines the direction of the data transfer, i.e. whether data will be written to or read from the slave device.

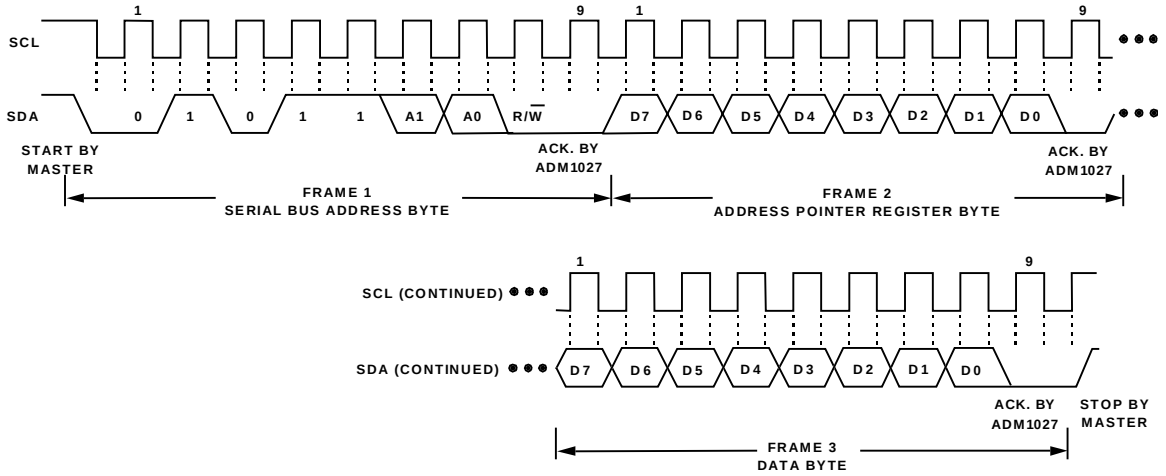


Figure 2a. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

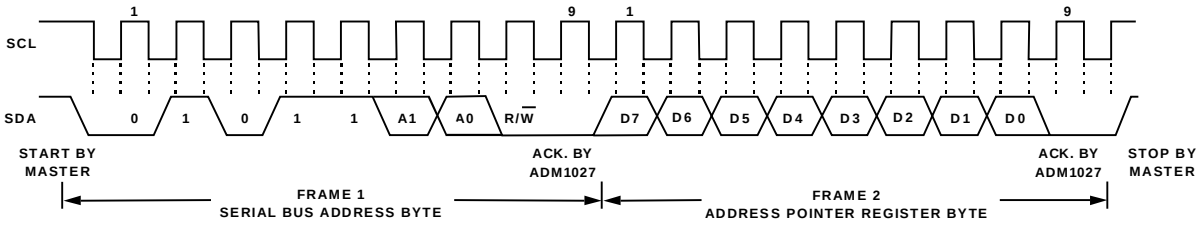


Figure 2b. Writing to the Address Pointer Register only

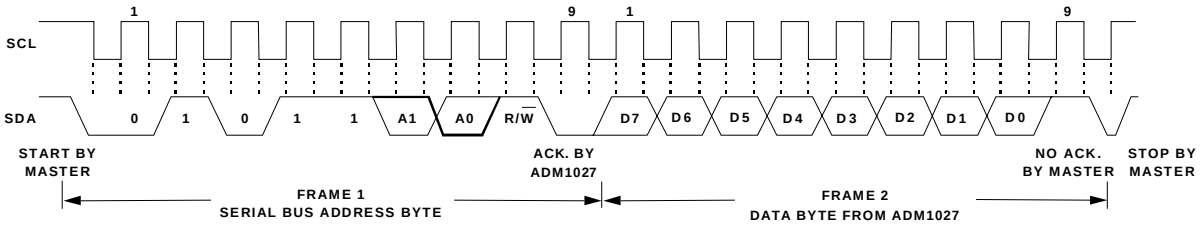


Figure 2c. Reading Data from a Previously Selected Register

The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the Acknowledge Bit. All other devices on the bus now remain idle whilst the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is a 0 then the master will write to the slave device. If the R/$\overline{W}$ bit is a 1 the master will read from the slave device.

2. Data is sent over the serial bus in sequences of 9 clock pulses, 8 bits of data followed by an Acknowledge Bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low to high transition when the clock is high may be interpreted as a STOP signal. The number of data bytes that can be transmitted over the serial bus in a single READ or WRITE operation is limited only by what the master and slave devices can handle.
3. When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master will pull the data line high during the 10th clock pulse to assert a STOP condition. In READ mode, the master device will override the acknowldge bit by pulling the data line high during the low period before the 9th clock pulse. This is known as No Acknowledge. The master will then take the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a STOP condition.

Any number of bytes of data may be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation, because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

In the case of the ADM1027, write operations contain either one or two bytes, and read operations contain one byte, and perform the following functions:

To write data to one of the device data registers or read data from it, the Address Pointer Register must be set so that the correct data register is addressed, then data can be written into that register or read from it. The first byte of a write operation always contains an address that is stored in the Address Pointer Register. If data is to be written to the device, then the write operation contains a second data byte that is written to the register selected by the address pointer register.

This is illustrated in Figure 2a. The device address is sent over the bus followed by R/$\overline{W}$ set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the Address Pointer Register. The second data byte is the data to be written to the internal data register.

When reading data from a register there are two possibilities:

1. If the ADM1027's Address Pointer Register value is unknown or not the desired value, it is first necessary to set it to the correct value before data can be read from the desired data register. This is done by performing a write to the ADM1027 as before, but only the data byte containing the register address is sent, as data is not to be written to the register. This is shown in Figure 2b.

   A read operation is then performed consisting of the serial bus address, R/$\overline{W}$ bit set to 1, followed by the data byte read from the data register. This is shown in Figure 2c.
2. If the Address Pointer Register is known to be already at the desired address, data can be read from the corresponding data register without first writing to the Address Pointer Register, so Figure 2b can be omitted.

Notes:

1. Although it is possible to read a data byte from a data register without first writing to the Address Pointer Register, if the Address Pointer Register is already at the correct value, it is not possible to write data to a register without writing to the Address Pointer Register, because the first data byte of a write is always written to the Address Pointer Register.
2. In Figures 2a to 2c, the serial bus address is shown as the default value 01011(A1)(A0), where A1 and A0 are set by the Address Select Mode function previously defined.
3. In addition to supporting the Send Byte and Receive Byte protocols, the ADM1027 also supports the Read Byte protocol (see System Management Bus specifications Rev. 2.0 for more information).
4. If it is required to perform several read or write operations in succession, the master can send a repeat start condition instead of a stop condition to begin a new operation.

ADM1027 WRITE OPERATIONS

The SMBus specification defines several protocols for different types of read and write operations. The ones used in the ADM1027 are discussed below. The following abbreviations are used in the diagrams:

S - START

P - STOP

R - READ

W - WRITE

A - ACKNOWLEDGE

$\overline{A}$ - NO ACKNOWLEDGE

The ADM1027 uses the following SMBus write protocols:

Send Byte

In this operation the master device sends a single command byte to a slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master asserts a STOP condition on SDA and the transaction ends.

In the ADM1027, the send byte protocol is used to write a register address to RAM for a subsequent single byte read from the same address. This is illustrated in Figure 3a.

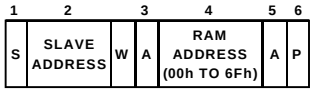


Figure 3a. Setting A Register Address For Subsequent Read

If it is required to read data from the register immediately after setting up the address, the master can assert a repeat start condition immediately after the final ACK and carry out a single byte read without asserting an intermediate stop condition.

Write Byte

In this operation the master device sends a command byte and one data byte to the slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends a data byte.
7. The slave asserts ACK on SDA.
8. The master asserts a STOP condition on SDA to end the transaction.

This is illustrated in Figure 3b.

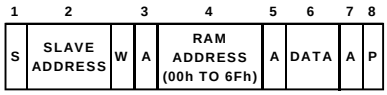


Figure 3b. Single Byte Write To A Register

ADM1027 READ OPERATIONS

The ADM1027 uses the following SMBus read protocols:

RECEIVE BYTE

This is useful when repeatedly reading a single register. The register address needs to have been set up previously. In this operation the master device receives a single byte from a slave device, as follows:

1. The master device asserts a START condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts ACK on SDA.
4. The master receives a data byte.
5. The master asserts NO ACK on SDA.
6. The master asserts a STOP condition on SDA and the transaction ends.

In the ADM1027, the receive byte protocol is used to read a single byte of data from a register whose address has previously been set by a send byte or write byte operation.

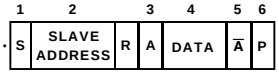


Figure 3c. Single Byte Read From A Register

ALERT RESPONSE ADDRESS

Alert Response Address (ARA) is a feature of SMBus devices that allows an interrupting device to identify itself to the host when multiple devices exist on the same bus.

The $\overline{\text{SMBALERT}}$ output can be used as an interrupt output or can be used as an $\overline{\text{SMBALERT}}$. One or more outputs can be connected to a common $\overline{\text{SMBALERT}}$ line connected to the master. If a device's $\overline{\text{SMBALERT}}$ line goes low, the following procedure occurs:-

1. $\overline{\text{SMBALERT}}$ pulled low.
2. Master initiates a read operation and sends the Alert Response Address (ARA = 0001 100). This is a general call address that must not be used as a specific device address.
3. The device whose $\overline{\text{SMBALERT}}$ output is low responds to the Alert Response Address, and the master reads its device address. The address of the device is now known and it can be interrogated in the usual way.
4. If more than one device's $\overline{\text{SMBALERT}}$ output is low, the one with the lowest device address will have priority, in accordance with normal SMBus arbitration.
5. Once the ADM1027 has responded to the Alert Response Address, the master must read the Status Registers and the $\overline{\text{SMBALERT}}$ will only be cleared if the error condition has gone away.

MEASUREMENT INPUTS

The ADM1027 has six external analog measurement inputs, which perform various functions. It also measures its own supply voltage, V_{CC}, and the internal chip temperature gives an indication of ambient system temperature.

Pins 17 and 18 are intended for CPU temperature measurement, whilst pins 15 and 16 are used as inputs for a second remote temperature sensor.

Pins 20 to 23 are dedicated to measuring +5V, +12V, +2.5V supplies and the processor core voltage V_{CCP} (0 to 3V input). The V_{CC} supply voltage measurement is carried out through the V_{CC} pin (pin 4). Setting bit 7 of Configuration Register 1 (Reg.0x40) allows a 5V supply to be used. The +2.5V input can be used to monitor a chipset supply voltage.

A-TO-D CONVERTER

All analog inputs are multiplexed into the on-chip, successive approximation, analog-to-digital converter. This has a resolution of 10 bits. The basic input range is zero to +2.25V, but the inputs have built-in attenuators to allow measurement of 2.5V, 3.3V, 5V, 12V and the processor core voltage V_{CCP}, without any external components. To allow for the tolerance of these supply voltages, the A to D converter produces an output of 3/4 full-scale (decimal 768 or 300 hex) for the nominal input voltage, and so has adequate headroom to cope with overvoltages.

TABLE 2. 10-BIT A/D OUTPUT CODE VS. V_{IN}

Input Voltage					A/D Output	
+12V_{IN}	**+5V_{IN}**	**V_{CC} (3.3V_{IN})***	**+2.5V_{IN}**	**+V_{CCPIN}**	**Decimal**	**Binary (10-bits)**
<0.0156	<0.0065	<0.0042	<0.0032	<0.00293	0	00000000 00
0.0156 - 0.0312	0.0065 - 0.0130	0.0042 - 0.0085	0.0032 - 0.0065	0.0293 - 0.0058	1	00000000 01
0.0312 - 0.0469	0.0130 - 0.0195	0.0085 - 0.0128	0.0065 - 0.0097	0.0058 - 0.0087	2	00000000 10
0.0469 - 0.0625	0.0195 - 0.0260	0.0128- 0.0171	0.0097 - 0.0130	0.0087 - 0.0117	3	00000000 11
0.0625 - 0.0781	0.0260 - 0.0325	0.0171 - 0.0214	0.0130 - 0.0162	0.0117 - 0.0146	4	00000001 00
0.0781 - 0.0937	0.0325 - 0.0390	0.0214 - 0.0257	0.0162 - 0.0195	0.0146 - 0.0175	5	00000001 01
0.0937- 0.1093	0.0390 - 0.0455	0.0257 - 0.0300	0.0195 - 0.0227	0.0175 - 0.0205	6	00000001 10
0.1093 - 0.125	0.0455 - 0.0521	0.0300 - 0.0343	0.0227 - 0.0260	0.0205 - 0.0234	7	00000001 11
0.125 - 0.1406	0.0521 - 0.0586	0.0343 - 0.0386	0.0260 - 0.0292	0.0234 - 0.0263	8	00000010 00
			● ● ●			
4.000 - 4.0156	1.6675 - 1.6740	1.100 - 1.1042	0.8325 - 0.8357	0.7500 - 0.7529	256 (1/4-scale)	01000000 00
			● ● ●			
8.000 - 8.0156	3.330 - 3.3415	2.200 - 2.2042	1.6650 - 1.6682	1.5 - 1.5029	512 (1/2-scale)	10000000 00
			● ● ●			
12.000 - 12.0156	5.0025 - 5.0090	3.300 - 3.3042	2.4975 - 2.5007	2.2500 - 2.2529	768 (3/4 scale)	11000000 00
			● ● ●			
15.8281 - 15.8437	6.5983 - 6.6048	4.3527 - 4.3570	3.2942 - 3.2974	2.9677 - 2.9707	1013	11111101 01
15.8437- 15.8593	6.6048 - 6.6113	4.3570 - 4.3613	3.2974 - 3.3007	2.9707 - 2.9736	1014	11111101 10
15.8593 - 15.8750	6.6113 - 6.6178	4.3613 - 4.3656	3.3007 - 3.3039	2.9736 - 2.9765	1015	11111101 11
15.8750 - 15.8906	6.6178 - 6.6244	4.3656 - 4.3699	3.3039 - 3.3072	2.9765 - 2.9794	1016	11111110 00
15.8906 - 15.9062	6.6244 - 6.6309	4.3699 - 4.3742	3.3072 - 3.3104	2.9794 - 2.9824	1017	11111110 01
15.9062 - 15.9218	6.6309 - 6.6374	4.3742 - 4.3785	3.3104 - 3.3137	2.9824 - 2.9853	1018	11111110 10
15.9218 - 15.9375	6.6374 - 6.439	4.3785 - 4.3828	3.3137 - 3.3169	2.9853 - 2.9882	1019	11111110 11
15.9375 - 15.9531	6.6439 - 6.6504	4.3828 - 4.3871	3.3169 - 3.3202	2.9882 - 2.9912	1020	11111111 00
15.9531 - 15.9687	6.6504 - 6.6569	4.3871 - 4.3914	3.3202 - 3.3234	2.9912 - 2.9941	1021	11111111 01
15.9687 - 15.9843	6.6569 - 6.6634	4.3914 - 4.3957	3.3234 - 3.3267	2.9941 - 2.9970	1022	11111111 10
>15.9843	>6.6634	>4.3957	>3.3267	>2.9970	1023	11111111 11

***Note: The V_{CC} output codes listed assume that V_{CC} is 3.3V. If V_{CC} input is reconfigured for 5V operation (by setting bit 7 of Configuration Register 1), then the V_{CC} output codes are the same as for the +5V_{IN} column.**

Table 2 shows the input ranges of the analog inputs and output codes of the 10-bit A to D converter.

When the ADC is running, it samples and converts a voltage input in 711µs, and averages 16 conversions to reduce noise, and so a measurement on each input takes nominally 11.38ms.

INPUT CIRCUITRY

The internal structure for the analog inputs are shown in Figure 4. Each input circuit consists of an input protection diode, an attenuator, plus a capacitor to form a first-order lowpass filter which gives the input immunity to high frequency noise.

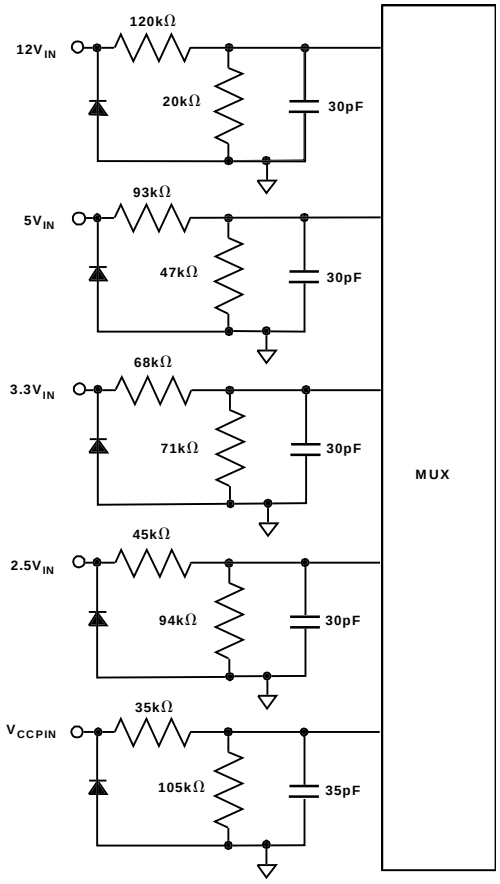


Figure 4. Structure of Analog Inputs

TEMPERATURE MEASUREMENT SYSTEM

LOCAL TEMPERATURE MEASUREMENT

The ADM1027 contains an on-chip bandgap temperature sensor, whose output is digitized by the on-chip 10-bit ADC. The 8-bit MSB temperature data is stored in the Local Temp Register (address 26h). As both positive and negative temperatures can be measured, the temperature data is stored in two's complement format, as shown in Table 3. Theoretically, the temperature sensor and ADC can measure temperatures from -128°C to +127°C with a resolution of 0.25°C. However, this exceeds the operating temperature range of the device, so local temperature measurements outside this range are not possible. Temperature measurement from -127°C to +127°C is possible using a remote sensor.

REMOTE TEMPERATURE MEASUREMENT

The ADM1027 can measure the temperature of two remote diode sensors or diode-connected transistors, connected to pins 15 and 16 or 17 and 18.

The forward voltage of a diode or diode-connected transistor, operated at a constant current, exhibits a negative temperature coefficient of about -2mV/°C.Unfortunately, the absolute value of V_{be}, varies from device to device, and individual calibration is required to null this out, so the technique is unsuitable for mass-production. The technique used in the ADM1027 is to measure the change in V_{be} when the device is operated at two different currents.

This is given by:

$\Delta V_{be} = KT/q \times \ln(N)$

where:

K is Boltzmann's constant

q is charge on the carrier

T is absolute temperature in Kelvins

N is ratio of the two currents

Figure 8 shows the input signal conditioning used to measure the output of a remote temperature sensor. This figure shows the external sensor as a substrate transistor, provided for temperature monitoring on some microprocessors, but it could equally well be a discrete transistor such as a 2N3904.

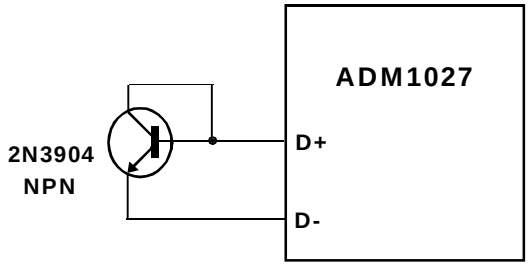


Figure 5a. Measuring Temperature Using An NPN Transistor

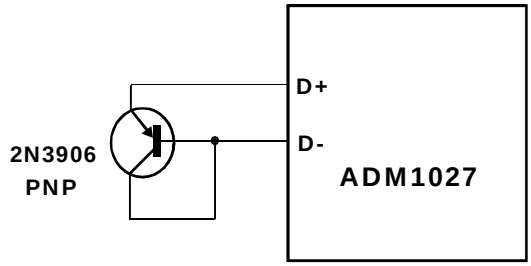


Figure 5b. Measuring Temperature Using A PNP Transistor

If a discrete transistor is used, the collector will not be grounded, and should be linked to the base. If a PNP transistor is used the base is connected to the D- input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D- input and the base to the D+ input. Figure 5 shows how to connect the ADM1027 to an NPN or PNP transistor for temperature measurement. To prevent ground noise interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode at the D- input.

To measure ΔV_{be}, the sensor is switched between operating currents of I and N x I. The resulting waveform is passed through a 65kHz lowpass filter to remove noise, and to a chopper-stabilized amplifier that performs the functions of amplification and rectification of the waveform to produce a DC voltage proportional to ΔV_{be}. This voltage is measured by the ADC to give a temperature output in 10-bit two's complement format. To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles. A remote temperature measurement takes nominally 68.27ms. The results of remote temperature measurements are stored in 10 bit, twos-complement format, as illustrated in Table 3. The extra resolution for the temperature measurements is held in the Extended Resolution Register 2 (Reg. 0x77). This gives temperature readings with a resolution of 0.25ºC.

TABLE 3. TEMPERATURE DATA FORMAT

Temperature	Digital Output (10-bit)
-128 °C	1000 0000 **00**
-125 °C	1000 0011 **00**
-100 °C	1001 1100 **00**
-75 °C	1011 0101 **00**
-50 °C	1100 1110 **00**
-25 °C	1110 0111 **00**
-10 ºC	1111 0110 **00**
0 °C	0000 0000 **00**
+10.25 °C	0000 1010 **01**
+25.5 °C	0001 1001 **10**
+50.75 °C	0011 0010 **11**
+75 °C	0100 1011 **00**
+100 °C	0110 0100 **00**
+125 °C	0111 1101 **00**
+127 °C	0111 1111 **00**

***Bold denotes 2 LSBs of measurement in Extended Resolution Register 2 (Reg. 0x77) with 0.25ºC resolution.**

SOURCES OF ERRORS ON THERMAL TRANSISTOR MEASUREMENTS

EFFECT OF IDEALITY FACTOR (*n*)

The effects of ideality factor (*n*) and beta (β) of the temperature measured by a thermal transistor are discussed below. For a thermal transistor implemented on a submicron process, such as the substrate PNP used on a Pentium III processor,the temperature errors due to the combined effect of the ideality factor and beta are shown to be less than 3 °C. Equation 2 is optimized for a substrate PNP transistor (used as a thermal diode) usually found on CPUs designed on submicron CMOS processes such as the Pentium III Processor. There is a thermal diode on each of these processors.The *n* in the Equation 2 represents the ideality factor of this thermal diode. This ideality factor is a measure of the deviation of the thermal diode from ideal behavior. According to Pentium III Processor manufacturing specifications, measured values of *n* at 100°C are:

n_{MIN} =1.0057 <$n_{TYPICAL}$ =1.008 <n_{MAX} =1.0125

The ADM1027 takes this ideality factor into consideration when calculating temperature T_{TD} of the thermal diode. The ADM1027 is optimized for $n_{TYPICAL}$ =1.008; any deviation on *n* from this typical value causes a temperature error that is calculated below for the n_{MIN} and n_{MAX} of a Pentium III Processor at T_{TD} =100°C,

$$\Delta T_{MIN} = \frac{1.0057-1.008}{1.008} *(273.15\text{Kelvin}+100°C)=-0.85°C$$

$$\Delta T_{MAX} = \frac{1.0125-1.008}{1.008} *(273.15\text{Kelvin}+100°C)=+1.67°C$$

Thus, the temperature error due variation on *n* of the thermal diode for the Pentium III Processor is about 2.5°C.

In general, this additional temperature error of the thermal diode measurement due to deviations on *n* from its typical value is given by,

$$\Delta T = \frac{n - 1.008}{1.008} *(273.15\text{Kelvin}+T_{TD}),$$ where T_{TD} is in °C

BETA OF THERMAL TRANSISTOR (β)

In Figure 6, the thermal diode is a substrate PNP transistor where the emitter current is being forced into the device. The derivation of Equation 2 above assumed that the collector currents scaled by "N " as the emitter currents were also scaled by "N." In other words, this assumes that beta (β) of the transistor is constant for various collector currents. Figure 5 shows typical beta variation versus collector current for Pentium III Processors at 100°C. The maximum beta is 4.5 and varies less than 1% over the collector current range from 7 µA to 300 µA.

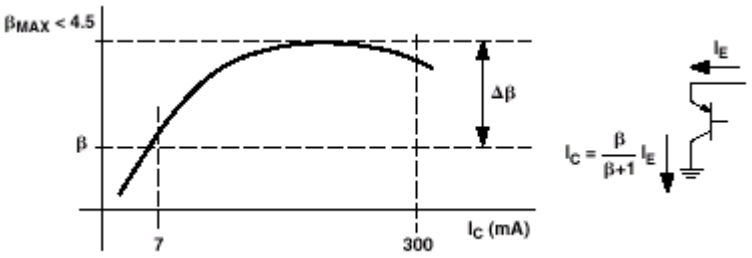


Figure 6. Variation of β with Collector Currents

Expressing the collector current in terms of the emitter current,

$I_C = I_E [\beta/(\beta+1)]$ where $\beta(300\ \mu A) = \beta(7\ \mu A)(1+\varepsilon)$, $\varepsilon = \Delta\beta/\beta$ and $\beta = \beta(7\ \mu A)$. Rewriting the equation for ΔV_{BE}, to include the ideality factor "*n*" and beta "β" we have,

$$\Delta V_{BE} = \frac{nKT}{q} * \ln\left[\frac{(1+\varepsilon) * (\beta+1)}{(1+\varepsilon)\ \beta+1} * N\right]$$

Beta variations of less than 1% (ε <0.01) contribute to temperature errors of less than 0.4 °C.

The total temperature error in the measurement will be the sum of the error due to ideality factor, the beta of the thermal transistor, plus the accuracy specification of the ADM1027.

LAYOUT CONSIDERATIONS

Digital boards can be electrically noisy environments, and care must be taken to protect the analog inputs from noise, particularly when measuring the very small voltages from a remote diode sensor. The following precautions should be taken:

1. Place the ADM1027 as close as possible to the remote sensing diode. Provided that the worst noise sources such as clock generators, data/address buses and CRTs are avoided, this distance can be 4 to 8 inches.
2. Route the D+ and D- tracks close together, in parallel, with grounded guard tracks on each side. Provide a ground plane under the tracks if possible.
3. Use wide tracks to minimize inductance and reduce noise pickup. 10 mil track minimum width and spacing is recommended.

Figure 7. Arrangement of Signal Tracks

4. Try to minimize the number of copper/solder joints, which can cause thermocouple effects. Where copper/solder joints are used, make sure that they are in both the D+ and D- path and at the same temperature.

   Thermocouple effects should not be a major problem as 1°C corresponds to about 240μV, and thermocouple voltages are about 3μV/°C of temperature difference. Unless there are two thermocouples with a big temperature differential between them, thermocouple voltages should be much less than 200μV.

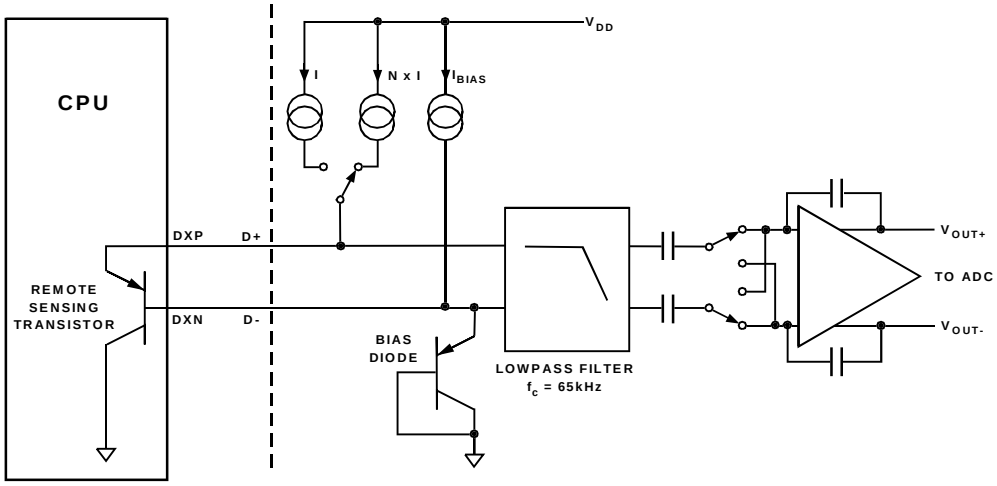


Figure 8. Signal Conditioning for Remote Diode temperature Sensors

5. Place a 0.1µF supply bypass capacitor close to the ADM1027.
6. If the distance to the remote sensor is more than 8 inches, the use of twisted pair cable is recommended. This will work up to about 6 to 12 feet.
7. For really long distances (up to 100 feet) use shielded twisted pair such as Belden #8451 microphone cable. Connect the twisted pair to D+ and D- and the shield to GND close to the ADM1027. Leave the remote end of the shield unconnected to avoid ground loops.

Because the measurement technique uses switched current sources, excessive cable and/or filter capacitance can affect the measurement.

Cable resistance can also introduce errors. 1Ω series resistance introduces about 0.5°C error.

NULLING OUT TEMPERATURE ERRORS

As CPUs run faster, it is getting more difficult to avoid high frequency clocks when routing the D+, D- traces around a system board. Even when recommended layout guidelines are followed, there may still be temperature errors, attributed to noise being coupled on to the D+/D- lines. High frequency noise generally has the effect of giving temperature measurements that are too high by a constant amount. The ADM1027 has temperature offset registers at addresses 0x70, 0x72 for the Remote 1 and Remote 2 temperature channels. By doing a one-time calibration of the system, you can determine the offset caused by system board noise and null it out using the offset registers. The Offset Registers automatically add a 2s complement 8-bit reading to every temperature measurement. This ensures that the readings in the temperature measurement registers are correct.

ADDITIONAL ADC FUNCTIONS

A number of other functions are available on the ADM1027 to offer the systems designer increased flexibility:-

TURN OFF AVERAGING

For each temperature and voltage measurement read from a value register, 16 readings have actually been taken by the ADM1027 and the results averaged, before being placed in to the value register. There may be an instance where you would like to take a very fast measurement, e.g. of CPU temperature. Setting bit 4 of Configuration Register 2 (Reg 0x73) turns averaging off.

BYPASS VOLTAGE INPUT ATTENUATORS

Setting bit 5 of Configuration Register 2 (Reg 0x73) removes the attenuation circuitry from the 2.5V, V_{CCP}, V_{CC}, 5V and 12V inputs. This allows the user to directly connect up external sensors or rescale the analog voltage measurement inputs for other applications. The input range of the ADC without the attenuators is 0V to 2.25V.

SINGLE CHANNEL ADC CONVERSIONS

Setting bit 6 of Configuration Register 2 (Reg. 0x73) places the ADM1027 in to Single channel ADC Conversion Mode. In this mode, the ADM1027 can be made to read a single channel only. If the internal ADM1027 clock is used, the selected input will be read every ??ms. The appropriate ADC Channel is selected by writing to bits <7:5> of TACH1 Minimum High Byte Register (0x55).

Bits <7:5> Reg 0x55	Channel Selected
000	2.5V
001	V_{CCP}
010	V_{CC}
011	5V
100	12V
101	Remote 1 Temp
110	Local Temp
111	Remote 2 Temp

Configuration Register 2 (Reg. 0x73)

<4> = 1 Averaging Off

<5> = 1 Bypass Input Attenuators

<6> = 1 Single Channel Convert Mode

TACH1 Minimum High Byte (Reg. 0x55)

<7:5> Selects ADC Channel for Single Channel Convert Mode

LIMIT VALUES

Limit values for analog measurements are stored in the appropriate limit registers. In the case of voltage measurements, high and low limits can be stored so that an interrupt bit will be asserted if the measured value goes above or below acceptable values. In the case of temperature, a Hot Temperature or High Limit can be programmed, and a Hot Temperature Hysteresis or Low Limit, which will usually be some degrees lower. This can be useful as it allows the system to be shut down when the hot limit is exceeded, and restarted automatically when it has cooled down to a safe temperature.

STATUS REGISTERS

The results of limit comparisons are stored in Status Registers 1 and 2. The Status Register bit for a particular measurement channel reflects the status of the last measurement and limit comparison on that channel. If a measurement is within limits the corresponding status register bit will be cleared to "0". If the measurement is out of limits the corresponding status register bit will be set to "1".

The state of the various measurement channels may be polled by reading the Status Registers over the serial bus. Bit 7 of Status Register 1 (Reg. 0x41) when set means that an out-of-limit event has been flagged in Status Register 2. This means that you need only read Status Register 2 if this bit is set. Alternatively, pin 10 can be configured as an $\overline{\text{SMBALERT}}$ output. This will automatically notify the system supervisor of an out-of-limit condition. Reading the Status registers clears the appropriate status bit as long as the error condition that caused the interrupt has cleared. Status Register bits are "sticky". Whenever a Status bit gets set, indicating an out-of-limit condition, it will remain set even if the event that caused it has gone away (until read). The only way to clear the status bit is to read the Status Register when the event has gone away. Interrupt Status Mask Registers (Reg. 0x74, 0x75) allow individual interrupt sources to be masked from causing an $\overline{\text{SMBALERT}}$. However, if one of these masked interrupt sources goes out-of-limit, its associated status bit will get set in the Interrupt Status Registers.

ANALOG MONITORING CYCLE TIME

The analog monitoring cycle begins when a one is written to the Start Bit (bit 0) of Configuration Register 1(Reg 0x40). The ADC measures each analog input in turn,and as each measurement is completed the result is automatically stored in the appropriate value register. This "round-robin" monitoring cycle continues until it is disabled by writing a 0 to bit 0 of Configuration Register 1.

As the ADC will normally be left to free-run in this manner, the time taken to monitor all the analog inputs will normally not be of interest, as the most recently measured value of any input can be read out at any time.

For applications where the monitoring cycle time is important, it can easily be calculated.

The total number of channels measured is:

4 dedicated supply voltage inputs

$3.3V_{STBY}$ or +5V supply (V_{CC} pin)

Local temperature

2 remote temperatures

As mentioned previously, the ADC performs round-robin conversions and takes 11.38ms for each voltage measurement, 22.76ms for a local temperature reading and 68.27ms for a remote temperature reading.

The total monitoring cycle time for voltage and temperature inputs is therefore nominally:

$(5 \times 11.38) + 22.76 + (2 \times 68.27) = 216.2$ms.

All fan tach measurements are made in parallel, and take nominally 728ms.

FAN DRIVE USING PWM CONTROL

The ADM1027 uses Pulse Width Modulation (PWM) techniques to control fan speed. This relies on varying the duty cycle (or on/off ratio) of a squarewave applied to the fan, to vary the fan speed. The external circuitry required to drive a fan using PWM control is extremely simple. A single NMOS FET is the only drive device required. The specifications of the MOSFET depends on the maximum current required by the fan being driven. Typical notebook fans draw a nominal 170mA, and so SOT devices can be used where board space is a concern. In desktops, fans can typically draw 250 - 300mA each. If you drive several fans in parallel from a single PWM output, or drive larger server fans, the MOSFET will need to handle the higher current requirements. The only other stipulation is that the MOSFET should have a gate voltage drive, V_{GS} < 3.3V for direct interfacing to the PWM_OUT pin. V_{GS} can be greater than 3.3V as long as the pull-up on the gate is tied to +5V. The MOSFET should also have a low on-resistance to ensure that there is not significant voltage drop across the FET. This would reduce the voltage applied across the fan and hence the maximum operating speed of the fan.

Figure 9 shows how a 3-wire fan may be driven using PWM control.

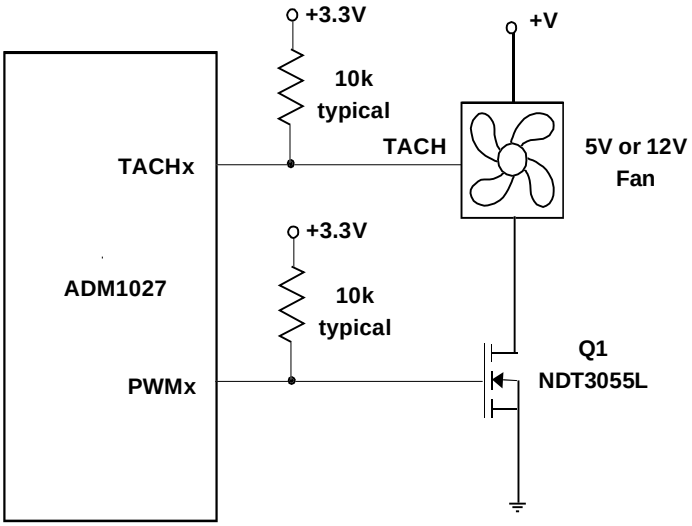


Figure 9. Interfacing a 3-wire fan to the ADM1027 using an n-channel MOSFET

Figure 9 uses a 10k pullup resistor for the TACH signal. This assumes that the TACH signal is open-collector from the fan. In all cases, the TACH signal from the fan must be kept below 6.5V maximum to prevent damaging the ADM1027. If in doubt as to whether the fan used has an open-collector or totem pole TACH output, use one of the input signal conditioning circuits shown in the **Fan Inputs** section of the datasheet.

Figure 10 shows an alternative arrangement for driving the fan using an NPN transistor such as a general purpose MMBT2222. While these devices are inexpensive, they tend to have much lower current handling capabilities and higher on-resistance than MOSFETs. When choosing a transistor, care should be taken in ensuring that it meets the fan's current requirements. You should also ensure that the base resistor is chosen such that the transistor is saturated when the fan is powered on.

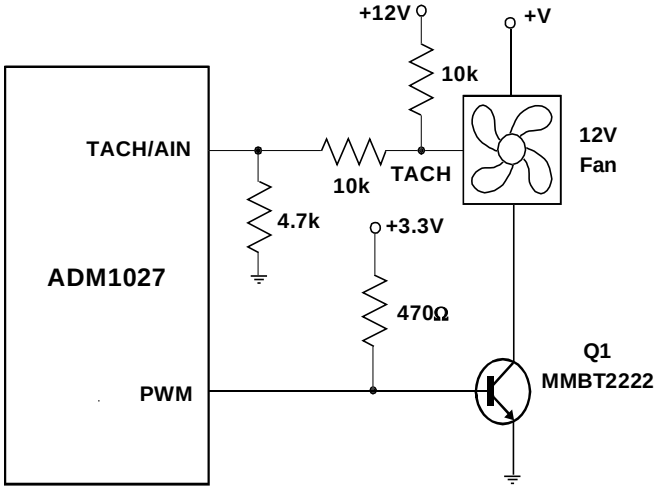


Figure 10. Interfacing a 3-wire fan to the ADM1027 using an NPN transistor

Figure 10 also shows how to connect up the TACH signal to the ADM1027 when the fan is being powered from +12V. The resistors on the TACH input ensure that the TACH signal is limited to the correct voltage range for the ADM1027.

Note that the ADM1027 has four TACH inputs available for fan speed measurement, but only three PWM drive outputs. If a fourth fan is being used in the system, then it should be driven from the PWM3 output in parallel with the third fan. Figure 13 shows how to drive two fans in parallel using low-cost NPN transistors. Figure 14 is the equivalent circuit using the NDT3055L MOSFET. Note that since the MOSFET can handle up to 3.5A, it is simply a matter of connecting another fan directly in parallel with the first.

Care should be taken in designing drive circuits with transistors and FETs to ensure that the PWM pins are not required to source current, and that they sink less than the 8mA max current specified on the datasheet.

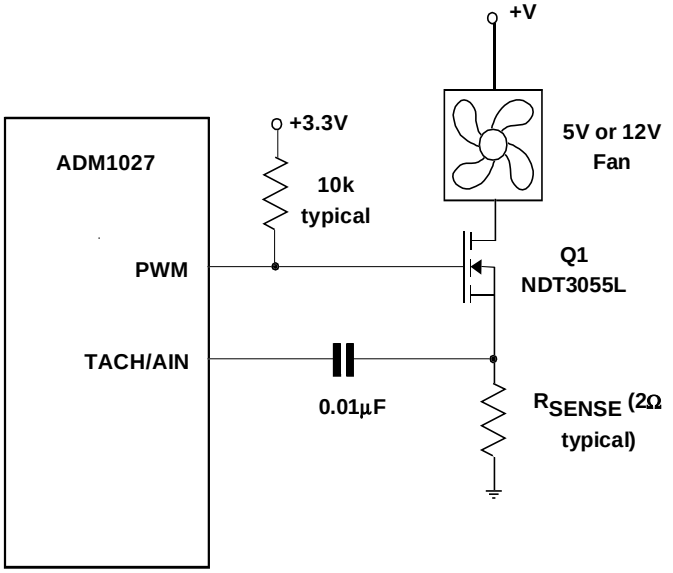


Figure 11. Interfacing the ADM1027 to a 2-wire fan

Figure 11 shows how a 2-wire fan may be connected to the ADM1027. This circuit allows the speed of a 2-wire fan to be measured even though the fan has no dedicated Tach signal. A series R_{SENSE} resistor in the fan circuit converts the fan commutation pulses in to a voltage. This is ac coupled in to the ADM1027 through the 0.01µF capacitor. On-chip signal conditioning allows accurate monitoring of fan speed. For fans drawing approximately 200mA, a 2Ω R_{SENSE} value is suitable. For fans that draw more current such as larger desktop or server fans, R_{SENSE} may be reduced. The smaller R_{SENSE} is the better, since more voltage will be developed across the fan, and the fan will spin faster. Figure 13 shows a typical plot of the sensing waveform at a TACH/AIN pin. The most important thing is that the negative going spikes are more than 250mV in amplitude. This will be the case for most fans when R_{SENSE} = 2Ω. You can reduce the value of R_{SENSE} as long as the voltage spikes at the TACH/AIN pin are greater than 250mV. This allows fan speed to be reliably determined.

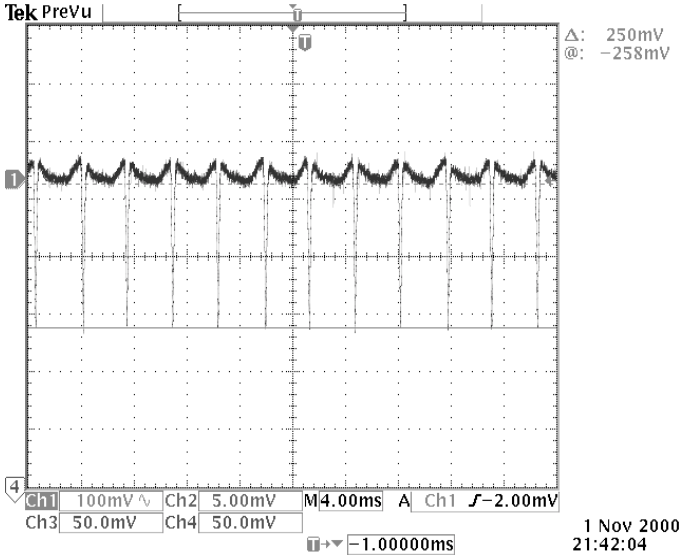


Figure 12. Fan Speed Sensing Waveform at TACH/AIN pin

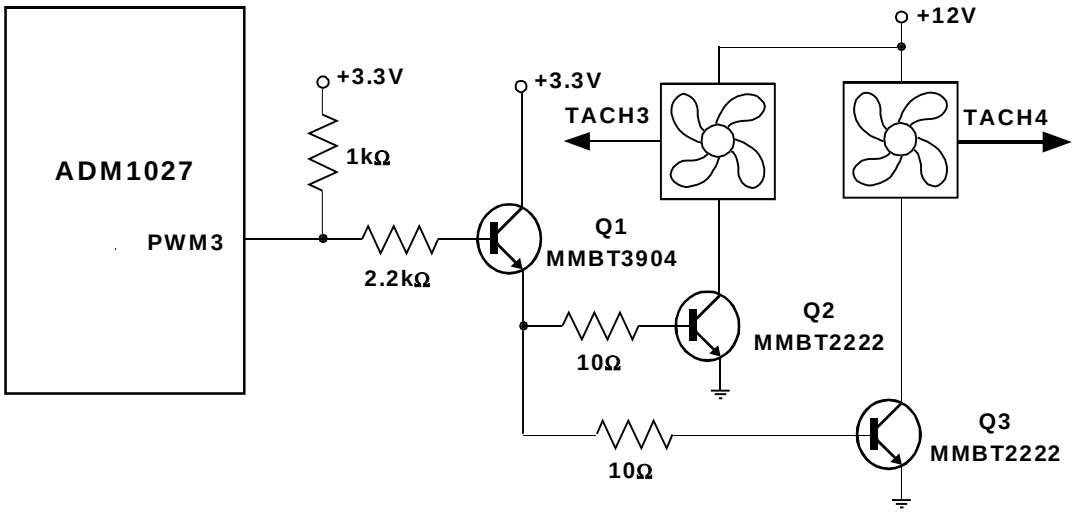


Figure 13. Interfacing 2 fans in parallel to the PWM3 output using low-cost NPN transistors

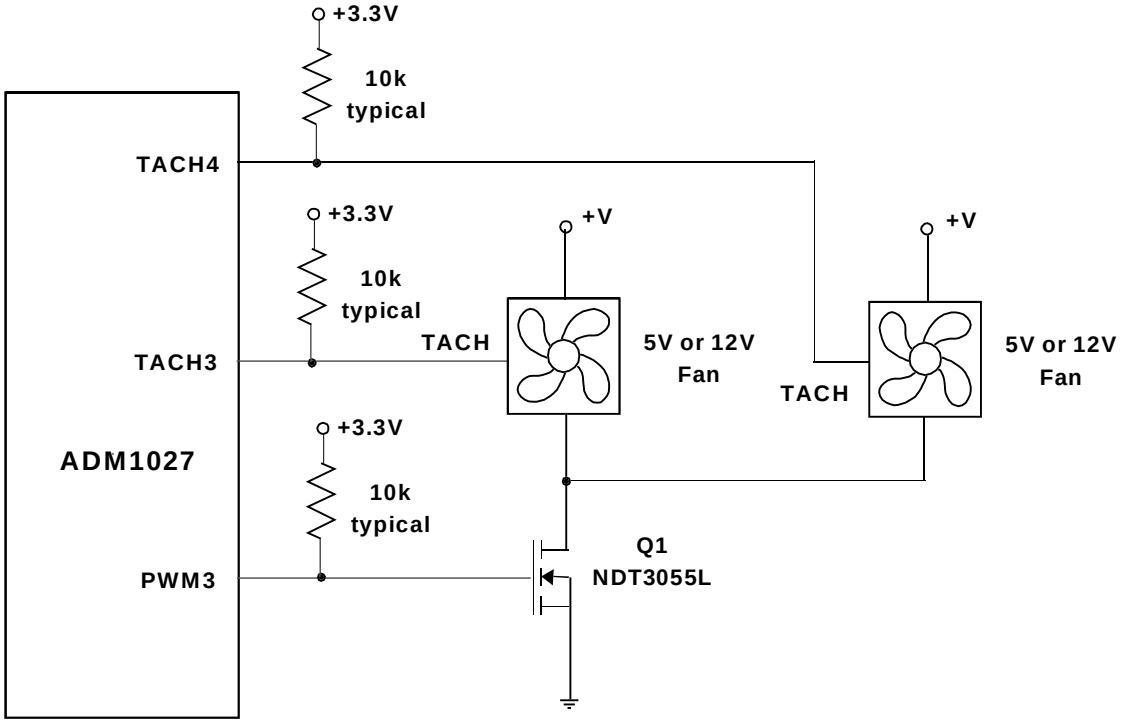


Figure 14. Interfacing 2 fans in parallel to the PWM3 output using a single N-channel MOSFET

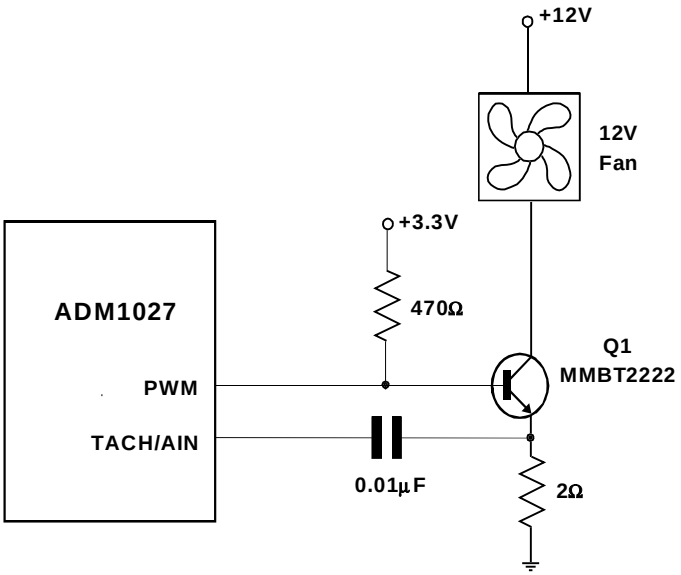


Figure 15. Interfacing the ADM1027 to a 2-wire fan using an NPN transistor

Figure 15 shows how a 2-wire fan may be connected to the ADM1027 when driven by an NPN transistor. The interface is almost identical to that using a MOSFET except that you need to calculate the base resistor value to ensure that the transistor operates in its saturation region when switched on.

Finally, Figure 16 shows how to layout a common circuit arrangement for 2-wire and 3-wire fans. Some components will not be populated depending on whether a 2-wire or 3-wire fan is being used.

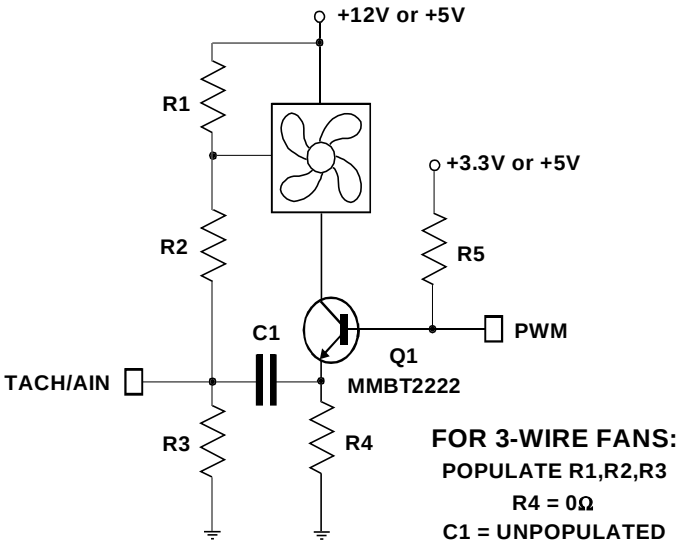


Figure 16. Accomodating 2-wire or 3-wire fans on a PCB

FAN INPUTS

Pins 11, 12, 9 and 14 are TACH inputs intended for fan speed measurement. These inputs are open-drain.

Signal conditioning in the ADM1027 accommodates the slow rise and fall times typical of fan tachometer outputs. The maximum input signal range is 0 to +6.5V, even where V_{CC} is less than 5V. In the event that these inputs are supplied from fan outputs which exceed 0 to 6.5V, either resistive attenuation of the fan signal or diode clamping must be included to keep inputs within an acceptable range.

Figures 17a to 17d show circuits for most common fan tachometer outputs.

If the fan TACH output has a resistive pullup to V_{CC} then it can be connected directly to the fan input, as shown in Figure 17a.

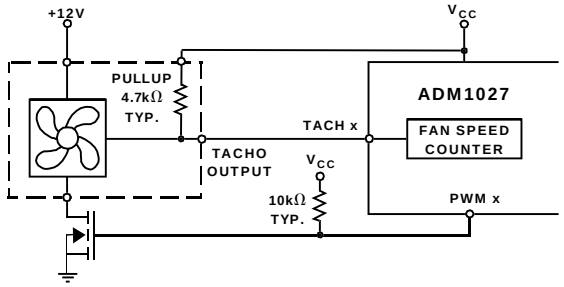


Figure 17a. Fan With Tach Pullup To $+V_{CC}$.

If the fan output has a resistive pullup to +12V (or other voltage greater than 6.5V) then the fan output can be clamped with a zener diode, as shown in Figure 17b. The zener voltage should be chosen so that it is greater than V_{IH} but less than 6.5V, allowing for the voltage tolerance of the zener. A value of between 3V and 5V is suitable.

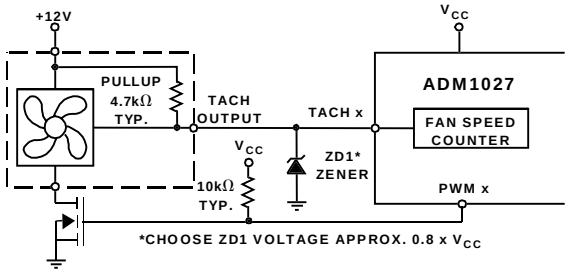


Figure 17b. Fan with Tach. Pullup to Voltage >6.5V e.g. 12V) Clamped with Zener Diode

If the fan has a strong pullup (less than 1kΩ) to +12V, or a totem-pole output, then a series resistor can be added to limit the zener current, as shown in Figure 17c. Alternatively, a resistive attenuator may be used, as shown in Figure 17d.

R1 and R2 should be chosen such that:

$2V < V_{PULLUP} \times R2/(R_{PULLUP} + R1 + R2) < 5V$

The fan inputs have an input resistance of nominally 160kΩ to ground, so this should be taken into account when calculating resistor values.

With a pullup voltage of 12V and pullup resistor less than

1kΩ, suitable values for R1 and R2 would be 100kΩ and 47kΩ. This will give a high input voltage of 3.83V.

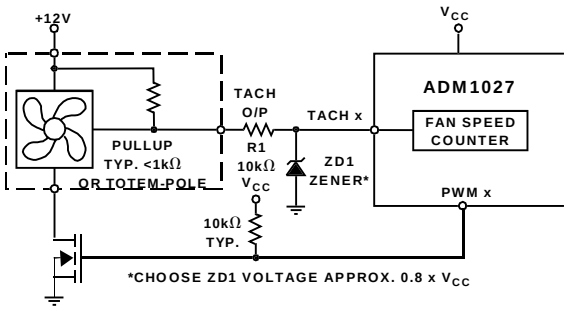


Figure 17c. Fan with Strong Tach. Pullup to >V_{CC} or Totem-Pole Output, Clamped with Zener and Resistor

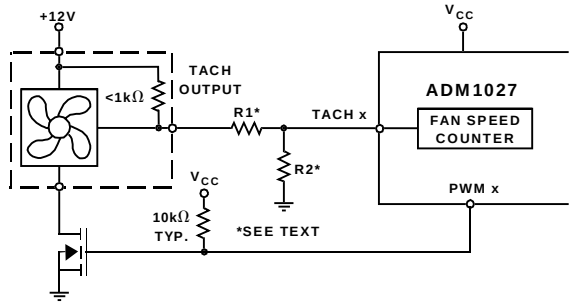


Figure 17d. Fan with Strong Tach. Pullup to >V_{CC} or Totem-Pole Output, Attenuated with R1/R2

FAN SPEED MEASUREMENT

The fan counter does not count the fan tach output pulses directly, because the fan speed may be less than 1000 RPM and it would take several seconds to accumulate a reasonably large and accurate count. Instead, the period of the fan revolution is measured by gating an on-chip 90kHz oscillator into the input of a 16-bit counter for N periods of the fan tacho output, as shown in Figure 18, so the accumulated count is actually proportional to the fan tachometer period and inversely proportional to the fan speed.

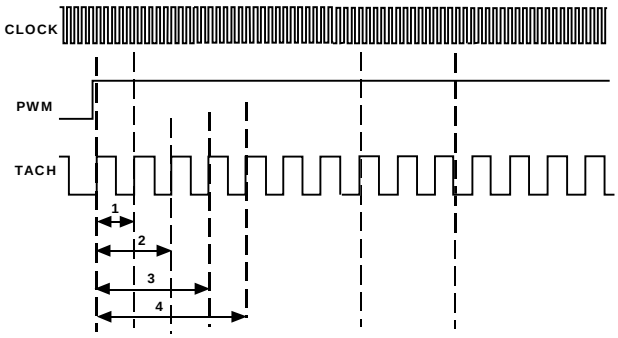


Figure 18. Fan Speed Measurement

N, the number of pulses counted is determined by the settings of Register 0x7B (Fan Pulses Per Revolution Register). This register contains 2 bits for each fan, allowing 1, 2 (default), 3 or 4 tach pulses to be counted.

The Fan Tachometer Readings are 16-bit values read back from the ADM1027 as two bytes. Since the ADM1027 does not include SMBus block read/write support, the upper and lower Fan Tachometer bytes must be read back seperately. To ensure a valid fan speed reading, the low byte of a Fan Tachometer Reading must be read first. As soon as the low byte is read, the Fan Tachometer High and Low Bytes are latched or frozen. The high and low bytes will only be updated once both bytes have been read. This is to prevent erroneous fan tach measurement readings. The relevant Fan Tachometer Reading registers are given in Table 4.

TABLE 4. FAN TACHOMETER REGISTERS

Address	Register Name
0x28	TACH1 Low Byte
0x29	TACH1 High Byte
0x2A	TACH2 Low Byte
0x2B	TACH2 High Byte
0x2C	TACH3 Low Byte
0x2D	TACH3 High Byte
0x2E	TACH4 Low Byte
0x2F	TACH4 High Byte

The Fan Tachometer Reading registers report back the number of 11.11µs period clocks (90kHz oscillator) gated to the fan speed counter, from the rising edge of the first fan tach pulse to the rising edge of the third fan tach pulse (assuming 2 pulses per revolution is being counted). Since the device is essentially measuring the fan tach period, the higher the count value, the slower the fan is actually running. A 16-bit Fan Tachometer reading of 0xFFFF indicates either that the fan has stalled or is running very slowly (<100RPM). This event will be flagged by the appropriate status bit in Status Register 2. The Fan TACH readings are normally updated once every second. The FAST bit (bit 3) of Configuration Register 3 (Reg. 0x78), when set, updates the Fan TACH readings every 250ms.

If any of the fans are not being driven by a PWM channel, but are powered directly from 5V or 12V, it's associated DC bit in Configuration Register 3 should be set. This allows tach readings to be taken on a continuous basis for fans connected directly to a DC source.

FAN PULSES PER REVOLUTION

Different fan models can output either 1, 2, 3 or 4 Tach pulses per revolution. Once the number of fan tach pulses has been determined, it can be programmed in to the Fan Pulses Per Revolution Register (Reg.0x7B) for each fan.

FAN PULSES PER REVOLUTION REGISTER

<1:0> FAN1 default = 2 pulses per rev.

<3:2> FAN2 default = 2 pulses per rev.

<5:4> FAN3 default = 2 pulses per rev.

<7:6> FAN4 default = 2 pulses per rev.

00 = 1 pulse per rev.
01 = 2 pulses per rev.
10 = 3 pulses per rev.
11 = 4 pulses per rev.

Assuming a fan outputs N tach pulses/revolution (and N is correctly set in the Fan Pulses per Revolution Register (Reg.0x7B)), fan speed is calculated by: -

Fan Speed (RPM) = (90,000 * 60)/ Fan Tach Reading

where,

Fan Tach Reading = 16-bit Fan Tachometer Reading

Example:

TACH1 High Byte (Reg 0x29) = 0x17

TACH1 Low Byte (Reg 0x28) = 0xFF

What is Fan 1 speed in RPM?

Fan 1 TACH reading = 0x17FF = 6143 decimal.

RPM = (f * 60)/Fan 1 TACH reading

RPM = (90000 * 60)/6143

Fan Speed = 879 RPM

CONFIGURING THE PWM OUTPUTS

Certain characteristics of the PWM outputs driving the fans can be adjusted. The fan start-up times can be programmed by writing to the PWM Configuration Registers (Reg. 0x5C-0x5E). The PWM logic state is set using bit 4 (INV bit) of the PWM Configuration Registers. If bit 4 = 0, the PWM output is not inverted, so 100% PWM duty cycle corresponds to a logic high output. If bit 4 = 1, then the PWM output gets inverted and 100% PWM duty cycle corresponds to an output that is always low. The PWM output drive frequencies for each output may be adjusted by writing to the T_{RANGE}/PWM Frequency Registers (Reg. 0x5F-0x61).

CONFIGURING PWM DRIVE FREQUENCY

The PWM output drive frequency for each PWM output can be adjusted to suit different fan models. Bits <2:0> of Reg. 0x5F-0x61 (T_{RANGE}, PWM Frequency Registers) determine the PWM output frequency for each PWM output. Table 5 shows how to adjust the PWM output frequency for each fan.

TABLE 5. CONFIGURING PWM DRIVE FREQUENCY

Bits<2:0>	PWM Output Frequency
000	11.0Hz
001	14.7Hz
010	22.1Hz
011	29.4Hz
100	35.3Hz (default)
101	44.1Hz
110	58.8Hz
111	88.2Hz

PWM Duty Cycle Select Mode

The ADM1027 allows the duty cycle on any of the PWM outputs to be manually adjusted. This can be useful if you wish to change fan speed in software or want to adjust PWM duty cycle output for test purposes. Bits <7:5> of Registers 0x5C-0x5E (PWM Configuration) control the behaviour of each PWM output. These bits can be used to enable each PWM output to adjust automatically with temperature. Alternatively, each PWM output may be manually controlled by setting bits <7:5> of each PWM Configuration Register = 111. Once under manual control, each PWM output may be manually updated by writing to registers 0x30-0x32 (PWMx Current Duty Cycle Registers). Table 6 shows how the PWM duty cycle for each fan may be manually written.

TABLE 6. ADJUSTING PWM DUTY CYCLE

Bits<7:0>	PWM Duty Cycle
0x00	0%
|	|
0x40	25%
|	|
0x80	50%
|	|
0xFF	100%

Likewise, by reading the PWMx Current Duty Cycle Registers you can keep track of the current duty cycle on each PWM output, even when the fans are running in Automatic Fan Speed Control Mode or Acoustic Enhancement Mode.

OVERTEMPERATURE EVENTS

Overtemperature events on any of the temperature channels can be detected and dealt with automatically. Registers 0x6A - 0x6C are the THERM limits. When a temperature exceeds its THERM limit, all fans will run at 100% duty cycle. The fans will stay running at 100% until the temperature drops below THERM - Hysteresis. The hysteresis value for that THERM limit is the value programmed into Registers 0x6D, 0x6E (Hysteresis registers). The default hysteresis value is 4°C.

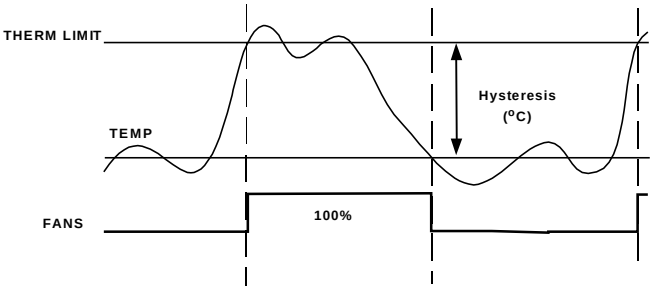


Figure 19. THERM limit operation

AUTOMATIC FAN SPEED CONTROL

The ADM1027 has a local temperature channel and 2 remote temperature channels, which may be connected to an on-chip diode-connected transistor on a CPU. These 3 temperature channels may be used as the basis for an automatic fan speed control loop to drive fans using Pulse Width Modulation (PWM). The T_{MIN} and T_{RANGE} values chosen for a given fan are critical, since these define the thermal characteristics of the system. The thermal validation of the system is one of the most important steps of the design process so these values should be chosen carefully.

HOW DOES THE CONTROL LOOP WORK?

The Automatic Fan Speed Control Loop is shown in Figure 20 below.

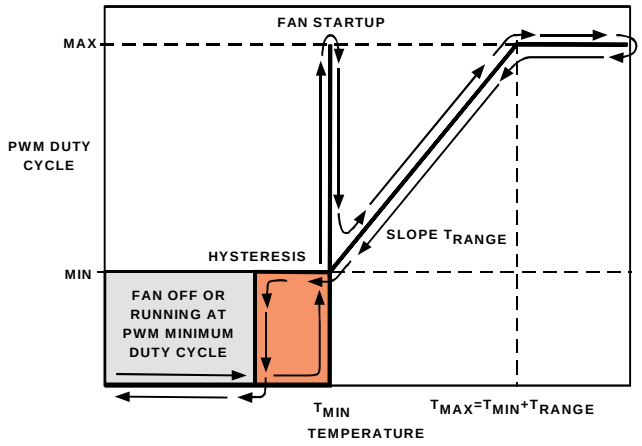


Figure 20. Automatic Fan Speed Control

In order for the fan speed control loop to work, certain loop parameters need to be programmed in to the device:-

1. **T_{MIN}**. This is the temperature at which a fan should switch on and run at minimum speed. The fan will only turn on once the temperature being measured rises above the T_{MIN} value programmed. The fan is spun up until 2 valid tach rising edges are counted. See Fan Startup Timeout section for more details. In some cases, primarily for pyscho-acoustic reasons, it is desirable that the fan never switches off, so bits <7:5> of Register 0x62 give the option of keeping the fans running at PWM Minimum Duty Cycle should the temperature be below T_{MIN}.

2. **T_{RANGE}**. This will be the temperature range over which the ADM1027 will automatically adjust fan speed. As the temperature increases beyond T_{MIN}, the PWM duty cycle will be increased accordingly. The T_{RANGE} parameter actually defines the PWM duty cycle versus temperature slope of the control loop.

3. **T_{MAX}**. This is defined as the temperature at which a fan will be at its maximum speed. At this temperature, the PWM duty cycle driving the fan will be 100%. T_{MAX} is given by T_{MIN} + T_{RANGE}. Since this parameter is the sum of the T_{MIN} and T_{RANGE} parameters, it does *not* need to be programmed in to a register on-chip.

4. **HYSTERESIS:** Programmable hysteresis is included in the control loop to prevent the fan continuously switching on and off if the temperature is close to T_{MIN}. The fan will continue to run until such time as the temperature drops below T_{MIN}-$T_{HYSTERESIS}$. The hysteresis portion of the control loop is only valid where the PWM outputs are configured to be at 0% duty cycle when the temperature is below T_{MIN} (determined by bits <7:5> of Register 0x62). Up to 15°C of hysteresis can be programmed for each Automatic Fan Speed Control Loop. Registers 0x6D, 0x6E program the hysteresis values. The hysteresis value for each control loop is 4°C by default. Care should be taken not to program hysteresis values to 0°C, as this would cause the fan to switch on and off, when the temperature is around T_{MIN}.

Register 0x6D Remote 1, Local Hysteresis

Bits <7:4> HYSR1 = Remote 1 Temp Hysteresis

Bits <3:0> HYSL = Local Temp Hysteresis

Register 0x6E Remote 2 Temp Hysteresis

Bits <7:4> HYSR2 = Remote 2 Temp Hysteresis

5. **FAN STARTUP TIMEOUT:** This defines the maximum allowable time set for the fan to output 2 valid tach rising edges. This has been determined to be a reliable way of overcoming fan inertia.

FAN STARTUP TIMEOUT

As was previously mentioned, once the temperature being measured exceeds the T_{MIN} value programmed, the fan will turn on at minimum speed (default = 50% duty cycle). In practice, the systems designer may want the fans to switch on and run at a lower duty cycle, e.g. 25%. However, the problem with fans being driven by PWM is that 25% duty cycle may not enough to reliably start the fan spinning. The solution is to start the fan until it is reliably spinning, and once the fan has spun-up, its running speed may be reduced in line with the temperature being measured. Bits <2:0> (SPIN bits) of Registers 0x5C-0x5E (PWMx Configuration Registers) control the fan startup timeout periods. This parameter sets the maximum allowable time each PWM output is held at 100% to start the fan, i.e. see two valid tach rising edges. As soon as two tach rising edges are seen from the fan, the fan is reliably started and the PWM duty cycle will drop to its normal value.

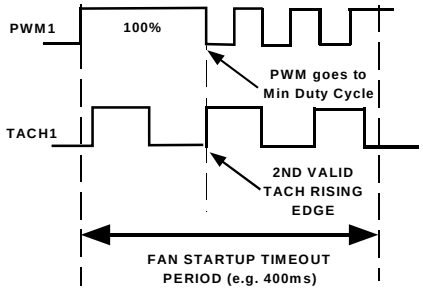


Figure 21a. Fan starts up within 400ms startup time

Figure 21a shows how a fan attached to PWM1 starts to run within 400ms fan startup time. PWM1 is driven at 100% until two valid tach rising edges are seen from the fan. PWM1 duty cycle is then set to the value held in the PWM1 Minimum Duty Cycle Register. Figure 21b shows what happens when a fan is either stuck or is unconnected on power-up. Bit 2 (FAN1) of Interrupt Status Register 2 (Reg. 0x42) gets set to indicate a fan fault.

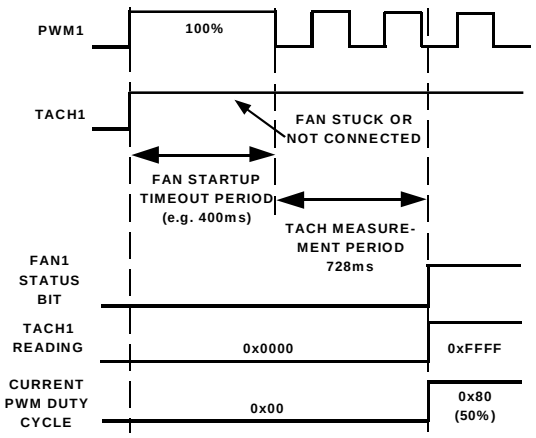


Figure 21b. Fan fails to start within 400ms startup time

Table 7 details the fan start-up timeout periods available.

TABLE 7. CONFIGURING FAN STARTUP TIMEOUT

Bits<2:0>*	Startup timeout
000	No startup timeout
001	100ms
010	250ms (default)
011	400ms
100	667ms
101	1 sec
110	2 secs
111	4 secs

*Register 0x5C = PWM1 Configuration
Register 0x5D = PWM2 Configuration
Register 0x5E = PWM3 Configuration

ADJUSTING THE SYSTEM'S THERMAL CHARACTERISTICS USING T_{RANGE}

T_{RANGE} defines how the PWM output duty cycle varies according to temperature. Once the starting temperature, T_{MIN}, has been chosen, it is T_{RANGE} that defines the thermal characteristics of the system. A very small T_{RANGE} value will cause fan speed to vary quickly with temperature. This may cause the system to be overcooled, i.e. the fan is running faster than it needs to be, producing unwanted noise. Choosing a very large T_{RANGE} may mean that the system overheats before the fan provides the necessary cooling. The T_{RANGE} value should be chosen carefully to provide adequate cooling. Once the correct thermal characteristics of the system are found through thermal validation, the system's acoustics can be adjusted seperately, as described later. For more information on Thermal and Acoustic Validation systems, contact your local Analog Devices field representative.

Figure 22 shows the different control slopes determined by the T_{RANGE} value chosen, and programmed in to the ADM1027. T_{MIN} was set to 0°C to start all slopes from the same point. It can be seen how changing the T_{RANGE} value affects the PWM Duty Cycle vs. Temperature slope. Table 8 shows the different T_{RANGE} values available for the Remote 1, Local and Remote 2 Temperature channels. Bits <7:4> (RANGE bits) of Registers 0x5F to 0x61 configure the T_{RANGE} values for each temperature channel.

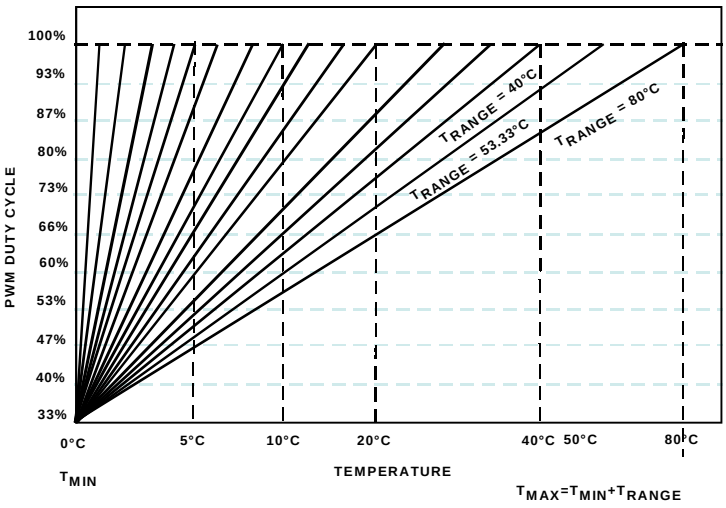


Figure 22. PWM Duty Cycle versus Temperature Slopes (T_{RANGE})

TABLE 8. CONFIGURING T_{RANGE}

Bits<7:4>*	T_{RANGE} value
0000	2°C
0001	2.5°C
0010	3.33°C
0011	4°C
0100	5°C
0101	6.67°C
0110	8°C
0111	10°C
1000	13.33°C
1001	16°C
1010	20°C
1011	26.67°C

1100	32°C (default)
1101	40°C
1110	53.33°C
1111	80°C

* Register 0x5F configures Remote 1 T_{RANGE}
Register 0x60 configures Local T_{RANGE}
Register 0x61 configures Remote 2 T_{RANGE}

Figure 23 shows how for a given T_{RANGE}, changing the T_{MIN} value affects the loop. Increasing the T_{MIN} value will increase the T_{MAX} (temperature at which the fan runs full speed) value, since $T_{MAX} = T_{MIN} + T_{RANGE}$. Note, however, that the PWM Duty Cycle vs Temperature slope remains exactly the same. Changing the T_{MIN} value merely shifts the control slope.

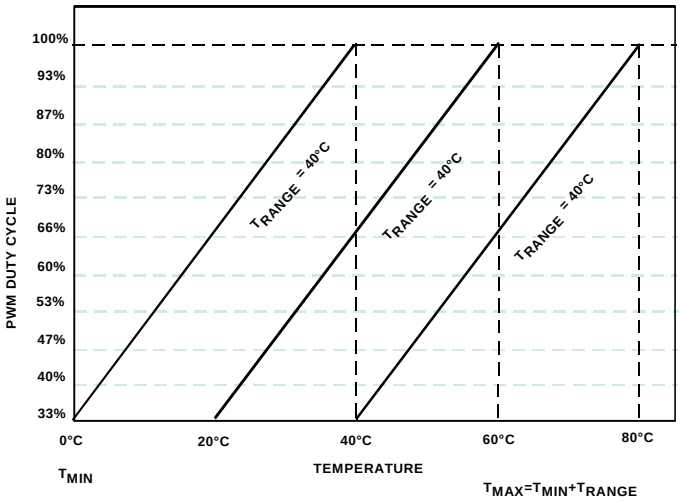


Figure 23. Effect of Increasing T_{MIN} value on Control Loop

Once the Automatic Fan Speed Control Loop parameters have been chosen, the ADM1027 device may be programmed. The ADM1027 is placed in to Automatic Fan Speed Control Mode by writing to bits <7:5> of the PWM Configuration Registers (Reg. 0x5C - 0x5E). These bits allow complete system flexibility in that they allow any of the PWM outputs to be assigned to particular temperature channels. Register 0x5C configures PWM1, 0x5D configures PWM2 and 0x5E configures PWM3.

TABLE 9. AUTO MODE FAN BEHAVIOUR

BITS <7:5>	CONTROL OPERATION (PWMx Config)
000	Remote Temp 1 controls PWMx
001	Local Temp controls PWMx
010	Remote Temp 2 controls PWMx
011	PWMx runs full-speed
100	PWMx disabled
101	Fastest Calculated Speed by Local and Remote 2 Temperature channels drives PWMx
110	Fastest Calculated Speed by all three Temperature channels drives PWMx
111	Manual Mode (PWM Duty Cycle Register may be written to output any duty cycle value.

When bits <7:5> are set to 110, this offers increased flexibility. The local and remote temperature channels can have independently programmed control loops with different control parameters. Whichever control loop calculates the fastest fan speed based on the temperature being measured, drives the fan.

Figure 24 shows how the fan's PWM duty cycle is determined by 2 independent control loops. This is the type of Auto Mode Fan Behaviour seen when bits <7:5> are set to 101. The top graph shows the control loop for the Local Temperature channel. Its T_{MIN} value has been programmed to 20°C, and its T_{RANGE} value is 40°C. The local temperature's T_{MAX} will thus be 60°C. The bottom graph shows the control loop for the Remote 2 Temperature channel. Its T_{MIN} value has been set to 0°C, while its T_{RANGE} = 80°C. Therefore, the Remote 2 Temperature's T_{MAX} value will be 80°C.

Consider, if both temperature channels measure 40°C. Both control loops will calculate a PWM duty cycle of 66%. Therefore, the fans will be driven at 66% duty cycle.

If both temperature channels measure 20°C, the Local channel will calculate 33% PWM duty cycle, whilst the Remote 2 channel will calculate 50% PWM duty cycle. Thus, the fan will be driven at 50% PWM duty cycle. Consider, the Local temperature measuring 60°C, while the Remote 2 temperature is measuring 70°C. The PWM duty cycle calculated by the Local temperature control loop will be 100% (since the temperature = T_{MAX}). The PWM duty cycle calculated by the Remote 2 temperature control loop at 70°C will be approximately 90%. So the fan will run full-speed (100% duty cycle). Remember, that the fan speed will be based on the fastest speed calculated, and is not necessarily based on the highest temperature measured. Depending on the control loop parameters programmed, a lower temperature on one channel, may actually calculate a faster speed, than a higher temperature on another channel.

PROGRAMMING THE AUTOMATIC FAN SPEED CONTROL LOOP

1. Program a value for T_{MIN}.
2. Program a value for the slope T_{RANGE}.
3. $T_{MAX} = T_{MIN} + T_{RANGE}$.
4. Program a value for Fan Startup Timeout.
5. Program the desired Automatic Fan Speed Control Mode Behaviour, i.e. which temperature channel controls each PWM output.

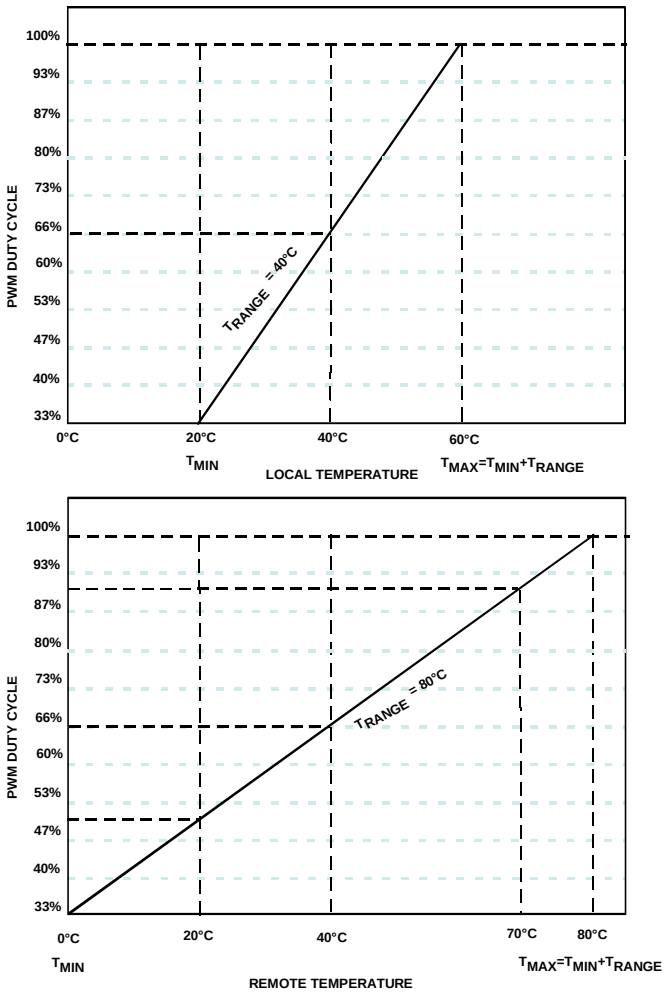


Figure 24. Max Speed Calculated by Local and Remote 2 Temperature Control Loops drives Fan

OTHER CONTROL LOOP PARAMETERS?

Having programmed all the above loop parameters, are there any other parameters to worry about?

T_{MIN} was defined as being the temperature at which a fan switched on and ran at minimum speed. This minimum speed is 50% duty cycle by default. If the minimum PWM duty cycle is programmed to 33%, then the fan control loops will operate as previously described.

It should be noted however, that changing the minimum PWM duty cycle affects the control loop behaviour.

Slope 1 of Figure 25 shows T_{MIN} set to 0°C and the T_{RANGE} chosen is 40°C. In this case, the fan's PWM duty cycle will vary over the range 33% to 100%. The fan will run full-speed at 40°C. If the minimum PWM duty cycle at which the fan runs at T_{MIN} is changed, its effect can be seen on Slopes 2 and 3. Take case 2, where the minimum PWM duty cycle is reprogrammed from 33% (default) to 53%. The fan will actually reach full-speed at a much lower temperature; 28°C. Case 3 shows that when the minimum PWM duty cycle was increased to 73%, the temperature at which the fan ran full-speed was 16°C. So the effect of increasing the minimum PWM duty cycle, with a fixed T_{MIN} and fixed T_{RANGE}, is that the fan will actually reach full-speed (T_{MAX}) at a lower temperature than T_{MIN} + T_{RANGE}. How can we calculate T_{MAX}?

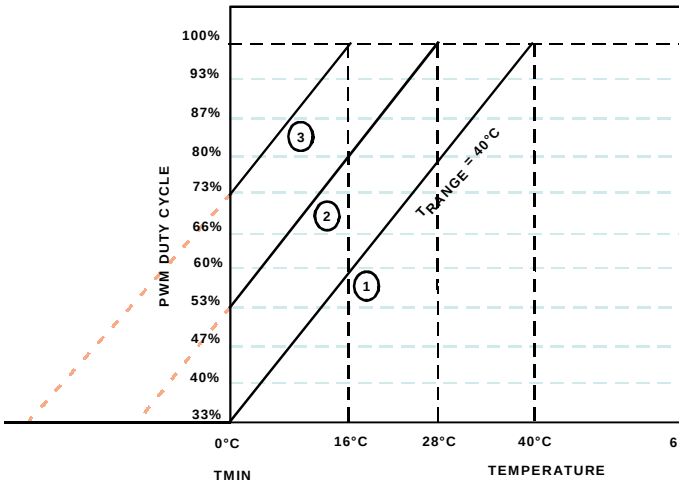


Figure 25. Effect of Changing Minimum Duty Cycle on Control Loop with fixed T_{MIN} and T_{RANGE} values

In Automatic Fan Speed Control Mode, the registers which hold the minimum PWM duty cycle at T_{MIN}, are the Minimum PWM Duty Cycle Registers (Reg 0x64-0x66). Table 10 shows the relationship between hex values written to the Minimum PWM Duty Cycle Registers and PWM duty cycle obtained.

TABLE 10. Minimum PWM Duty Cycle

BITS <7:0>	PWM Duty Cycle
0x00	0% duty cycle
|	|
0x40	25% duty cycle
|	|
0x55	33% duty cycle
|	|
0x80	50% duty cycle (default)
|	|
0xFF	100% duty cycle

The temperature at which each fan will run full-speed (100% duty cycle) is given by:-

$$T_{MAX} = T_{MIN} + ((\text{Max D.C.} - \text{Min D.C.}) * T_{RANGE}/170)$$

where,

T_{MAX} = Temperature at which fan runs full-speed

T_{MIN} = Temperature at which fan will turn on

Max D.C. = Maximum Duty Cycle (100%) = 255 decimal

Min D.C. = Duty Cycle at T_{MIN}, programmed in to PWMx Minimum Duty Cycle Register (default = 50% = 128 decimal)

T_{RANGE} = PWM Duty Cycle versus Temperature Slope

It is recommended that if you want to use the exact T_{RANGE} values listed, you set the PWMx Minimum Duty Cycle value to 33%.

Example 1:

T_{MIN} = 0°C, T_{RANGE} = 40°C

Min D.C. = 53% = 135 decimal

Calculate T_{MAX}.

$T_{MAX} = T_{MIN} + ((\text{Max D.C.} - \text{Min D.C.}) * T_{RANGE}/170)$

$T_{MAX} = 0 + ((100\%\text{D.C.} - 53\%\text{D.C.}) * 40/170)$

$T_{MAX} = 0 + ((255 - 135) * 0.235) = 28.2$

T_{MAX} = 28°C (As seen on slope 2 of Figure 25)

Example 2:

T_{MIN} = 0°C, T_{RANGE} = 40°C

Min D.C. = 73% = 186 decimal

Calculate T_{MAX}.

$T_{MAX} = T_{MIN} + ((\text{Max D.C.} - \text{Min D.C.}) * T_{RANGE}/170)$

$T_{MAX} = 0 + ((100\%\text{D.C.} - 73\%\text{D.C.}) * 40/170)$

$T_{MAX} = 0 + ((255 - 186) * 0.235) = 16.2$

T_{MAX} = 16°C (As seen on slope 3 of Figure 25)

Example 3:

T_{MIN} = 0°C, T_{RANGE} = 40°C

Min D.C. = 33% = 85 decimal

Calculate T_{MAX}.

$T_{MAX} = T_{MIN} + ((\text{Max D.C.} - \text{Min D.C.}) * T_{RANGE}/170)$

$T_{MAX} = 0 + ((100\%\text{D.C.} - 33\%\text{D.C.}) * 40/170)$

$T_{MAX} = 0 + ((255 - 85) * 0.235) = 40$

T_{MAX} = 40°C (As seen on slope 1 of Figure 25)

In this case, since the Minimum Duty Cycle is the default 33%, the equation for T_{MAX} reduces to:-

$T_{MAX} = T_{MIN} + ((\text{Max D.C.} - \text{Min D.C.}) * T_{RANGE}/170)$

$T_{MAX} = T_{MIN} + ((255 - 85) * T_{RANGE}/170)$

$T_{MAX} = T_{MIN} + (170 * T_{RANGE}/170)$

$T_{MAX} = T_{MIN} + T_{RANGE}$

REGISTERS FOR AUTOMATIC FAN SPEED CONTROL MODE

Registers 0x5C to 0x5E PWMx Configuration Registers

<7:5> 000 = Remote Temp 1 controls PWMx
001 = Local Temp controls PWMx
010 = Remote Temp 2 controls PWMx
011 = PWMx runs full-speed
100 = PWMx disabled
101 = Fastest speed calculated by Local and Remote Temp 2 controls PWMx
110 = Fastest speed calculated by all three temperature channels controls PWMx
111 = Manual PWM Duty Cycle Mode

<4> INV; Set to 1, 100% PWM duty cycle outputs logic low, set to 0, 100% duty cycle = high o/p.

<2:0> Fan Startup Timeout
000 = No Startup Timeout
001 = 100ms
010 = 250ms
011 = 400ms
100 = 667ms
101 = 1 sec
110 = 2 secs
111 = 4 secs

Registers 0x5F to 0x61 T_{RANGE}/PWM FREQ Registers

<2:0> PWM Frequency driving the fan
000 = 11.0Hz
001 = 14.7Hz
010 = 22.1Hz
011 = 29.4Hz
100 = 35.3Hz (default)
101 = 44.1Hz
110 = 58.8Hz
111 = 88.2Hz

<7:4> T_{RANGE}

0000 = 2°C
0001 = 2.5°C
0010 = 3.33°C
0011 = 4°C
0100 = 5°C
0101 = 6.67°C
0110 = 8°C
0111 = 10°C
1000 = 13.33°C
1001 = 16°C
1010 = 20°C
1011 = 26.67°C
1100 = 32°C (default)
1101 = 40°C
1110 = 53.33°C
1111 = 80°C

*Note that these T_{RANGE} values assume that the PWM Minimum Duty Cycle is 33%. If the minimum PWM duty cycle value is different, the T_{RANGE} values are different. Table 11 below shows the effective T_{RANGE} values for PWM duty cycles of 50%, 40% 33%, 25% and 20%.

Registers 0x64 to 0x55 Minimum PWM Duty Cycle

<7:0> These bits define the minimum PWM duty cycle for PWMx when being run in Automatic Fan Speed Control Mode.

Registers 0x67 to 0x69 T_{MIN} Registers

<7:0> These bits define the T_{MIN} values for Automatic Fan Speed Control Mode for each temperature channel.

Registers 0x6D, 0x69 Temperature Hysteresis Registers

These registers allow up to 15°C of hysteresis to be programmed for each temperature channel to prevent fans cycling on and off in Automatic Fan Speed Control Mode.

TABLE 11. T_{RANGE} VALUES CALCULATED FOR PWM MINIMUM DUTY CYCLE SETTINGS

Min Duty Cycle	50% (default)	40%	33%	25%	20%
Bit settings	**T_{RANGE}**	**T_{RANGE}**	**T_{RANGE}**	**T_{RANGE}**	**T_{RANGE}**
0000	1.5°C	1.8°C	2°C	2.25°C	2.4°C
0001	1.9°C	2.25°C	2.5°C	2.8°C	3°C
0010	2.5°C	3°C	3.33°C	3.74°C	4°C
0011	3°C	3.6°C	4°C	4.5°C	4.8°C
0100	3.7°C	4.5°C	5°C	5.6°C	6°C
0101	5°C	6°C	6.67°C	7.5°C	8°C
0110	6°C	7.2°C	8°C	9°C	9.6°C
0111	7.5°C	9°C	10°C	11°C	12°C
1000	10°C	12°C	13.33°C	15°C	16°C
1001	12°C	14°C	16°C	18°C	19°C
1010	15°C	18°C	20°C	23°C	24°C
1011	20°C	24°C	26.67°C	30°C	32°C
1100	24°C	29°C	32°C	36°C	38°C
1101	30°C	36°C	40°C	45°C	48°C
1110	40°C	48°C	53.33°C	60°C	64°C
1111	60°C	72°C	80°C	90°C	96°C

ENHANCING SYSTEM ACOUSTICS

The Automatic Fan Speed Control Loop reacts instantaneously to changes in temperature, i.e. the PWM duty cycle will respond immediately to temperature change. In certain circumstances, we may not want the PWM output to react instantaneously to temperature changes. If temperature was found to be varying drastically in a system, this would have the effect of cycling the fan speed up and down, which could be obvious to someone in close proximity. One way to improve the system's acoustics would be to slow down the loop, so that fans ramp slowly to the newly calculated fan speed. This also ensures that temperature transients will effectively be ignored, and the fan's operation will be smooth.

THE APPROACH

There are two different approaches to implementing System Acoustic Enhancement. The first method would be to "smooth" transient temperatures as they are measured by a temperature source, e.g. Remote 1 Temperature. The temperature values used to calculate PWM duty cycle values would be smoothed, reducing fan speed. However, this approach would cause an inherent delay in updating fan speed and would cause the thermal characteristics of the system to change. It would also cause the system fans to stay on longer than necessary, since the fan's reaction is merely delayed. The user would also have no control over noise from different fans, driven by the same temperature source. Consider controlling a CPU Cooler Fan (on PWM1) and a Chassis Fan (on PWM2) using Remote 1 Temperature. Because the Remote 1 Temperature is smoothed, both fans will be updated at exactly the same rate. If the Chassis Fan is much louder than the CPU Fan, there is no way to improve its acoustics without changing the thermal solution of the CPU Cooling Fan.

The second approach is to control the PWM duty cycle driving the fan at a fixed rate, e.g. 6%. Each time the PWM duty cycle is updated, it is incremented by a fixed 6%. So the fan ramps smoothly to it's newly calculated speed. If the temperature starts to drop, the PWM duty cycle immediately decreases by 6% every update. So the fan ramps smoothly up or down without inherent system delay. Consider controlling the same CPU Cooler fan (on PWM1) and Chassis Fan (on PWM2) using Remote 1 Temperature. The T_{MIN} and T_{RANGE} settings have already been defined in Automatic Fan Speed Control Mode, i.e. thermal characterisation of the control loop has been optimized. Now the Chassis Fan is noisier than the CPU Cooling Fan. So PWM2 can be placed in to Acoustic Enhancement Mode independently of PWM1. The acoustics of the Chassis Fan can therefore be adjusted without affecting the acoustic behaviour of the CPU Cooling Fan, even though both fans are being controlled by Remote 1 Temperature. This is how Acoustic Enhancement works on the ADM1027.

The Acoustic Enhancement Mode on the ADM1027 is invoked by setting bit 3 of the Enhance Acoustics Register 1 (Reg. 0x62) for PWM1, bit 7 of Enhance Acoustics Register 2 (Reg. 0x63) for PWM2, and bit 3 for PWM3.

Enabling Acoustic Enhancement for each PWM output

Enhance Acoustics Register 1 (Reg. 0x62)

<3> = 1 Enables Acoustic Enhancement on PWM1 output.

Enhance Acoustics Register 2 (Reg. 0x63)

<7> = 1 Enables Acoustic Enhancement on PWM2 output.

<3> = 1 Enables Acoustic Enhancement on PWM3 output.

Effect of Ramp Rate on Enhanced Acoustics Mode

Bits <2:0> of Registers 0x62 and 0x63 (Enhance Acoustics Registers) determine the ramp rate for PWM1 and PWM2. Bits <6:4> of Reg. 0x63 sets the ramp rate for PWM3. The PWM signal driving the fan will have a period, T, given by the PWM drive frequency, f, since T = 1/f. For a given PWM period, T, the PWM period is subdivided in to 255 equal timeslots. One timeslot corresponds to the smallest possible increment in PWM duty cycle. A PWM signal of 33% duty cycle will thus be high for 1/3*255 timeslots and low for 2/3*255 timeslots. Therefore, 33% PWM duty cycle corresponds to a signal which is high for 85 timeslots and low for 170 timeslots.

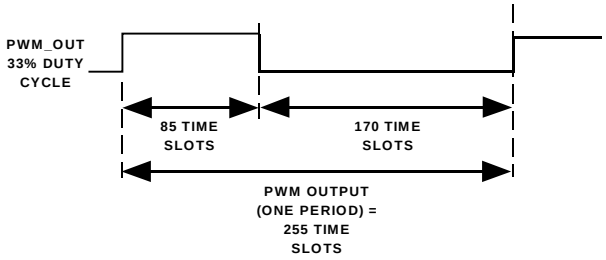


Figure 26. 33% PWM duty cycle represented in timeslots

The ramp rates in Enhanced Acoustics Mode are selectable between 1, 2, 3, 5, 8, 12, 24 and 48. The ramp rates are actually discrete timeslots. For example, if the ramp rate = 8, then 8 timeslots will be added to the PWM high duty cycle each time the PWM duty cycle needs to be increased. Figure 27 shows how the Enhanced Acoustics Mode algorithm operates.

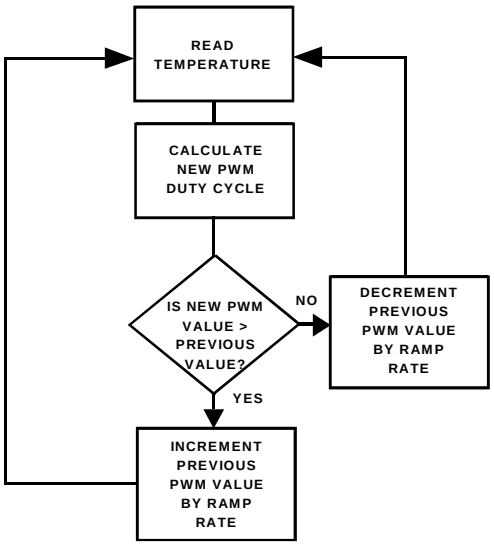


Figure 27. Enhanced Acoustics Mode Algorithm

The Enhanced Acoustics Mode algorithm calculates a new PWM duty cycle based on the temperature measured. If the new PWM duty cycle value is greater than the previous PWM value, then the previous PWM duty cycle value is incremented by either 1, 2, 3, 5, 8, 12, 24 or 48 timeslots (depending on the settings of the Enhance Acoustics Registers). If the new PWM duty cycle value is less than the previous PWM value, then the previous PWM duty cycle is decremented by 1, 2, 3, 5, 8, 12, 24 or 48 timeslots. Each time the PWM duty cycle is incremented or decremented, it is stored as the previous PWM duty cycle for the next comparison.

A Ramp Rate of 1 corresponds to 1 time slot, which is 1/ 255 of the PWM period. In Enhanced Acoustics Mode, incrementing or decrementing by 1, changes the PWM output by 1/255 * 100%.

TABLE 12. EFFECT OF RAMP RATES ON PWM O/P

RAMP RATE	TIME FROM 33% TO 100%
1	35 secs
2	17.6 secs
3	11.8 secs
5	7 secs
8	4.4 secs
12	3 secs
24	1.6 secs
48	0.8 secs

So programming a ramp rate value simply increases or decreases the PWM duty cycle by the amounts shown in Table 12, depending on whether the temperature is increasing or decreasing. Table 12 also lists the amount of time it takes for the PWM output duty cycle to increase from 33% to 100% duty cycle. This assumes that a temperature reading is updated every 216.2ms.

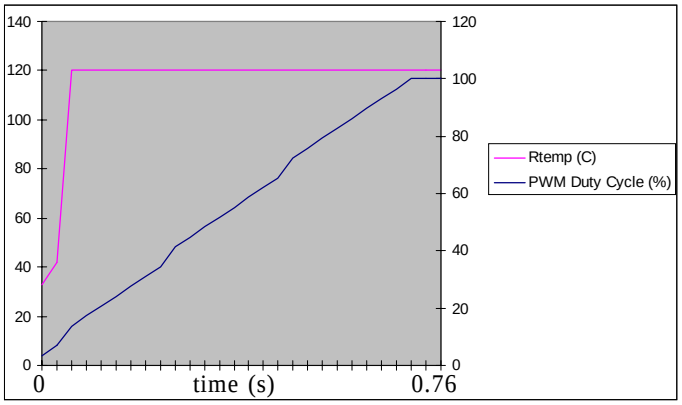


Figure 28. Enhanced Acoustics Mode with Ramp Rate = 48

Figure 28 shows remote temperature plotted against PWM duty cycle for Enhanced Acoustics Mode. The ramp rate is set to 16 which would correspond to the fastest ramp rate. Assume that a new temperature reading is available every 216.2ms. With these settings it took approximately 0.76 seconds to go from 33% duty cycle to 100% duty cycle (full-speed). The T_{MIN} value = 32°C and the T_{RANGE} = 80°C. It can be seen that even though the temperature increased very rapidly, the fan ramps up to full speed gradually.

Figure 29 shows how changing the ramp rate from 48 to 8 affects the control loop. The overall response of the fan is slower. Since the ramp rate is reduced, it takes longer for the fan to achieve full running speed. In this case, it took approximately 4.4 seconds for the fan to reach full speed.

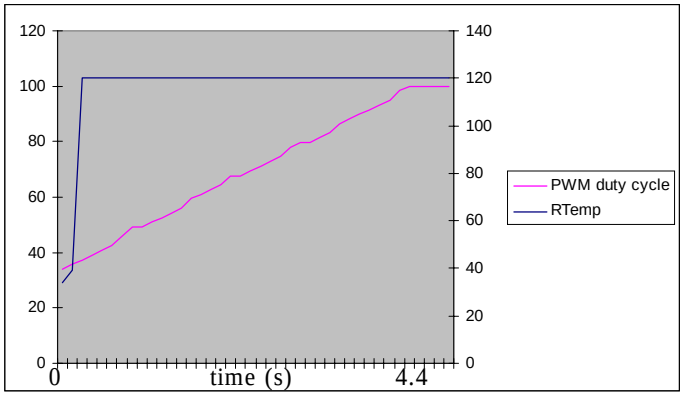


Figure 29. Enhanced Acoustics Mode with Ramp Rate = 8

Figure 30 shows the PWM output response for a ramp rate of 2. In this instance the fan took about 17.6 seconds to reach full running speed.

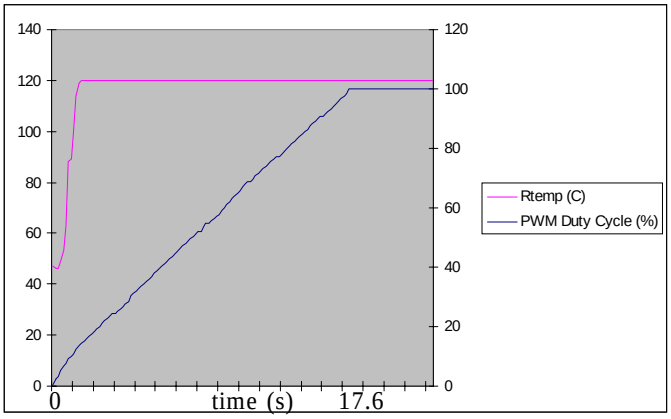


Figure 30. Enhanced Acoustics Mode with Ramp Rate = 2

Finally, Figure 31 shows how the control loop reacts to temperature with the slowest ramp rate. The ramp rate is set to 1, while all other control parameters remain the same. With the slowest ramp rate selected it took 35 seconds for the fan to reach full speed.

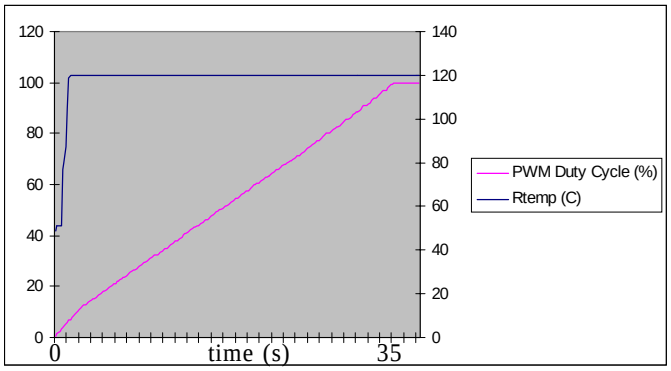


Figure 32. Enhanced Acoustics Mode with Ramp Rate = 1

As can be seen from Figures 28 thru 32, the rate at which the fan will react to temperature change is dependent on the ramp rate selected in the Enhance Acoustics Registers. The higher the ramp rate, the faster the fan will reach the newly calculated fan speed.

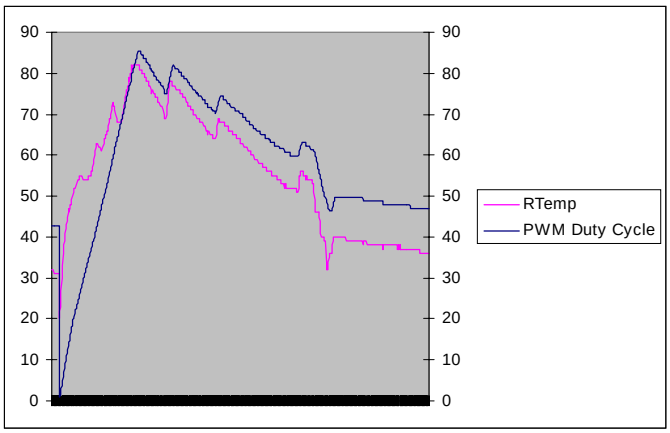


Figure 32. How Fan reacts to Temperature Variation in Enhanced Acoustics Mode

Figure 32 shows the behaviour of the PWM output as temperature varies. As the temperature is rising, the fan speed will ramp up. Small drops in temperature will not affect the ramp-up function since the newly calculated fan speed will still be higher than the previous PWM value. The Enhanced Acoustics Mode allows the PWM output to be made less sensitive to temperature variations. This will be dependent on the ramp rate selected and programmed in to the Enhance Acoustics Registers.

REGISTERS FOR ENHANCED ACOUSTICS MODE

In addition to the registers used to program the Automatic Fan Speed Control Mode, the following registers need to be programmed :-

Register 0x62 Enhance Acoustics Register 1

<3> EN1:- when this bit is set to 1, it enables acoustic enhancement on PWM1.

<2:0> ACOU :- these bits set the ramp rate for Acoustic Enhancement on PWM1
000 = 1 (Time = 35 secs)
001 = 2 (Time = 17.6 secs)
010 = 3 (Time = 11.8 secs)
011 = 5 (Time = 7 secs)
100 = 8 (Time = 4.4 secs)
101 = 12 (Time = 3 secs)
110 = 24 (Time = 1.6 secs)
111 = 48 (Time = 0.8 secs)

Register 0x63 Enhance Acoustics Register 2

<7> EN2:- when this bit is set to 1, it enables acoustic enhancement on PWM2.

<6:4> ACOU2 :- these bits set the ramp rate for Acoustic Enhancement on PWM2.
000 = 1 (Time = 35 secs)
001 = 2 (Time = 17.6 secs)
010 = 3 (Time = 11.8 secs)
011 = 5 (Time = 7 secs)
100 = 8 (Time = 4.4 secs)
101 = 12 (Time = 3 secs)
110 = 24 (Time = 1.6 secs)
111 = 48 (Time = 0.8 secs)

<3> EN3:- when this bit is set to 1, it enables acoustic enhancement on PWM3.

<2:0> ACOU3 :- these bits set the ramp rate for Acoustic Enhancement on PWM3.
000 = 1 (Time = 35 secs)
001 = 2 (Time = 17.6 secs)
010 = 3 (Time = 11.8 secs)
011 = 5 (Time = 7 secs)
100 = 8 (Time = 4.4 secs)
101 = 12 (Time = 3 secs)
110 = 24 (Time = 1.6 secs)
111 = 48 (Time = 0.8 secs)

PROGRAMMING THE ENHANCED ACOUSTICS MODE

1. Program a value for T_{MIN}.
2. Program a value for the slope T_{RANGE}.
3. $T_{MAX} = T_{MIN} + T_{RANGE}$.
4. Program a value for Fan Startup Timeout.
5. Program the desired Automatic Fan Speed Control Mode Behaviour, i.e. which temperature channel controls each fan.
6. Evaluate the thermal characteristics of the system with the T_{MIN} and T_{RANGE} values selected.
7. If necessary, change the T_{MIN} and T_{RANGE} values until the thermal design is optimized.
6. Program a ramp rate for the Enhanced Acoustics Mode.
7. Enable Acoustics Enhancement by setting the Enable bits in the Enhance Acoustics Registers.
8. Evaluate the acoustic performance of the system. Tweak if necessary. Ensure that the thermal characteristics of the design are still being met.

MONITORING $\overline{\text{PROCHOT}}$ SIGNAL

The ADM1027 allows the Intel Pentium 4 processor's $\overline{\text{PROCHOT}}$ signal to be monitored when the CPU is forced to clock-modulate due to critical CPU temperature. Ideally, the thermal design of the system is such that the Thermal Control Circuit (TCC) of the CPU never gets activated. In practice, there are a number of things beyond the control of the systems board designer which can cause the TCC to activate and $\overline{\text{PROCHOT}}$ to assert. These include: -

1. Improper mounting of the CPU heatsink.
2. Too much thermal grease.
3. Insufficient thermal grease.
4. Underrated heatsink.
5. Fan Failures.
6. Inadequate airflow in the chassis.
7. Too many high power peripherals (PCI, AGP, HDD, DVD, etc) for the fans to adequately cool.

The ADM1027 can detect when $\overline{\text{PROCHOT}}$ is first asserted and when the $\overline{\text{PROCHOT}}$ signal negates. It can also measure the duration that $\overline{\text{PROCHOT}}$ has been asserted for (measuring the extremity of the performance hit), and generate an interrupt. A $\overline{\text{PROCHOT}}$ limit can be set to ignore short $\overline{\text{PROCHOT}}$ assertions, but to report longer $\overline{\text{PROCHOT}}$ assertions, which could signify a more serious thermal problem with the system. Being able to monitor and time $\overline{\text{PROCHOT}}$ is also very useful for thermal validation, when configuring the thermal characteristics of the system (T_{MIN} and T_{RANGE} settings for Automatic Fan Speed Control).

It can be expected that a system that monitors $\overline{\text{PROCHOT}}$ will be quieter than a system that does not. This is because the system software can self-calibrate, and allow the CPU run closer to it's thermal limits.

Pin 14 can be configured as the $\overline{\text{PROCHOT}}$ input by setting bit 1 (PHOT) of Configuration Register 3 (Reg. 0x78). Once pin 14 is configured as an input, it can be programmed to run all fans 100% whenever $\overline{\text{PROCHOT}}$ is asserted low, by setting bit 2 (BOOST) of Configuration Register 3 (Reg. 0x78). Figure 33 shows the $\overline{\text{PROCHOT}}$ events that are captured in the $\overline{\text{PROCHOT}}$ Status Register (Reg. 0x79).

Bit 7 (ASRT) of the PROCHOT Status Register (Reg. 0x79) gets set high when the $\overline{\text{PROCHOT}}$ signal asserts low. This also starts the 6-bit timer, TMR, to measure the duration of the $\overline{\text{PROCHOT}}$ assertion. The ASRT bit gets cleared on a read of the PROCHOT Status Register. Once the $\overline{\text{PROCHOT}}$ signal goes high, bit 6 (NEG) of the PROCHOT Status Register gets set high to indicate the negation of $\overline{\text{PROCHOT}}$. At this point, the timer, TMR, is stopped. Bit 6 gets cleared on a read of the PROCHOT Status Register. While $\overline{\text{PROCHOT}}$ is asserted low, all fans will run at 100% to provide critical cooling if bit 2 (BOOST) of Configuration Register 3 (Reg. 0x78) is set. To ensure a valid reading of the $\overline{\text{PROCHOT}}$ duration, only read the TMR bits after bit 6 (NEG) has been set.

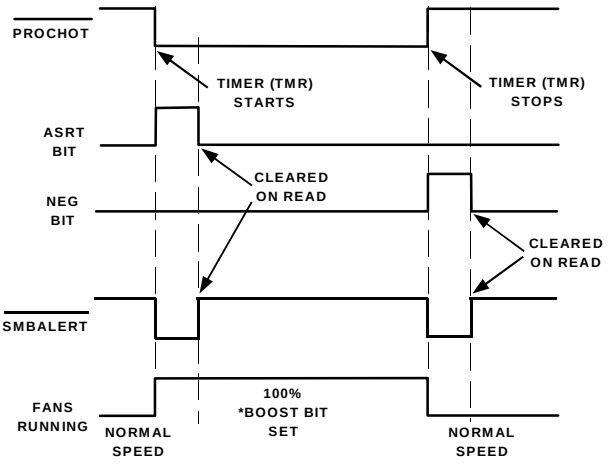


Figure 33. $\overline{\text{PROCHOT}}$ and $\overline{\text{SMBALERT}}$ Timing Behaviour

MEASURING $\overline{\text{PROCHOT}}$ ASSERTION TIME

The PROCHOT Status Register (Reg. 0x79) holds a 6-bit timer (TMR) to measure the $\overline{\text{PROCHOT}}$ assertion time. The 6-bit timer resolution allows a $\overline{\text{PROCHOT}}$ assertion time from 125ms to 7.875 seconds to be measured. This allows software to not only detect the occurrence of $\overline{\text{PROCHOT}}$ events, but also the severity of the critical temperature. Occasional short $\overline{\text{PROCHOT}}$ assertions may be of little concern to the systems designer, but long, regular $\overline{\text{PROCHOT}}$ assertions can point to poor thermal design, or a hardware-specific problem. Remember that for every $\overline{\text{PROCHOT}}$ assertion, the system's performance is dramatically reduced.

CONFIGURING A $\overline{\text{PROCHOT}}$ ASSERTION LIMIT

The user can determine the severity of a $\overline{\text{PROCHOT}}$ assertion time before generating an interrupt using the PROCHOT Mask Register (Reg. 0x7A). Bits <5:0> are a 6-bit timer limit (LIMT) for $\overline{\text{PROCHOT}}$. The 6-bit TMR value of the PROCHOT Status Register is automatically compared with the 6-bit timer limit (LIMT). If the TMR value exceeds the programmed LIMT value, then an interrupt is generated. In this way, it is possible to ignore short $\overline{\text{PROCHOT}}$ assertions, while reporting longer, more severe $\overline{\text{PROCHOT}}$ assertions to systems management software. Since the LIMT value is a

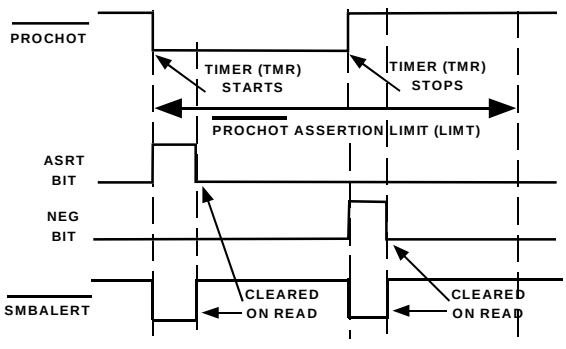


Figure 34a. $\overline{\text{PROCHOT}}$ activation below LIMT

6-bit limit, it allows timer limits from 125ms to 7.875 seconds to be programmed. If the TMR value exceeds the LIMT value, bit 5 (F4P) of Status Register 2 (Reg. 0x42) gets set. Figure 33a shows how the SMBALERT behaves for a PROCHOT assertion below the LIMT value.

Figure 34b shows how the SMBALERT behaves when the PROCHOT TMR exceeds the LIMT value. On the rising edge of PROCHOT (signal is negated), the NEG bit and F4P bit gets set. This generates an SMBALERT, and is cleared on a read of the PROCHOT Status Register. Bit 5 (F4P) of Interrupt Status Register 2 (Reg. 0x42) gets set since the timer value, TMR, has exceeded the limit value, LIMT. This causes an SMBALERT indicating that the PROCHOT assertion time has exceeded the acceptable PROCHOT assertion time limit, LIMT.

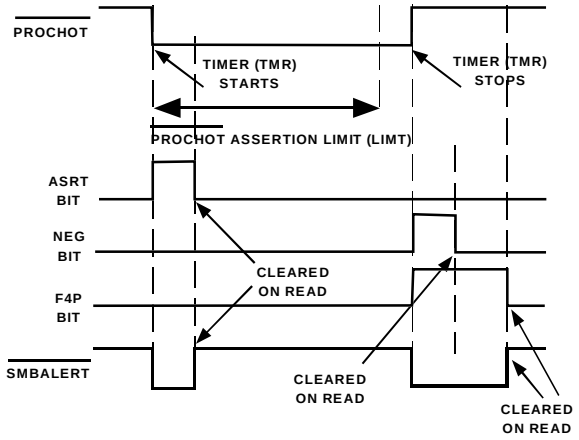


Figure 34b. PROCHOT activation above LIMT

In Figures 34a and 34b, whenever PROCHOT is asserted or negated, an SMBALERT is generated. In some cases you may want to ignore when PROCHOT is asserted and negated for short durations, and only generate an SMBALERT for PROCHOT assertion durations greater than the limit value, LIMT, programmed. By setting bits 7 (ASRT) and 6 (NEG) in the PROCHOT Mask Register (0x7A) it is possible to mask out interrupts when PROCHOT is asserted and negated. Figure 34c shows how the SMBALERT output behaves when the ASRT and NEG bits are masked in the PROCHOT Mask Register.

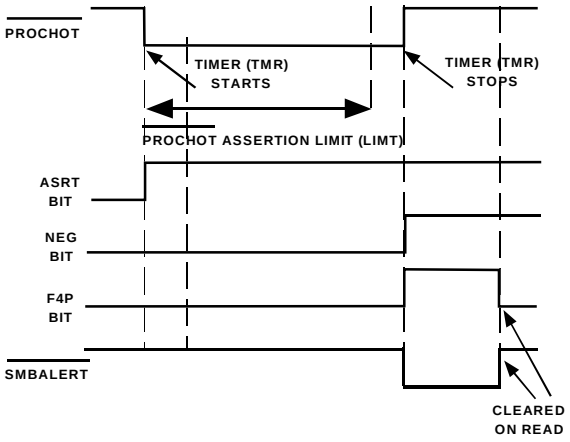


Figure 34c. PROCHOT activation above LIMT with ASRT/ NEG bits masked

XOR TREE TEST MODE

The ADM1027 includes an XOR Tree Test Mode. This mode is useful for in-circuit test equipment at board-level testing. By applying stimulus to the pins included in the XOR Tree, it's possible to detect opens or shorts on the system board. Figure 35 shows the signals that are exercised in the XOR Tree Test Mode.

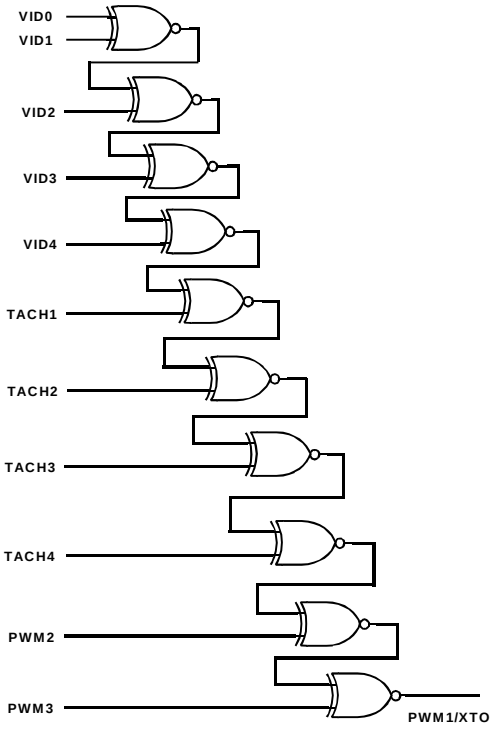


Figure 35. XOR Tree Test

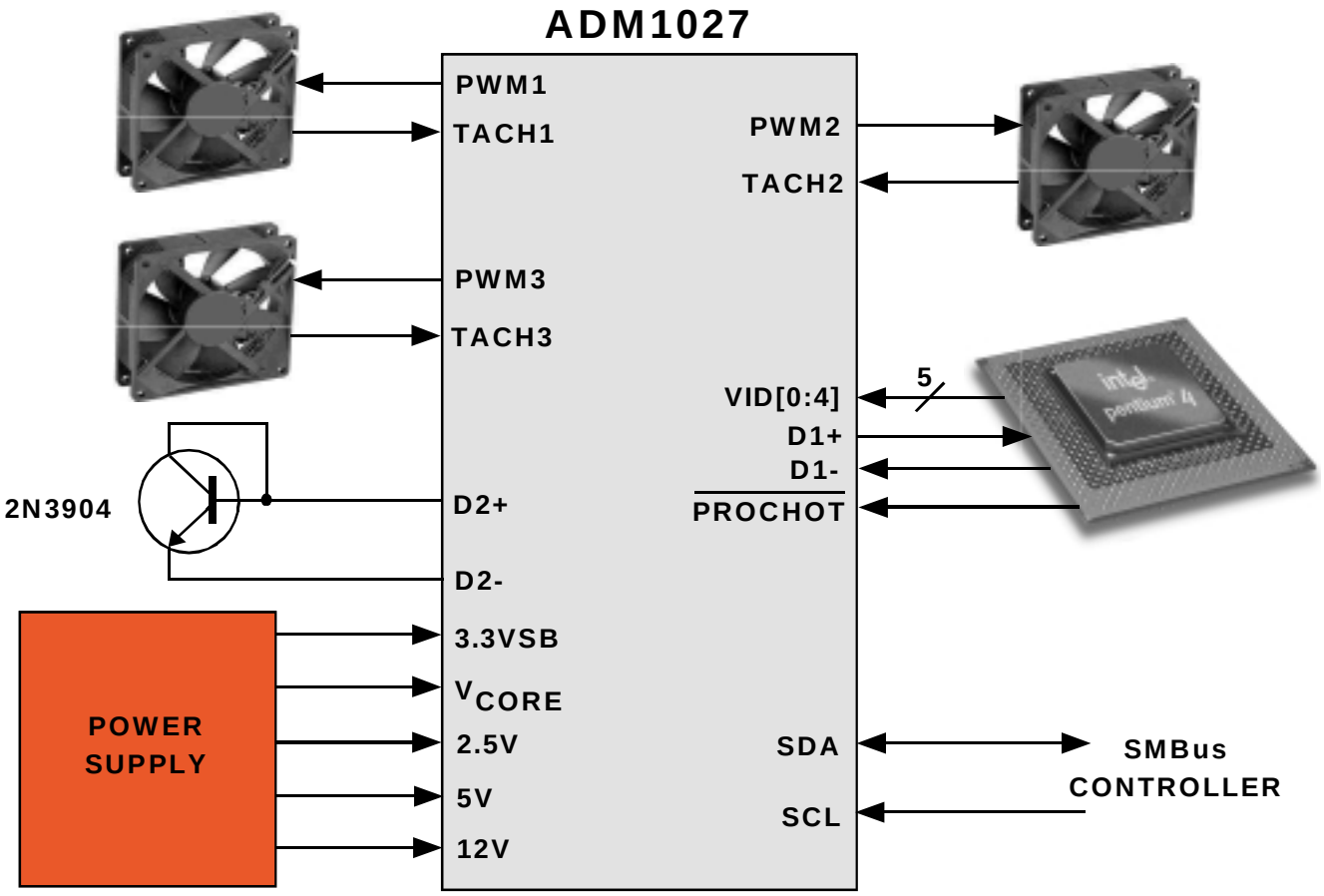


Figure 36. Monitoring $\overline{\text{PROCHOT}}$ and controlling 3 fans

PSEUDOCODE CONFIGURATION LISTING

Set bit 1 (PHOT) of Configuration Register 3 (0x78) = 1	;Configures pin 14 as $\overline{\text{PROCHOT}}$ input.
Set bit 2 (BOOST) of Configuration Register 3 = 1	;Runs fans 100% if $\overline{\text{PROCHOT}}$ gets asserted.
Write value to bits <5:0> (LIMT) of PROCHOT Mask Register (0x7A)	; ;Sets $\overline{\text{PROCHOT}}$ assertion time limit.
Configure Temperature High and Low Limits	;
Configure Voltage Measurement High and Low Limits	;
Configure Fan Tach Minimum Limits	;
Configure PWM Configuration Registers	;
Configure T_{MIN}, T_{RANGE} for Automatic Fan Speed Control	;
Set bit 0 (STRT) of Configuration Register 1 (0x40) = 1	;Starts ADM1027 Monitoring.
Set bit 1 (LOCK) of Configuration Register 1 (0x40) = 1	; Locks all lockable registers and prevents their contents from being modified.

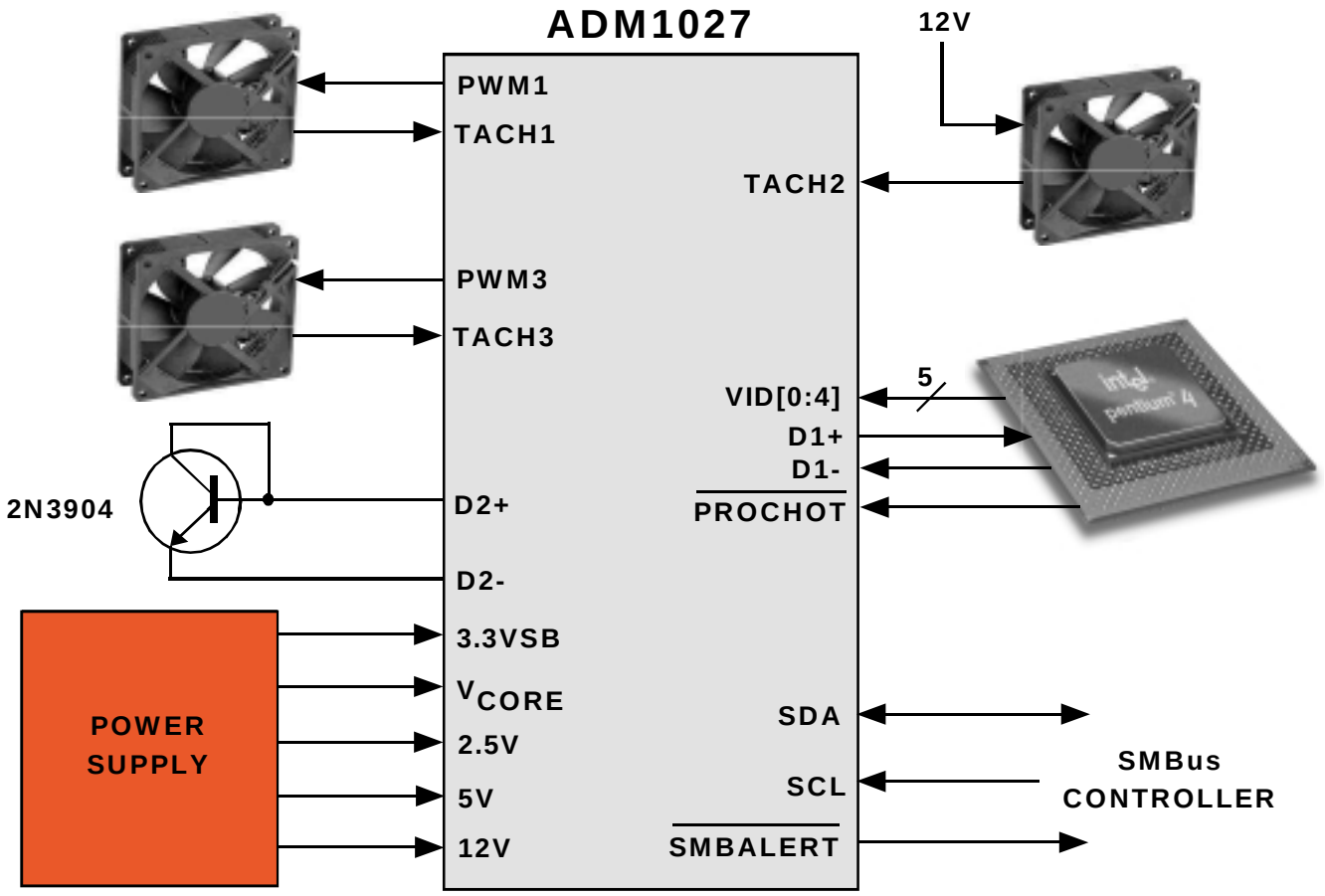


Figure 37. Monitoring $\overline{\text{PROCHOT}}$ and Generating $\overline{\text{SMBALERT}}$

PSEUDOCODE CONFIGURATION LISTING

Set bit 0 (ALERT) of Configuration Register 3 (0x78) = 1	;Configures pin 10 as the $\overline{\text{SMBALERT}}$ interrupt output.
Set bit 1 (PHOT) of Configuration Register 3 (0x78) = 1	;Configures pin 14 as $\overline{\text{PROCHOT}}$ input.
Set bit 2 (BOOST) of Configuration Register 3 = 1	;Runs fans 100% if $\overline{\text{PROCHOT}}$ gets asserted.
Set bit 5 (DC2) of Configuration Register 3 = 1	;Allows continuous tach measurements on TACH2.
Write value to bits <5:0> (LIMT) of PROCHOT Mask Register (0x7A)	; ;Sets $\overline{\text{PROCHOT}}$ assertion time limit.
Write to Interrupt Mask Register 1	;If you want to mask certain out-of-limit conditions
Write to Interrupt Mask Register 2	;from causing $\overline{\text{SMBALERT}}$s
Configure Temperature High and Low Limits	;
Configure Voltage Measurement High and Low Limits	;
Configure Fan Tach Minimum Limits	;
Configure PWM Configuration Registers	;
Configure T_{MIN}, T_{RANGE} for Automatic Fan Speed Control	;
Set bit 0 (STRT) of Configuration Register 1 (0x40) = 1	;Starts ADM1027 Monitoring.
Set bit 1 (LOCK) of Configuration Register 1 (0x40) = 1	; Locks all lockable registers and prevents their contents from being modified.

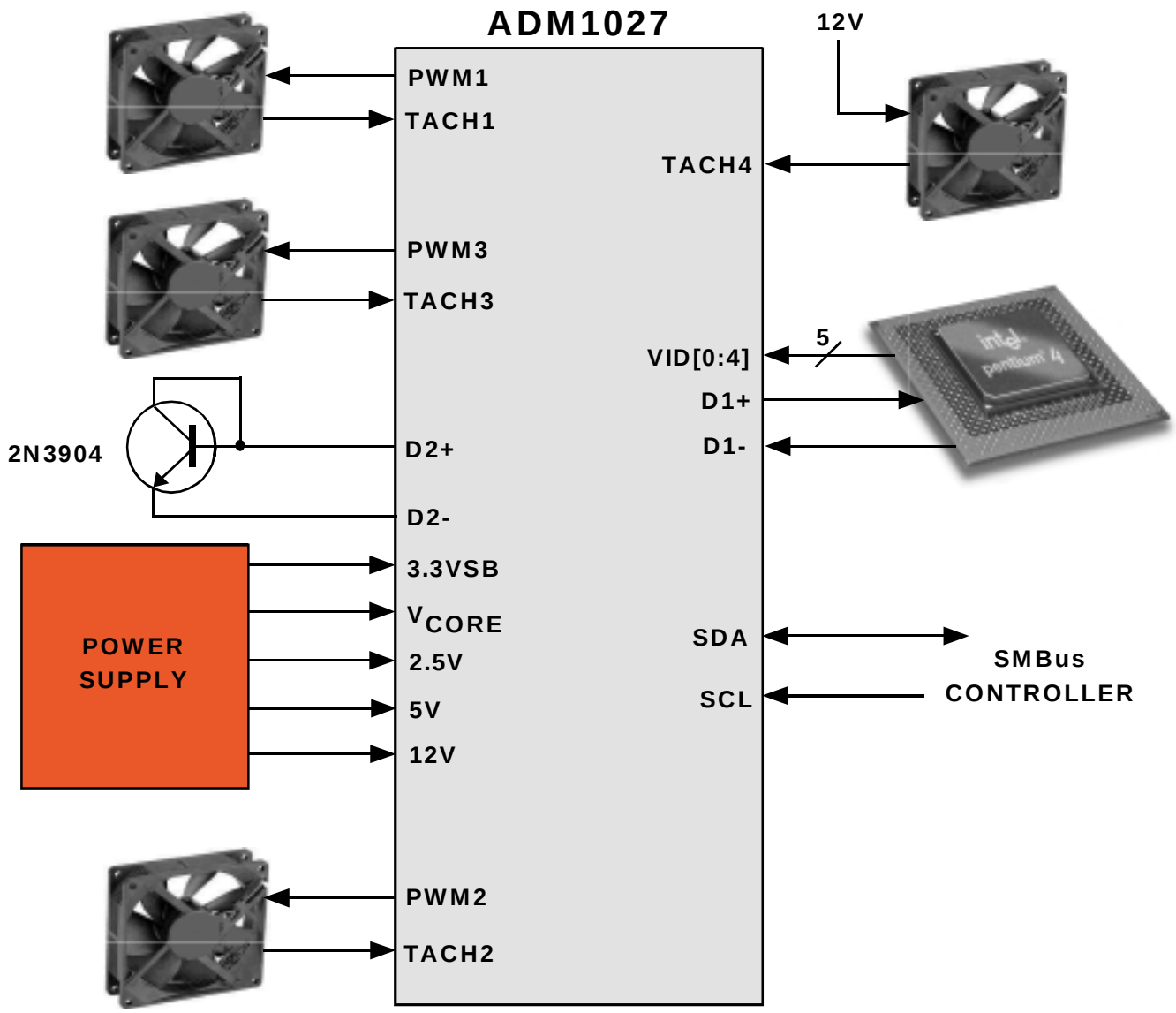


Figure 38. Controlling 3 fans, Measuring 4 fan speeds.

PSEUDOCODE CONFIGURATION LISTING

Set bit 7 (DC4) of Configuration Register 3 (0x78) = 1	;allows continuous tach measurements on TACH4.
Configure Temperature High and Low Limits	;
Configure Voltage Measurement High and Low Limits	;
Configure Fan Tach Minimum Limits	;
Configure PWM Configuration Registers	;
Configure T_{MIN}, T_{RANGE} for Automatic Fan Speed Control	;
Set bit 0 (STRT) of Configuration Register 1 (0x40) = 1	;Starts ADM1027 Monitoring.
Set bit 1 (LOCK) of Configuration Register 1 (0x40) = 1	; Locks all lockable registers and prevents their contents from being modified.

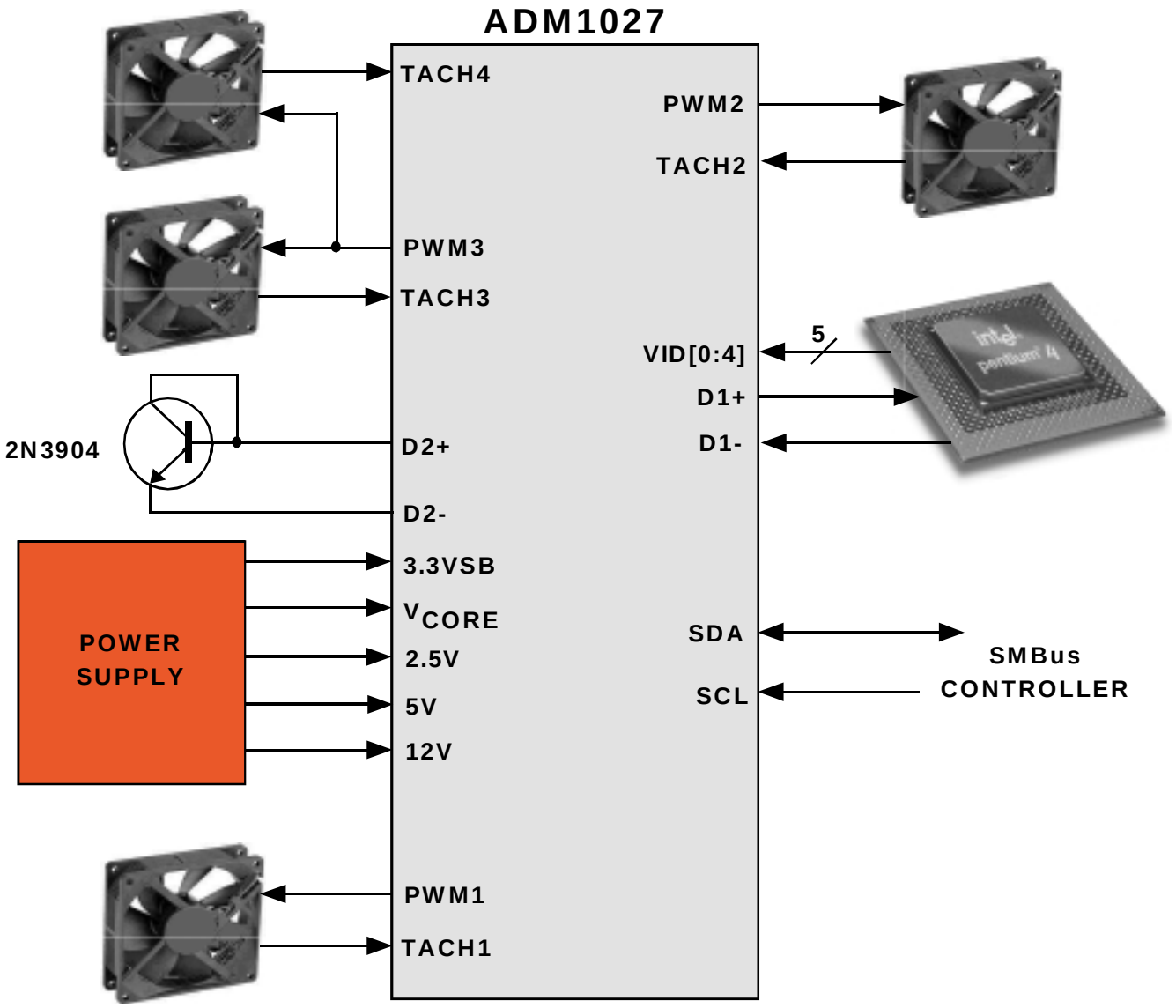


Figure 39. Controlling and measuring the speed of 4 fans

PSEUDOCODE CONFIGURATION LISTING

Configure Temperature High and Low Limits	;
Configure Voltage Measurement High and Low Limits	;
Configure Fan Tach Minimum Limits	;
Configure PWM Configuration Registers	;
Configure T_{MIN}, T_{RANGE} for Automatic Fan Speed Control	;
Set bit 0 (STRT) of Configuration Register 1 (0x40) = 1	;Starts ADM1027 Monitoring.
Set bit 1 (LOCK) of Configuration Register 1 (0x40) = 1	; Locks all lockable registers and prevents their contents from being modified.

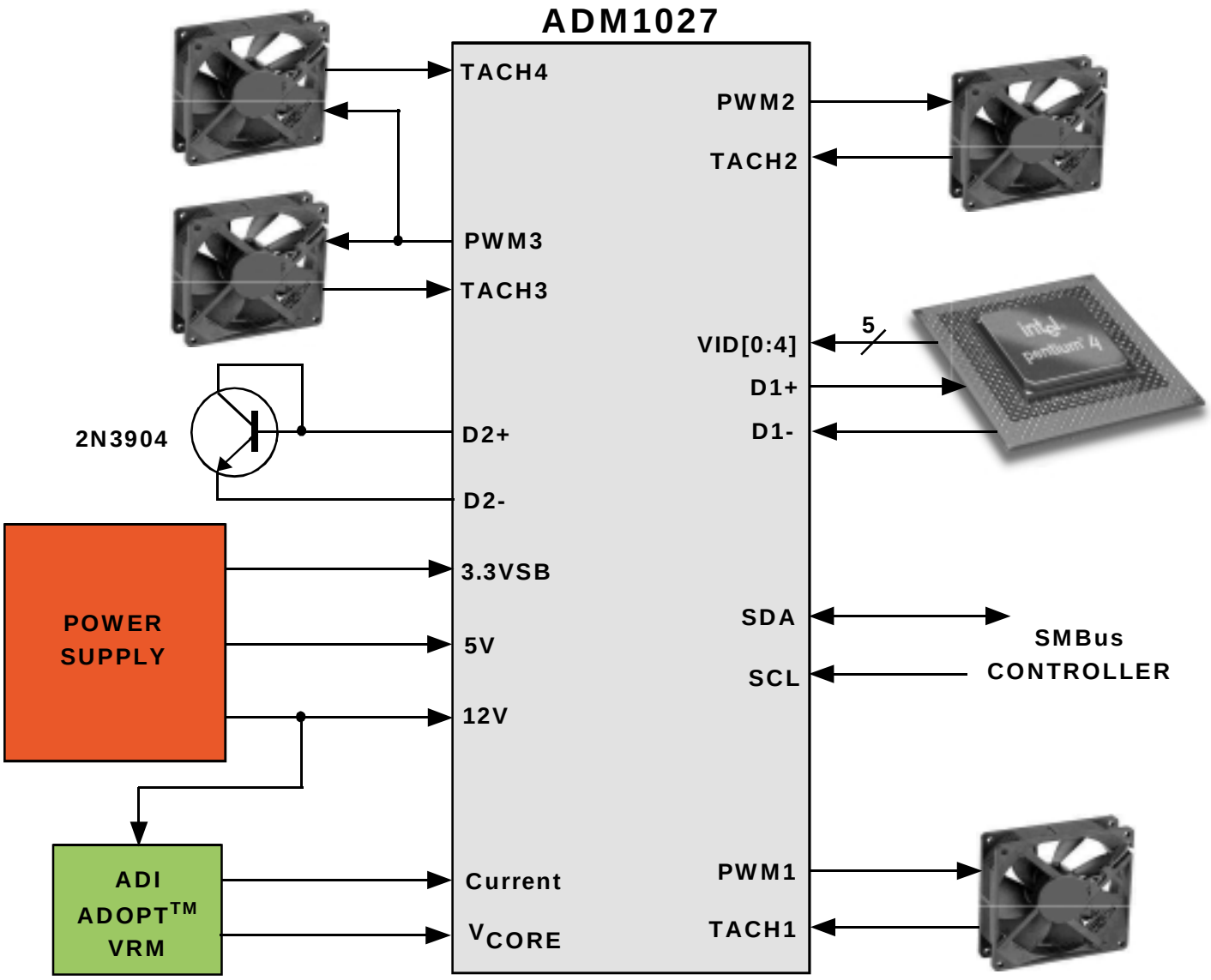


Figure 40. Monitoring and Displaying CPU Watts (V * I)

PSEUDOCODE CONFIGURATION LISTING

Set bit 4 (V*I) of Configuration Register 1 (0x40) = 1	;allows CPU current to be monitored using ADI ADOPT™ VRM Controller solution. By monitoring processor core voltage, CPU Watts can be calculated and displayed.
Configure Temperature High and Low Limits	;
Configure Voltage Measurement High and Low Limits	;
Configure Fan Tach Minimum Limits	;
Configure PWM Configuration Registers	;
Configure T_{MIN}, T_{RANGE} for Automatic Fan Speed Control	;
Set bit 0 (STRT) of Configuration Register 1 (0x40) = 1	;Starts ADM1027 Monitoring.
Set bit 1 (LOCK) of Configuration Register 1 (0x40) = 1	; Locks all lockable registers and prevents their contents from being modified.

Figure 41. Typical Application Schematic

TABLE 13. ADM1027 REGISTERS

Address	R/W	Description	Bit7	Bit 6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default	Lockable?
0x20	R	2.5V Reading	9	8	7	6	5	4	3	2	0x00	
0x21	R	V_{CCP} Reading	9	8	7	6	5	4	3	2	0x00	
0x22	R	V_{CC} Reading	9	8	7	6	5	4	3	2	0x00	
0x23	R	5V Reading	9	8	7	6	5	4	3	2	0x00	
0x24	R	12V Reading	9	8	7	6	5	4	3	2	0x00	
0x25	R	Remote 1 Temperature	9	8	7	6	5	4	3	2	0x00	
0x26	R	Local Temperature	9	8	7	6	5	4	3	2	0x00	
0x27	R	Remote 2 Temperature	9	8	7	6	5	4	3	2	0x00	
0x28	R	TACH1 Low Byte	7	6	5	4	3	2	1	0	0x00	
0x29	R	TACH1 High Byte	15	14	13	12	11	10	9	8	0x00	
0x2A	R	TACH2 Low Byte	7	6	5	4	3	2	1	0	0x00	
0x2B	R	TACH2 High Byte	15	14	13	12	11	10	9	8	0x00	
0x2C	R	TACH3 Low Byte	7	6	5	4	3	2	1	0	0x00	
0x2D	R	TACH3 High Byte	15	14	13	12	11	10	9	8	0x00	
0x2E	R	TACH4 Low Byte	7	6	5	4	3	2	1	0	0x00	
0x2F	R	TACH4 High Byte	15	14	13	12	11	10	9	8	0x00	
0x30	R/W	PWM1 Current Duty Cycle	7	6	5	4	3	2	1	0	0xFF	
0x31	R/W	PWM2 Current Duty Cycle	7	6	5	4	3	2	1	0	0xFF	
0x32	R/W	PWM3 Current Duty Cycle	7	6	5	4	3	2	1	0	0xFF	
0x3D	R	Device ID Register	7	6	5	4	3	2	1	0	0x27	
0x3E	R	Company ID Number	7	6	5	4	3	2	1	0	0x41	
0x3F	R	Revision Number	VER	VER	VER	VER	STP	STP	STP	STP	0x60	
0x40	R/W	Configuration Register 1	VCC	TODIS	RES	V*I	FSPD	RDY	LOCK	STRT	0x00	YES
0x41	R	Interrupt Status Register 1	OOL	R2T	LT	R1T	5V	V_{CC}	V_{CCP}	2.5V	0x00	
0x42	R	Interrupt Status Register 2	D2	D1	F4P	FAN3	FAN2	FAN1	OVT	12V	0x00	
0x43	R	VID Register	RES	RES	RES	VID4	VID3	VID2	VID1	VID0	0x??	
0x44	R/W	2.5V Low Limit	7	6	5	4	3	2	1	0	0x00	
0x45	R/W	2.5V High Limit	7	6	5	4	3	2	1	0	0xFF	
0x46	R/W	V_{CCP} Low Limit	7	6	5	4	3	2	1	0	0x00	
0x47	R/W	V_{CCP} High Limit	7	6	5	4	3	2	1	0	0xFF	
0x48	R/W	V_{CC} Low Limit	7	6	5	4	3	2	1	0	0x00	
0x49	R/W	V_{CC} High Limit	7	6	5	4	3	2	1	0	0xFF	
0x4A	R/W	5V Low Limit	7	6	5	4	3	2	1	0	0x00	
0x4B	R/W	5V High Limit	7	6	5	4	3	2	1	0	0xFF	
0x4C	R/W	12V Low Limit	7	6	5	4	3	2	1	0	0x00	
0x4D	R/W	12V High Limit	7	6	5	4	3	2	1	0	0xFF	
0x4E	R/W	Remote 1 Temp Low Limit	7	6	5	4	3	2	1	0	0x81	
0x4F	R/W	Remote 1 Temp High Limit	7	6	5	4	3	2	1	0	0x7F	
0x50	R/W	Local Temp Low Limit	7	6	5	4	3	2	1	0	0x81	

TABLE 13. ADM1027 REGISTERS (CONTINUED)

Address	R/W	Description	Bit7	Bit 6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default	Lockable?
0x51	R/W	Local Temp High Limit	7	6	5	4	3	2	1	0	0x7F	
0x52	R/W	Remote 2 Temp Low Limit	7	6	5	4	3	2	1	0	0x81	
0x53	R/W	Remote 2 Temp High Limit	7	6	5	4	3	2	1	0	0x7F	
0x54	R/W	TACH1 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	
0x55	R/W	TACH1 Minimum High Byte	15	14	13	12	11	10	9	8	0xFF	
0x56	R/W	TACH2 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	
0x57	R/W	TACH2 Minimum High Byte	15	14	13	12	11	10	9	8	0xFF	
0x58	R/W	TACH3 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	
0x59	R/W	TACH3 Minimum High Byte	15	14	13	12	11	10	9	8	0xFF	
0x5A	R/W	TACH4 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	
0x5B	R/W	TACH4 Minimum High Byte	15	14	13	12	11	10	9	8	0xFF	
0x5C	R/W	PWM1 Configuration Register	BHVR	BHVR	BHVR	INV	RES	SPIN	SPIN	SPIN	0x62	YES
0x5D	R/W	PWM2 Configuration Register	BHVR	BHVR	BHVR	INV	RES	SPIN	SPIN	SPIN	0x62	YES
0x5E	R/W	PWM3 Configuration Register	BHVR	BHVR	BHVR	INV	RES	SPIN	SPIN	SPIN	0x62	YES
0x5F	R/W	Remote 1 T_{RANGE}/PWM 1 Freq	RANGE	RANGE	RANGE	RANGE	RES	FREQ	FREQ	FREQ	0xC4	YES
0x60	R/W	Local T_{RANGE}/PWM 2 Freq	RANGE	RANGE	RANGE	RANGE	RES	FREQ	FREQ	FREQ	0xC4	YES
0x61	R/W	Remote 2 T_{RANGE}/PWM 3 Freq	RANGE	RANGE	RANGE	RANGE	RES	FREQ	FREQ	FREQ	0xC4	YES
0x62	R/W	Enhance Acoustics Reg 1	OFF3	OFF2	OFF1	RES	EN1	ACOU	ACOU	ACOU	0x00	YES
0x63	R/W	Enhance Acoustics Reg 2	EN2	ACOU2	ACOU2	ACOU2	EN3	ACOU3	ACOU3	ACOU3	0x00	YES
0x64	R/W	PWM1 Min Duty Cycle	7	6	5	4	3	2	1	0	0x80	YES
0x65	R/W	PWM2 Min Duty Cycle	7	6	5	4	3	2	1	0	0x80	YES
0x66	R/W	PWM3 Min Duty Cycle	7	6	5	4	3	2	1	0	0x80	YES
0x67	R/W	Remote 1 Temp T_{MIN}	7	6	5	4	3	2	1	0	0x5A	YES
0x68	R/W	Local Temp T_{MIN}	7	6	5	4	3	2	1	0	0x5A	YES
0x69	R/W	Remote 2 Temp T_{MIN}	7	6	5	4	3	2	1	0	0x5A	YES
0x6A	R/W	Remote 1 THERM Limit	7	6	5	4	3	2	1	0	0x64	YES
0x6B	R/W	Local THERM Limit	7	6	5	4	3	2	1	0	0x64	YES
0x6C	R/W	Remote 2 THERM Limit	7	6	5	4	3	2	1	0	0x64	YES
0x6D	R/W	Remote 1, Local Hysteresis	HYSR1	HYSR1	HYSR1	HYSR1	HYSL	HYSL	HYSL	HYSL	0x44	YES
0x6E	R/W	Remote 2 Temp Hysteresis	HYSR2	HYSR2	HYSR2	HYSR2	RES	RES	RES	RES	0x40	YES
0x6F	R/W	XOR Tree Test Enable	RES	RES	RES	RES	RES	RES	RES	XEN	0x00	YES
0x70	R/W	Remote 1 Temperature Offset	7	6	5	4	3	2	1	0	0x00	YES
0x71	R/W	Local Temperature Offset	7	6	5	4	3	2	1	0	0x00	YES
0x72	R/W	Remote 2 Temperature Offset	7	6	5	4	3	2	1	0	0x00	YES
0x73	R/W	Configuration Register 2	SHDN	CONV	ATTN	AVG	AIN4	AIN3	AIN2	AIN1	0x00	YES
0x74	R/W	Interrupt Mask 1 Register	OOL	R2T	LT	R1T	5V	V_{CC}	V_{CCP}	2.5V	0x00	
0x75	R/W	Interrupt Mask 2 Register	D2	D1	F4P	FAN3	FAN2	FAN1	OVT	12V	0x00	
0x76	R/W	Extended Resolution 1	5V	5V	Vcc	Vcc	Vccp	Vccp	2.5V	2.5V	0x00	
0x77	R/W	Extended Resolution 2	TDM2	TDM2	LTMP	LTMP	TDM1	TDM1	12V	12V	0x00	

TABLE 13. ADM1027 REGISTERS (CONTINUED)

Address	R/W	Description	Bit7	Bit 6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default	Lockable?
0x78	R/W	Configuration Register 3	DC4	DC3	DC2	DC1	FAST	BOOST	PHOT	ALERT	0x00	YES
0x79	R	PROCHOT Status	ASRT	NEG	TMR	TMR	TMR	TMR	TMR	TMR	0x00	
0x7A	R/W	PROCHOT Mask	ASRT	NEG	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT	0x00	
0x7B	R/W	Fan Pulses per Revolution	FAN4	FAN4	FAN3	FAN3	FAN2	FAN2	FAN1	FAN1	0x55	
0x7E	R	Test Register 1	DO NOT WRITE TO THESE REGISTERS								0x00	YES
0x7F	R	Test Register 2	DO NOT WRITE TO THESE REGISTERS								0x00	YES

TABLE 14. VOLTAGE READING REGISTERS (POWER ON DEFAULT = 00H)

Register Address	R/W	Description
0x20	Read Only	2.5V Reading (8 MSBs of reading)
0x21	Read Only	V_{CCP} Reading: holds processor core voltage measurement (8 MSBs of reading)
0x22	Read Only	V_{CC} Reading: measures V_{CC} through the V_{CC} pin (8 MSBs of reading)
0x23	Read Only	5V Reading (8 MSBs of reading)
0x24	Read Only	12V Reading(8 MSBs of reading)

If the extended resolution bits of these readings are also being read, the Extended Resolution registers (Reg. 0x76, 0x77) should be read first. Once the extended resolution register gets read, the associated MSB reading registers get frozen until read. Both the Extended Resolution Register and the MSB registers get frozen.

TABLE 15. TEMPERATURE READING REGISTERS (POWER ON DEFAULT = 00H)

Register Address	R/W	Description
0x25	Read Only	Remote 1 Temperature Reading* (8 MSBs of reading)
0x26	Read Only	Local Temperature Reading (8 MSBs of reading)
0x27	Read Only	Remote 2 Temperature Reading* (8 MSBs of reading)

These temperature readings are in 2's complement format.
*Note that a reading of 0x80 in a temperature reading register indicates a diode fault (open or short) on that channel. If the extended resolution bits of these readings are also being read, the Extended Resolution registers (Reg. 0x76, 0x77) should be read first. Once the extended resolution register gets read, all associated MSB reading registers get frozen until read. Both the Extended Resolution Register and the MSB registers get frozen.

TABLE 16. FAN TACHOMETER READING REGISTERS (POWER ON DEFAULT = 00H)

Register Address	R/W	Description
0x28	Read Only	TACH1 Low Byte
0x29	Read Only	TACH1 High Byte
0x2A	Read Only	TACH2 Low Byte
0x2B	Read Only	TACH2 High Byte
0x2C	Read Only	TACH3 Low Byte
0x2D	Read Only	TACH3 High Byte
0x2E	Read Only	TACH4 Low Byte
0x2F	Read Only	TACH4 High Byte

These registers count the number of 11.11us periods (based on an internal 90kHz clock) that occur between a number of consecutive fan tach pulses (default = 2). The number of tach pulses used to count can be changed using the Fan Pulses Per Revolution Register (Reg. 0x7B). This allows the fan speed to be accurately measured. Since a valid Fan Tachometer reading requires that two bytes are read, the Low Byte MUST be read first. Both the Low and High Bytes are then frozen until read. At power-on, these registers contain 0x0000 until such time as the first valid fan tach measurement is read in to these registers. This prevents false interrupts from occurring while the fans are spinning up.

A count of 0xFFFF indicates that a fan is:

1. **Stalled or Blocked** (object jamming the fan)
2. **Failed** (internal circuitry destroyed)
3. **Not Populated** (the ADM1027 expects to see a fan connected to each TACH. If a fan is not connected to that TACH, it's TACH Minimum High and Low Byte should be set to 0xFFFF)
4. **Alternate Function**, e.g. TACH4 reconfigured as $\overline{\text{PROCHOT}}$ input
5. **2-wire instead of 3-wire fan**

TABLE 17. CURRENT PWM DUTY CYCLE REGISTERS (POWER-ON DEFAULT = FFH)

Register Address	R/W	Description
0x30	Read/Write	PWM1 Current Duty Cycle (0% to 100% duty cycle = 0x00 to 0xFF)
0x31	Read/Write	PWM2 Current Duty Cycle (0% to 100% duty cycle = 0x00 to 0xFF)
0x32	Read/Write	PWM3 Current Duty Cycle (0% to 100% duty cycle = 0x00 to 0xFF)

These registers reflect the PWM duty cycle driving each fan at any given time. When in Automatic Fan Speed Control Mode, the ADM1027 reports the PWM duty cycles back through these registers. The PWM duty cycle values will vary according to temperature in Automatic Fan Speed Control Mode. During fan startup, these registers report back 0x00. In Software Mode, the PWM duty cycle outputs can be set to any duty cycle value by writing to these registers.

TABLE 18. REGISTER 40H - CONFIGURATION REGISTER 1 (POWER-ON DEFAULT = 00H)

Bit	Name	R/W	Description
<0>	STRT	Read/Write	Logic 1 enables monitoring and PWM control outputs based on the limit settings programmed. Logic 0 disables monitoring and PWM control based on the default power-up limit settings. Note that the limit values programmed are preserved even if a logic 0 is written to this bit and the default settings are enabled. This bit becomes read-only and cannot be changed once bit 1 (LOCK bit) has been written. All limit registers should be programmed by BIOS before setting this bit to 1. (Lockable)
<1>	LOCK	Write Once	Logic 1 locks all limit values to their current settings. Once this bit is set, all lockable registers become read only and cannot be modified, until the ADM1027 is powered down and powered up again. This prevents rogue programs such as viruses from modifying critical system limit settings. (Lockable)
<2>	RDY	Read Only	This bit gets set to 1 by the ADM1027 to indicate that the device is fully powered-up and ready to begin systems monitoring.
<3>	FSPD	Read/Write	When set to 1, this runs all fans at full-speed. Power-on default = 0. This bit does not get locked at any time.
<4>	V*I	Read/Write	BIOS should set this bit to a 1 when the ADM1027 is configured to measure current from an ADI ADOPT™ VRM controller and measure the CPU's core voltage. This will allow monitoring software to display CPU Watts usage. (Lockable)
<5>	RES	Read Only	Reserved
<6>	TODIS	Read/Write	When this bit is set to 1, the SMBus Timeout feature is disabled. This allows the ADM1027 to be used with SMBus controllers that cannot handle SMBus timeouts. (Lockable)
<7>	VCC	Read/Write	When this bit is set to 1, the ADM1027 rescales its V_{CC} pin to measure a 5V supply. If this bit is 0, the ADM1027 measures V_{CC} as a 3.3V supply. (Lockable)

TABLE 19. REGISTER 41H- INTERRUPT STATUS REGISTER 1 (POWER ON DEFAULT = 00H)

Bit	Name	Read/Write	Description
<0>	2.5V	Read Only	A one indicates the 2.5V High or Low limit has been exceeded. This bit gets cleared on a read of the Status Register only if the error condition has subsided.
<1>	V_{CCP}	Read Only	A one indicates the V_{CCP} High or Low limit has been exceeded. This bit gets cleared on a read of the Status Register only if the error condition has subsided.
<2>	V_{CC}	Read Only	A one indicates the V_{CC} High or Low limit has been exceeded. This bit gets cleared on a read of the Status Register only if the error condition has subsided.
<3>	5V	Read Only	A one indicates the +5V High or Low limit has been exceeded. This bit gets cleared on a read of the Status Register only if the error condition has subsided.
<4>	R1T	Read Only	A one indicates the Remote 1 Low or High Temp limit has been exceeded. This bit gets cleared on a read of the Status Register only if the error condition has subsided.
<5>	LT	Read Only	A one indicates the Local Low or High Temp limit has been exceeded. This bit gets cleared on a read of the Status Register only if the error condition has subsided.
<6>	R2T	Read Only	A one indicates the Remote 2 Low or High Temp limit has been exceeded. This bit gets cleared on a read of the Status Register only if the error condition has subsided.
<7>	OOL	Read Only	A one indicates that an Out-Of-Limit event has been latched in Status Register 2. This bit is a logical OR of all status bits in Status Register 2. Software can test this bit in isolation to determine whether any of the voltage, temperature or fan speed readings represented by Status Register 2 are out-of-limit. This saves the need to read Status Register 2 every interrupt or polling cycle.

TABLE 20. REGISTER 42H - INTERRUPT STATUS REGISTER 2 (POWER ON DEFAULT = 00H)

Bit	Name	Read/Write	Description
<0>	12V	Read Only	A one indicates the +12V High or Low limit has been exceeded. This bit gets cleared on a read of the Status Register only if the error condition has subsided.
<1>	OVT	Read Only	A one indicates that one of the THERM OVer-Temperature limits has been exceeded. This bit gets cleared on a read of the Status Register when the temperature drops below THERM - T_{HYST}.
<2>	FAN1	Read Only	A one indicates that Fan 1 has dropped below minimum speed or has stalled. This bit does NOT get set when the PWM 1 output is off.
<3>	FAN2	Read Only	A one indicates that Fan 2 has dropped below minimum speed or has stalled. This bit does NOT get set when the PWM 2 output is off.
<4>	FAN3	Read Only	A one indicates that Fan 3 has dropped below minimum speed or has stalled. This bit does NOT get set when the PWM 3 output is off.
<5>	F4P	Read Only	A one indicates that Fan 4 has dropped below minimum speed or has stalled. This bit does NOT get set when the PWM 3 output is off.
		Read Only	If pin 14 is configured as the $\overline{\text{PROCHOT}}$ input, then this bit gets set when the $\overline{\text{PROCHOT}}$ assertion time exceeds the limit programmed in the $\overline{\text{PROCHOT}}$ Mask Register (bits <5:0> Reg. 0x7A)
<6>	D1	Read Only	A one indicates either an open or short circuit on the Thermal Diode 1 inputs.
<7>	D2	Read Only	A one indicates either an open or short circuit on the Thermal Diode 2 inputs.

TABLE 21. REGISTER 43H - VID REGISTER (POWER ON DEFAULT = ??)

Bit	Name	R/W	Description
<4:0>	VID[4:0]	Read Only	The VID[4:0] inputs from the CPU to indicate the expected processor core voltage. On power-up these bits reflect the state of the VID pins, even if monitoring is not enabled.
<7:5>	RES	Read Only	Reserved

TABLE 22. VOLTAGE LIMIT REGISTERS

Register Address	R/W	Description	Power-on default
0x44	Read/Write	2.5V Low Limit	0x00
0x45	Read/Write	2.5V High Limit	0xFF
0x46	Read/Write	V_{CCP} Low Limit	0x00
0x47	Read/Write	V_{CCP} High Limit	0xFF
0x48	Read/Write	V_{CC} Low Limit	0x00
0x49	Read/Write	V_{CC} High Limit	0xFF
0x4A	Read/Write	5V Low Limit	0x00
0x4B	Read/Write	5V High Limit	0xFF
0x4C	Read/Write	12V Low Limit	0x00
0x4D	Read/Write	12V High Limit	0xFF

Setting the Configuration Register 1 Lock bit has no effect on these registers.

High Limits: An interrupt is generated when a value exceeds its high limit (> comparison).
Low Limits: An interrupt is generated when a value is equal to or below its low limit (< = comparison).

TABLE 23. TEMPERATURE LIMIT REGISTERS

Register Address	R/W	Description	Power-on default
0x4E	Read/Write	Remote 1 Temp Low Limit	0x81
0x4F	Read/Write	Remote 1 Temp High Limit	0x7F
0x50	Read/Write	Local Temp Low Limit	0x81
0x51	Read/Write	Local Temp High Limit	0x7F
0x52	Read/Write	Remote 2 Temp Low Limit	0x81
0x53	Read/Write	Remote 2 Temp High Limit	0x7F

Exceeding any of these temperature limits by 1°C will cause the appropriate status bit to be set in the Interrupt Status Register. Setting the Configuration Register 1 Lock bit has no effect on these registers.

High Limits: An interrupt is generated when a value exceeds its high limit (> comparison).
Low Limits: An interrupt is generated when a value is equal to or below its low limit (< = comparison).

TABLE 24. FAN TACHOMETER LIMIT REGISTERS

Register Address	R/W	Description	Power-on default
0x54	Read / Write	TACH 1 Minimum Low Byte	0xFF
0x55	Read / Write	TACH 1 Minimum High Byte	0xFF
0x56	Read / Write	TACH 2 Minimum Low Byte	0xFF
0x57	Read / Write	TACH 2 Minimum High Byte	0xFF
0x58	Read / Write	TACH 3 Minimum Low Byte	0xFF
0x59	Read / Write	TACH 3 Minimum High Byte	0xFF
0x5A	Read / Write	TACH 4 Minimum Low Byte	0xFF
0x5B	Read / Write	TACH 4 Minimum High Byte	0xFF

Exceeding any of the TACH limit registers by 1 indicates that the fan is running too slowly or has stalled. The appropriate status bit will be set in Interrupt Status Register 2 to indicate the fan failure. Setting the Configuration Register 1 Lock bit has no effect on these registers.

TABLE 25. PWM CONFIGURATION REGISTERS

Register Address	R/W	Description	Power-on default
0x5C	Read/Write	PWM1 Configuration	0x62
0x5D	Read/Write	PWM2 Configuration	0x62
0x5E	Read/Write	PWM3 Configuration	0x62

Bit	Name	Read/Write	Description
<2:0>	SPIN (Fan Startup Timeout)	Read/Write	These bits control the startup timeout for PWMx. The PWM output stays high until two valid tach rising edges are seen from the fan. If there is not a valid tach signal during the fan tach measurement directly after the Fan Startup Timeout period, then the tach measurement will read 0xFFFF and Status Register 2 reflects the Fan Fault. If the TACH Minimum High and Low Byte contains 0xFFFF or 0x0000, then the Status Register 2 bit will not get set, even if the fan has not started. 000 = No startup timeout 001 = 100ms 010 = 250ms (default) 011 = 400ms 100 = 667ms 101 = 1 sec 110 = 2 secs 111 = 4 secs
<3>	RES	Read Only	Reserved
<4>	INV	Read/Write	This bit inverts the PWM output. The default is 0, which corresponds to a logic high output for 100% duty cycle. Setting this bit to 1, inverts the PWM, so 100% duty cycle corresponds to a logic low output.
<7:5>	BHVR	Read/Write	These bits assign each fan to a particular temperature sensor for localized cooling. 000 = Remote 1 Temp controls PWMx (Automatic Fan Speed Control Mode) 001 = Local Temp controls PWMx (Automatic Fan Speed Control Mode) 010 = Remote 2 Temp controls PWMx (Automatic Fan Speed Control Mode) 011 = PWMx runs full-speed (default) 100 = PWMx disabled 101 = Fastest Speed Calculated by Local and Remote 2 Temp controls PWMx 110 = Fastest Speed Calculated by all 3 Temperatures controls PWMx 111 = Manual Mode. PWM Duty cycle Registers (Reg 0x30-0x32) become writable.

* These registers become Read Only when the Configuration Register 1 Lock bit is set to 1. Any subsequent attempts to write to these registers will fail.

TABLE 26. TEMP T_{RANGE} / PWM FREQUENCY REGISTERS

Register Address	R/W	Description	Power-on default
0x5F	Read/Write	Remote 1 T_{RANGE}/PWM 1 Frequency	0xC4
0x60	Read/Write	Local Temp T_{RANGE}/PWM 2 Frequency	0xC4
0x61	Read/Write	Remote 2 T_{RANGE}/PWM 3 Frequency	0xC4

Bit	Name	Read/Write	Description
<2:0>	FREQ	Read/Write	These bits control the PWMx frequency. 000 = 11.0Hz 001 = 14.7Hz 010 = 22.1Hz 011 = 29.4Hz 100 = 35.3Hz (default) 101 = 44.1Hz 110 = 58.8Hz 111 = 88.2Hz
<3>	RES	Read/Write	Reserved
<7:4>	RANGE	Read/Write	These bits determine the temperature range value used to calculate PWM duty cycle in the Automatic Fan Speed Control algorithm. 0000 = 2°C 0001 = 2.5°C 0010 = 3.33°C 0011 = 4°C 0100 = 5°C 0101 = 6.67°C 0110 = 8°C 0111 = 10°C 1000 = 13.33°C 1001 = 16°C 1010 = 20°C 1011 = 26.67°C 1100 = 32°C (default) 1101 = 40°C 1110 = 53.33°C 1111 = 80°C

*These registers become Read Only when the Configuration Register 1 Lock bit is set. Any further attempts to write to these registers shall have no effect.

TABLE 27. REGISTER 62H - ENHANCE ACOUSTICS REG 1 (POWER-ON DEFAULT = 00H)

Bit	Name	R/W	Description
<2:0>	ACOU	Read/Write	These bits select the ramp rate or timeslot change applied to the PWM1 output. Instead of PWM1 jumping instantaneously to its newly calculated speed, PWM1 will ramp gracefully at the rate determined by these bits. This feature enhances the acoustics of the fan being driven by the PWM1 output. **Time slot increase — Time for 33% to 100%** 000 = 1 — 35 secs 001 = 2 — 17.6 secs 010 = 3 — 11.8 secs 011 = 5 — 7 secs 100 = 8 — 4.4 secs 101 = 12 — 3 secs 110 = 24 — 1.6 secs 111 = 48 — 0.8 secs
<3>	EN1	Read/Write	When this bit is 1, Acoustic Enhancement is enabled on PWM1 output.
<4>	RES	Read Only	Reserved
<5>	OFF1	Read/Write	When the ADM1027 is in Automatic Fan Speed Control Mode, this bit defines whether PWM 1 is off (0% duty cycle) or at PWM 1 Minimum Duty Cycle when the controlling temperature is below its T_{MIN} value. 0 = 0% duty cycle below T_{MIN} - Hysteresis 1 = PWM 1 Minimum Duty Cycle below T_{MIN}
<6>	OFF2	Read/Write	When the ADM1027 is in Automatic Fan Speed Control Mode, this bit defines whether PWM 2 is off (0% duty cycle) or at PWM 2 Minimum Duty Cycle when the controlling temperature is below its T_{MIN} value. 0 = 0% duty cycle below T_{MIN} - Hysteresis 1 = PWM 2 Minimum Duty Cycle below T_{MIN}
<7>	OFF3	Read/Write	When the ADM1027 is in Automatic Fan Speed Control Mode, this bit defines whether PWM 3 is off (0% duty cycle) or at PWM 3 Minimum Duty Cycle when the controlling temperature is below its T_{MIN} value. 0 = 0% duty cycle below T_{MIN} - Hysteresis 1 = PWM 3 Minimum Duty Cycle below T_{MIN}

* This register becomes Read Only when the Configuration Register 1 Lock bit is set to 1. Any further attempts to write to this register will have no effect.

TABLE 28. REGISTER 63H - ENHANCE ACOUSTICS REG 2 (POWER-ON DEFAULT = 00H)

Bit	Name	R/W	Description
<2:0>	ACOU3	Read/Write	These bits select the ramp rate or timeslot change applied to the PWM3 output. Instead of PWM3 jumping instantaneously to its newly calculated speed, PWM3 will ramp gracefully at the rate determined by these bits. This effect enhances the acoustics of the fan being driven by the PWM3 output. **Time slot increase** — **Time for 33% to 100%** 000 = 1 — 35 secs 001 = 2 — 17.6 secs 010 = 3 — 11.8 secs 011 = 5 — 7 secs 100 = 8 — 4.4 secs 101 = 12 — 3 secs 110 = 24 — 1.6 secs 111 = 48 — 0.8 secs
<3>	EN3	Read/Write	When this bit is 1, Acoustic Enhancement is enabled on PWM3 output.
<6:4>	ACOU2	Read/Write	These bits select the ramp rate or timeslot change applied to the PWM2 output. Instead of PWM2 jumping instantaneously to its newly calculated speed, PWM2 will ramp gracefully at the rate determined by these bits. This effect enhances the acoustics of the fans being driven by the PWM2 output. **Time slot increase** — **Time for 33% to 100%** 000 = 1 — 35 secs 001 = 2 — 17.6 secs 010 = 3 — 11.8 secs 011 = 5 — 7 secs 100 = 8 — 4.4 secs 101 = 12 — 3 secs 110 = 24 — 1.6 secs 111 = 48 — 0.8 secs
<7>	EN2	Read/Write	When this bit is 1, Acoustic Enhancement is enabled on PWM2 output.

* This register becomes Read Only when the Configuration Register 1 Lock bit is set to 1. Any further attempts to write to this register will have no effect.

TABLE 29. PWM MIN DUTY CYCLE REGISTERS

Register Address	R/W	Description	Power-on default
0x64	Read/Write	PWM1 Min Duty Cycle	0x80 (50% duty cycle)
0x65	Read/Write	PWM2 Min Duty Cycle	0x80 (50% duty cycle)
0x66	Read/Write	PWM3 Min Duty Cycle	0x80 (50% duty cycle)

Bit	Name	Read/Write	Description
<7:0>	PWM Duty Cycle	Read / Write	These bits define the minimum PWM duty cycle for PWMx. 0x00 = 0% duty cycle (Fan off) | 0x40 = 25% duty cycle | 0x80 = 50% duty cycle | 0xFF = 100% duty cycle (Fan full-speed)

* These registers become Read Only when the ADM1027 is in Automatic Fan Speed Control Mode.

TABLE 30. TMIN REGISTERS

Register Address	R/W	Description	Power-on default
0x67	Read/Write	Remote 1 Temp T_{MIN}	0x5A (90°C)
0x68	Read/Write	Local Temp T_{MIN}	0x5A (90°C)
0x69	Read/Write	Remote 2 Temp T_{MIN}	0x5A (90°C)

These are the T_{MIN} registers for each temperature channel. When the temperature measured exceeds T_{MIN}, the appropriate fan will run at minimum speed and increase with temperature according to T_{RANGE}. * These registers become Read Only when the Configuration Register 1 Lock bit is set. Any further attempts to write to these registers shall have no effect.

TABLE 31. THERM LIMIT REGISTERS

Register Address	R/W	Description	Power-on default
0x6A	Read/Write	Remote 1 THERM limit	0x64 (100°C)
0x6B	Read/Write	Local THERM limit	0x64 (100°C)
0x6C	Read/Write	Remote 2 THERM limit	0x64 (100°C)

If any temperature measured exceeds its THERM Limit, all PWM outputs will drive their fans at 100% duty cycle. This is a failsafe mechanism incorporated to cool the system in the event of a critical overtemperature. It also ensures some level of cooling in the event that software or hardware locks up. If set to 0x80, this feature is disabled. The PWM output will remain asserted until the temperature drops below THERM limit - hysteresis.

* These registers become Read Only when the Configuration Register 1 Lock bit is set to 1. Any further attempts to write to these registers will have no effect.

TABLE 32. TEMPERATURE HYSTERESIS REGISTERS

Register Address	R/W	Description	Power-on default
0x6D	Read/Write	Remote 1, Local Temp Hysteresis	0x44
0x6E	Read/Write	Remote 2 Temp Hysteresis	0x40

Each nibble controls the amount of temperature hysteresis applied to a particular temperature channel. Once the temperature for that channel falls below its T_{MIN} value, the fan will remain running at minimum PWM duty cycle, until the temperature = T_{MIN} - Hysteresis. Up to 15°C of hysteresis may be assigned to any temperature channel. The hysteresis value chosen will also apply to that temperature channel if its THERM limit is exceeded. The PWM output being controlled will go to 100% if the THERM limit is exceeded and will remain at 100% until the temperature drops below THERM - hysteresis. For acoustic reasons, it is recommended that the hysteresis value not be programmed less than 4°C. Setting the hysteresis value lower than 4°C will cause the fan to switch on and off regularly when the temperature is close to T_{MIN}.

* These registers become Read Only when the Configuration Register 1 Lock bit is set to 1. Any further attempts to write to these registers will have no effect.

TABLE 33. XOR TREE TEST ENABLE

Register Address	R/W	Description	Power-on default
0x6F	Read/Write	XOR Tree Test Enable Register	0x00
<0>	XEN	If the XEN bit is set to 1, the device enters the XOR Tree Test Mode. Clearing the bit removes the device from the XOR Test Mode.	
<7:1>	Reserved	Unused. Do not write to these bits.	

* This register becomes Read Only when the Configuration Register 1 Lock bit is set to 1. Any further attempts to write to this register will have no effect.

TABLE 34. REMOTE 1 TEMPERATURE OFFSET

Register Address	R/W	Description	Power-on default
0x70	Read/Write	Remote 1 Temperature Offset	0x00
<7:0>	Read/Write	Allows a 2's complement offset value to be automatically added to or subtracted from the Remote 1 Temperature reading. This is to compensate for any inherent system offsets such as PCB trace resistance.	

* This register becomes Read Only when the Configuration Register 1 Lock bit is set to 1. Any further attempts to write to this register will have no effect.

TABLE 35. LOCAL TEMPERATURE OFFSET

Register Address	R/W	Description	Power-on default
0x71	Read/Write	Local Temperature Offset	0x00
<7:0>	Read/Write	Allows a 2's complement offset value to be automatically added to or subtracted from the Local Temperature reading.	

* This register becomes Read Only when the Configuration Register 1 Lock bit is set to 1. Any further attempts to write to this register will have no effect.

TABLE 36. REMOTE 2 TEMPERATURE OFFSET

Register Address	R/W	Description	Power-on default
0x72	Read/Write	Remote 2 Temperature Offset	0x00
<7:0>	Read/Write	Allows a 2's complement offset value to be automatically added to or subtracted from the Remote 2 Temperature reading. This is to compensate for any inherent system offsets such as PCB trace resistance.	

* This register becomes Read Only when the Configuration Register 1 Lock bit is set to 1. Any further attempts to write to this register will have no effect.

TABLE 37. REGISTER 73H - CONFIGURATION REGISTER 2 (POWER-ON DEFAULT = 00H)

Bit	Name	R/W	Description
0	AIN1	Read/Write	When this bit is 0, it allows the speed of 3-wire fans to be measured using the TACH output from the fan. If set to 1, pin 11 is reconfigured to measure the speed of 2-wire fans using an external sensing resistor and coupling capacitor.
1	AIN2	Read/Write	When this bit is 0, it allows the speed of 3-wire fans to be measured using the TACH output from the fan. If set to 1, pin 12 is reconfigured to measure the speed of 2-wire fans using an external sensing resistor and coupling capacitor.
2	AIN3	Read/Write	When this bit is 0, it allows the speed of 3-wire fans to be measured using the TACH output from the fan. If set to 1, pin 9 is reconfigured to measure the speed of 2-wire fans using an external sensing resistor and coupling capacitor.
3	AIN4	Read/Write	When this bit is 0, it allows the speed of 3-wire fans to be measured using the TACH output from the fan. If set to 1, pin 14 is reconfigured to measure the speed of 2-wire fans using an external sensing resistor and coupling capacitor.
4	AVG	Read/Write	When this bit is set to 1, Averaging on the temperature and voltage measurements is turned off. This allows measurements on each channel to be made much faster.
5	ATTN	Read/Write	When this bit is set to 1, the ADM1027 removes the attenuators from the 2.5V, Vccp, 5V and 12V inputs. This allows the user to use the inputs for other functions such as connecting up external sensors.
6	CONV	Read/Write	When this bit is set to 1, the ADM1027 is put in to a single channel ADC Conversion Mode. In this mode, the ADM1027 can be made to read from one input only, e.g. Remote 1 Temperature. It is also possible to Start ADC Conversions using an external clock. This mode could be useful if, for example, you wanted to characterize/profile CPU temperature quickly. The appropriate ADC Channel is selected by writing to bits <7:5> of TACH1 Minimum High Byte Register (0x55). **Bits <7:5> Reg 0x55 — Channel Selected** 000 — 2.5V 001 — Vccp 010 — Vcc (3.3V) 011 — 5V 100 — 12V 101 — Remote 1 Temp 110 — Local Temp 111 — Remote 2 Temp
7	SHDN	Read/Write	When this bit is set to 1, ADM1027 goes in to Shutdown Mode. All PWM outputs assert low (or high depending on state of INV bit) to switch off all fans. The PWM Current Duty Cycle registers read 0x00 to indicate that the fans are not being driven.

* This register becomes Read Only when the Configuration Register 1 Lock bit is set to 1. Any further attempts to write to this register will have no effect.

TABLE 38. REGISTER 74H- INTERRUPT MASK REGISTER 1 (POWER ON DEFAULT <7:0> = 00H)

Bit	Name	Read/Write	Description
0	2.5V	Read/Write	A one masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the 2.5V channel.
1	V_{CCP}	Read/Write	A one masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the V_{CCP} channel.
2	V_{CC}	Read/Write	A one masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the V_{CC} channel.
3	5V	Read/Write	A one masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the 5V channel.
4	R1T	Read/Write	A one masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the Remote 1 Temperature channel.
5	LT	Read/Write	A one masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the Local Temperature channel.
6	R2T	Read/Write	A one masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the Remote 2 Temperature channel.
7	OOL	Read Only	A one masks $\overline{\text{SMBALERT}}$ for any out-of-limit condition in Status Register 2.

TABLE 39. REGISTER 75H - INTERRUPT MASK REGISTER 2 (POWER ON DEFAULT <7:0> = 00H)

Bit	Name	Read/Write	Description
0	12V	Read/Write	A one masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the 12V channel.
1	OVT	Read Only	A one masks $\overline{\text{SMBALERT}}$ for over-temperature $\overline{\text{THERM}}$ conditions.
2	FAN1	Read/Write	A one masks $\overline{\text{SMBALERT}}$ for a Fan 1 Fault.
3	FAN2	Read/Write	A one masks $\overline{\text{SMBALERT}}$ for a Fan 2 Fault.
4	FAN3	Read/Write	A one masks $\overline{\text{SMBALERT}}$ for a Fan 3 Fault.
5	F4P	Read/Write	A one masks $\overline{\text{SMBALERT}}$ for a Fan 4 Fault. If the TACH4 pin is being used as the $\overline{\text{PROCHOT}}$ input, this bit masks $\overline{\text{SMBALERT}}$ for a $\overline{\text{PROCHOT}}$ event.
6	D1	Read/Write	A one masks $\overline{\text{SMBALERT}}$ for a diode open or short on Remote 1 channel.
7	D2	Read/Write	A one masks $\overline{\text{SMBALERT}}$ for a diode open or short on Remote 2 channel.

TABLE 40. EXTENDED RESOLUTION REGISTER 1

Bit	Name	Read/Write	Description
<1:0>	2.5V	Read Only	2.5V LSBs. Holds the 2 LSBs of the 10-bit 2.5V measurement.
<3:2>	V_{CCP}	Read Only	V_{CCP} LSBs. Holds the 2 LSBs of the 10-bit V_{CCP} measurement.
<5:4>	V_{CC}	Read Only	V_{CC} LSBs. Holds the 2 LSBs of the 10-bit V_{CC} measurement.
<7:6>	5V	Read Only	5V LSBs. Holds the 2 LSBs of the 10-bit 5V measurement.

If this register is read, this register and the registers holding the MSB of each reading is frozen until read.

TABLE 41. EXTENDED RESOLUTION REGISTER 2

Bit	Name	Read/Write	Description
<1:0>	12V	Read Only	12V LSBs. Holds the 2 LSBs of the 10-bit 12V measurement.
<3:2>	TDM1	Read Only	Remote 1 Temperature LSBs. Holds the 2 LSBs of the 10-bit Remote 1 Temperature measurement.
<5:4>	LTMP	Read Only	Local Temperature LSBs. Holds the 2 LSBs of the 10-bit Local Temperature measurement.
<7:6>	TDM2	Read Only	Remote 2 Temperature LSBs. Holds the 2 LSBs of the 10-bit Remote 2 Temperature measurement.

If this register is read, this register and the registers holding the MSB of each reading is frozen until read.

TABLE 42. REGISTER 78H - CONFIGURATION REGISTER 3 (POWER-ON DEFAULT = 00H)

Bit	Name	R/W	Description
<0>	ALERT	Read/Write	When set to 1, pin 10 (PWM2/$\overline{\text{SMBALERT}}$) is configured as an SMBAlert interrupt output to indicate out-of-limit error conditions.
<1>	PHOT	Read/Write	When set to 1, pin 14 (TACH4/ADDR SEL/$\overline{\text{PROCHOT}}$) is configured as a $\overline{\text{PROCHOT}}$ input from the CPU. When $\overline{\text{PROCHOT}}$ is asserted, fans can be run at full speed or a timer can be triggered to time how long $\overline{\text{PROCHOT}}$ has been asserted for.
<2>	BOOST	Read/Write	When set to 1, assertion of $\overline{\text{PROCHOT}}$ will cause all fans to run at 100% duty cycle for failsafe cooling.
<3>	FAST	Read/Write	Setting this bit to 1 enables fast TACH measurements on all channels. This increases the TACH measurement rate from once a second, to one every 250ms (4 readings/sec).
<4>	DC1	Read/Write	When set to 1, this bit enables tach measurements to be continuously made on TACH1.
<5>	DC2	Read/Write	When set to 1, this bit enables tach measurements to be continuously made on TACH2.
<6>	DC3	Read/Write	When set to 1, this bit enables tach measurements to be continuously made on TACH3.
<7>	DC4	Read/Write	When set to 1, this bit enables tach measurements to be continuously made on TACH4.

* This register becomes Read Only when the Configuration Register 1 Lock bit is set to 1. Any further attempts to write to this register will have no effect.

TABLE 43. REGISTER 79H - PROCHOT STATUS REGISTER (POWER ON DEFAULT = 00H)

Bit	Name	Read/Write	Description
<5:0>	TMR	Read Only	Times how long $\overline{\text{PROCHOT}}$ is asserted for. This is a 6-bit timer with a resolution of 125ms allowing $\overline{\text{PROCHOT}}$ assertion durations of 125ms to 7.875 seconds to be measured.
<6>	NEG	Read Only	Gets set high when $\overline{\text{PROCHOT}}$ signal returns high. Cleared on Read.
<7>	ASRT	Read Only	Gets set high on assertion of $\overline{\text{PROCHOT}}$ signal low. Cleared on Read.

TABLE 44. REGISTER 7AH - PROCHOT MASK REGISTER (POWER ON DEFAULT = 00H)

Bit	Name	Read/Write	Description
<5:0>	LIMT	Read/Write	Sets maximum $\overline{\text{PROCHOT}}$ assertion length allowed, before an interrupt is generated. This is a 6-bit limit with a resolution of 125ms allowing $\overline{\text{PROCHOT}}$ assertion limits of 125ms to 7.875 seconds to be programmed. If the $\overline{\text{PROCHOT}}$ assertion time exceeds this limit, bit 5 of Interrupt Status Register 2 (Reg 0x42) will be set.
<6>	NEG	Read/Write	If set to 1, this will prevent an $\overline{\text{SMBALERT}}$ interrupt when $\overline{\text{PROCHOT}}$ returns high after its assertion. The NEG bit of the PROCHOT Status Register gets set as normal.
<7>	ASRT	Read/Write	If set to 1, this will prevent an $\overline{\text{SMBALERT}}$ interrupt when $\overline{\text{PROCHOT}}$ is asserted low. The ASRT of the PROCHOT Status Register gets set as normal.

TABLE 45. REGISTER 7BH - FAN PULSES PER REVOLUTION REGISTER (POWER ON DEFAULT = 55H)

Bit	Name	Read/Write	Description
<1:0>	FAN1	Read/Write	Sets number of pulses to be counted when measuring FAN1 speed. Can be used to determine fan's pulses per revolution number for unknown fan type. **Pulses Counted** 00 = 1 01 = 2 (default) 10 = 3 11 = 4
<3:2>	FAN2	Read/Write	Sets number of pulses to be counted when measuring FAN2 speed. Can be used to determine fan's pulses per revolution number for unknown fan type. **Pulses Counted** 00 = 1 01 = 2 (default) 10 = 3 11 = 4
<5:4>	FAN3	Read/Write	Sets number of pulses to be counted when measuring FAN3 speed. Can be used to determine fan's pulses per revolution for unknown fan type. **Pulses Counted** 00 = 1 01 = 2 (default) 10 = 3 11 = 4
<7:6>	FAN4	Read/Write	Sets number of pulses to be counted when measuring FAN4 speed. Can be used to determine fan's pulses per revolution for unknown fan type. **Pulses Counted** 00 = 1 01 = 2 (default) 10 = 3 11 = 4

TABLE 46. REGISTER 7EH - MANUFACTURERS TEST REGISTER 1 (POWER ON DEFAULT = 00H)

Bit	Name	Read/Write	Description
<7:0>	Reserved	Read Only	Manufacturer's Test Register. These bits are reserved for manufacturer's test purposes and should NOT be written to under normal operation.

* This register becomes Read Only when the Configuration Register 1 Lock bit is set to 1. Any further attempts to write to this register will have no effect.

TABLE 47. REGISTER 7FH - MANUFACTURERS TEST REGISTER 2 (POWER ON DEFAULT = 00H)

Bit	Name	Read/Write	Description
<7:0>	Reserved	Read Only	Manufacturer's Test Register. These bits are reserved for manufacturer's test purposes and should NOT be written to under normal operation.

* This register becomes Read Only when the Configuration Register 1 Lock bit is set to 1. Any further attempts to write to this register will have no effect.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

24-Pin QSOP Package (RQ-24)