PLL Frequency Synthesizer

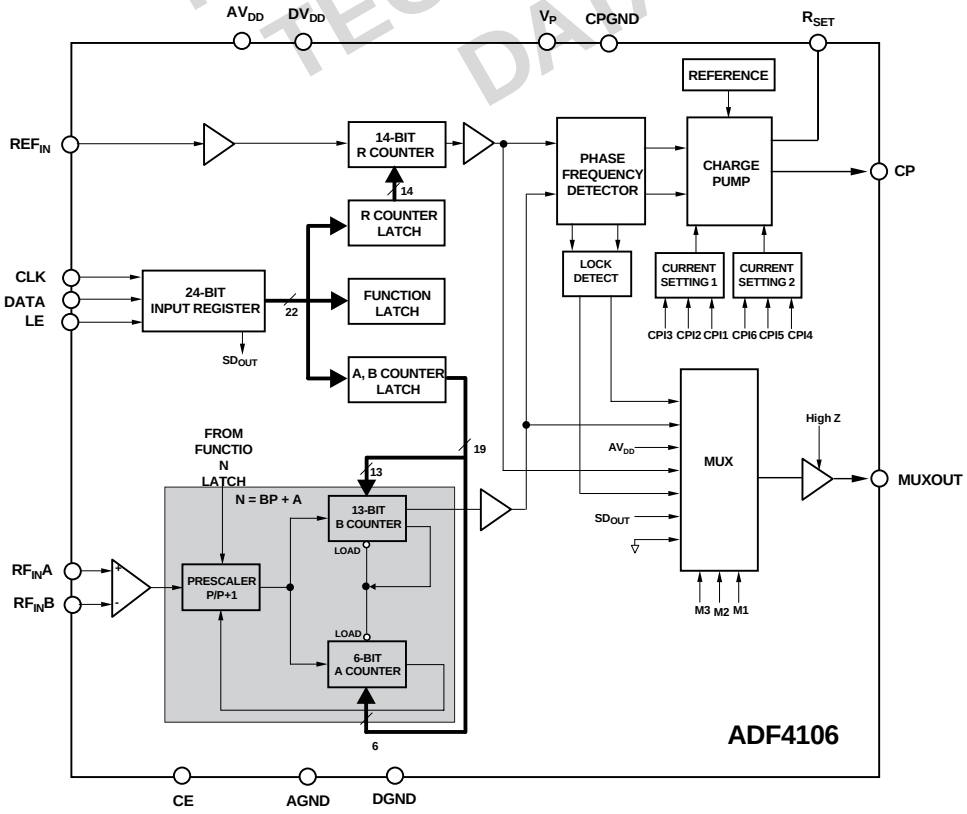
Preliminary Technical Data — ADF4106

FEATURES
6.5 GHz Bandwidth
+2.7 V to +3.3 V Power Supply
Separate Charge Pump Supply (V_P) Allows Extended Tuning Voltage in 3V Systems
Programmable Dual Modulus Prescaler 8/9, 16/17, 32/33, 64/65
Programmable Charge Pump Currents
Programmable Anti-Backlash Pulse Width
3-Wire Serial Interface
Analog and Digital Lock Detect
Hardware and Software Power Down Mode

APPLICATIONS
Broadband Wireless Access
Instrumentation
Wireless LANS

GENERAL DESCRIPTION
The ADF4106 frequency synthesizer can be used to implement local oscillators in the up-conversion and down-conversion sections of wireless receivers and transmitters. It consists of a low-noise digital PFD (Phase Frequency Detector), a precision charge pump, a programmable reference divider, programmable A and B counters and a dual-modulus prescaler (P/P+1). The A (6-bit) and B (13-bit) counters, in conjunction with the dual modulus prescaler (P/P+1), implement an N divider (N= BP+A). In addition, the 14-bit reference counter (R Counter), allows selectable REFIN frequencies at the PFD input. A complete PLL (Phase-Locked Loop) can be implemented if the synthesizer is used with an external loop filter and VCO (Voltage Controlled Oscillator). Its very high bandwidth means that frequency doublers can be eliminated in many high frequency systems, simplifying system architecture and lowering cost.

FUNCTIONAL BLOCK DIAGRAM



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ADF4106 – SPECIFICATIONS[1] ($AV_{DD} = DV_{DD} = +3\ V \pm 10\%$; $AV_{DD} \le V_P \le 5.0V$; AGND = DGND = CPGND= 0 V; $R_{SET} = 4.7k\Omega$; $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted)

Parameter	B Version	BChips[2] (Typical)	Units	Test Conditions/Comments
RF CHARACTERISTICS (3V)				See Figure X for input circuit.
RF Input Frequency (RF_{IN})	0.5/6.5	0.5/6.5	GHz min/max	Use a square wave for lower frequencies
RF Input Sensitivity	-15/0	-15/0	dBm min/max	
Maximum Allowable Prescaler Output Frequency[3]	275	275	MHz max	
REFIN CHARACTERISTICS				
REFIN Input Frequency	0/150	0/150	MHz min/max	
REFIN Input Sensitivity[4]	-5/0	-5/0	dBm min/max	AC coupled. When DC coupled: 0 to V_{DD} max (CMOS Compatible)
REFIN Input Capacitance	10	10	pF max	
REFIN Input Current	±100	±100	µA max	
PHASE DETECTOR				
Phase Detector Frequency[5]	100	100	MHz max	
CHARGE PUMP				
I_{CP} sink/source				Programmable: See Table 5
High Value	5	5	mA typ	With $R_{SET} = 4.7k\Omega$
Low Value	625	625	µA typ	
Absolute Accuracy	2.5	2.5	% typ	With $R_{SET} = 4.7k\Omega$
R_{SET} Range	2.7/10	2.7/10	kΩ typ	See Table 5
I_{CP} 3-State Leakage Current	1	1	nA max	
Sink and Source Current Matching	2	2	% typ	$0.5V \le V_{CP} \le V_P - 0.5$
I_{CP} vs. V_{CP}	1.5	1.5	% typ	$0.5V \le V_{CP} \le V_P - 0.5$
I_{CP} vs. Temperature	2	2	% typ	$V_{CP} = V_P/2$
LOGIC INPUTS				
V_{INH}, Input High Voltage	0.8 x DV_{DD}	0.8 x DV_{DD}	V min	
V_{INL}, Input Low Voltage	0.2 x DV_{DD}	0.2 x DV_{DD}	V max	
I_{INH}/I_{INL}, Input Current	±1	±1	µA max	
C_{IN}, Input Capacitance	10	10	pF max	
LOGIC OUTPUTS				
V_{OH}, Output High Voltage	DV_{DD} - 0.4	DV_{DD} - 0.4	V min	$I_{OH} = 500\mu A$
V_{OL}, Output Low Voltage	0.4	0.4	V max	$I_{OL} = 500\mu A$
POWER SUPPLIES				
AV_{DD}	2.7/3.3	2.7/3.3	V min/V max	
DV_{DD}	AV_{DD}	AV_{DD}		
V_P	AV_{DD}/5.0	AV_{DD}/5.0	V min/V max	$AV_{DD} \le V_P \le 5.0V$
I_{DD}[6] ($AI_{DD} + DI_{DD}$)				See Figures 27 and 28
ADF4106	15	15	mA max	12mA typical
I_P	0.4	0.4	mA max	$T_A = +25°C$
Low Power Sleep Mode	1	1	µA typ	

NOTES
1. Operating temperature range is as follows: B Version: –40°C to +85°C.
2. The BChip specifications are given as typical values.
3. This is the maximum operating frequency of the CMOS counters. The prescaler value should be chosen to ensure that the RF input is divided down to a frequency which is less than this value.
4. $AV_{DD} = DV_{DD} = 3V$
5. Guaranteed by design. Sample tested to ensure compliance.
6. $T_A = +25°C$; $AV_{DD} = DV_{DD} = 3V$; P = 16; SYNC = 0; DLY = 0; $RF_{IN} = 6.4GHz$

ADF4106 – SPECIFICATIONS[1] (AV_{DD} = DV_{DD} = +3 V ± 10% ; AV_{DD} ≤ V_P ≤ 5.0V ; AGND = DGND = CPGND= 0 V; R_{SET} = 4.7kΩ; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	B Version	BChips[2]	Units	Test Conditions/Comments
NOISE CHARACTERISTICS				
ADF4106 Phase Noise Floor[3]	-171	-171	dBc/Hz typ	@ 25kHz PFD Frequency
	-164	-164	dBc/Hz typ	@ 200kHz PFD Frequency
	-156	-156	dBc/Hz typ	@ 1MHz PFD Frequency
Phase Noise Performance[4]				@ VCO Output
6400MHz Output[5]	-74	-74	dBc/Hz typ	@ 1kHz offset and 200kHz PFD Frequency
6400MHz Output[6]	-80	-80	dBc/Hz typ	@ 1kHz offset and 1MHz PFD Frequency
Spurious Signals				
6400MHz output[5]	-65/-70	--65/-68	dBc typ	@ 200kHz/400kHz and 200kHz PFD Frequency
6400MHz Output[6]	-70/-75	-70/-75	dBc typ	@ 1MHz/2MHz and 1MHz PFD Frequency

NOTES

1. Operating temperature range is as follows: B Version: –40°C to +85°C.
2. The BChip specifications are given as typical values.
3. The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20logN (where N is the N divider value).
4. The phase noise is measured with the EVAL-ADF4106EB1 Evaluation Board and the HP8562E Spectrum Analyzer. The spectrum analyzer provides the REFIN for the synthesizer (f_{REFOUT} = 10MHz @ 0dBm). SYNC = 0; DLY = 0 (See Table 3).
5. f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; Offset frequency = 1 kHz; f_{RF} = 6400MHz; N = 32000; Loop B/W = 20kHz
6. f_{REFIN} = 10 MHz; f_{PFD} = 1MHz; Offset frequency = 1 kHz; f_{RF} = 6400MHz; N = 6400; Loop B/W = 100kHz

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADF4106BRU	–40°C to +85°C	RU-16
ADF4106BCP	–40°C to +85°C	CP-20

* RU = Thin Shrink Small Outline Package (TSSOP)
CP = Chip Scale Package
Contact the factory for chip availability

TIMING CHARACTERISTICS

(AV_{DD} = DV_{DD} = +3 V ± 10% ; AV_{DD} ≤ V_P ≤ 5.0V ; AGND = DGND = CPGND= 0 V; R_{SET} = 4.7kΩ; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Units	Test Conditions/Comments
t_1	10	ns min	DATA to CLOCK Set Up Time
t_2	10	ns min	DATA to CLOCK Hold Time
t_3	25	ns min	CLOCK High Duration
t_4	25	ns min	CLOCK Low Duration
t_5	10	ns min	CLOCK to LE Set Up Time
t_6	20	ns min	LE Pulse Width

NOTE
Guaranteed by Design but not Production Tested.

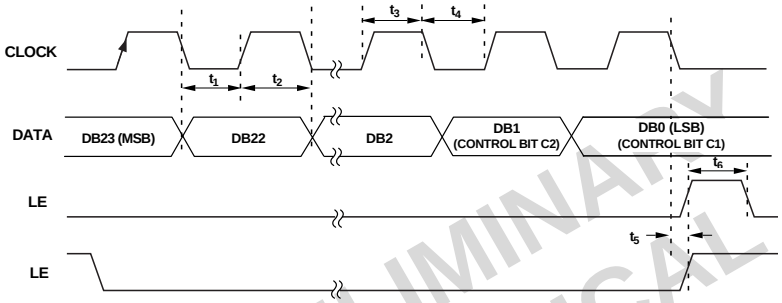


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1, 2]
(T_A = +25°C unless otherwise noted)

AV_{DD} to GND[3] ..... –0.3 V to +3.6 V
AV_{DD} to DV_{DD} ..... –0.3 V to +0.3 V
V_P to GND ..... –0.3 V to +5.3 V
V_P to AV_{DD} ..... –0.3 V to +5.3 V
Digital I/O Voltage to GND ..... –0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND ..... –0.3 V to V_P + 0.3 V
REF_{IN}, $RF_{IN}A$, $RF_{IN}B$ to GND ..... –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Industrial (B Version) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Maximum Junction Temperature ..... +150°C
TSSOP θ_{JA} Thermal Impedance ..... 150.4°C/W
CSP θ_{JA} Thermal Impedance ..... 122°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. This device is a high-performance RF integrated circuit with an ESD rating of < 2kV and it is ESD sensitive. Proper precautions should be taken for handling and assembly.
3. GND = AGND = DGND = 0V

CAUTION

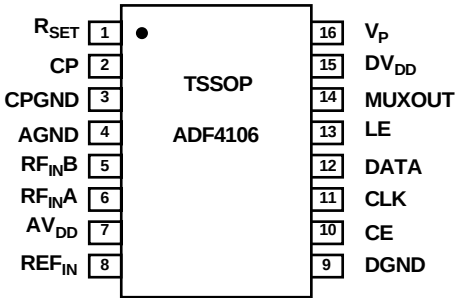
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this device features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN DESCRIPTION

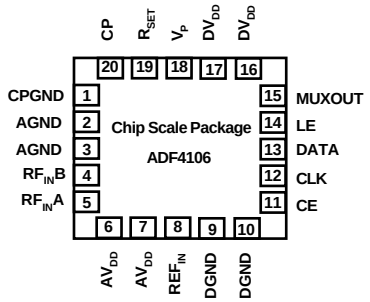
Mnemonic	Function
R_{SET}	Connecting a resistor between this pin and CPGND sets the maximum charge pump output current. The nominal voltage potential at the R_{SET} pin is 0.66V. The relationship between I_{CP} and R_{SET} is $$I_{CPmax} = \frac{23.5}{R_{SET}}$$ So, with R_{SET} = 4.7kΩ, I_{CPmax} = 5mA.
CP	Charge Pump Output. When enabled this provides ±I_{CP} to the external loop filter, which in turn drives the external VCO.
CPGND	Charge Pump Ground. This is the ground return path for the charge pump.
AGND	Analog Ground. This is the ground return path of the prescaler.
$RF_{IN}B$	Complementary Input to the RF Prescaler. This point must be decoupled to the ground plane with a small bypass capacitor, typically 100pF. See Figure 3.
$RF_{IN}A$	Input to the RF Prescaler. This small signal input is ac coupled to the external VCO.
AV_{DD}	Analog Power Supply. This may range from 2.7V to 3.3V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. AV_{DD} must be the same value as DV_{DD}
REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of V_{DD}/2 and a dc equivalent input resistance of 100kΩ. See Figure 2. This input can be driven from a TTL or CMOS crystal oscillator or it can be ac coupled.
DGND	Digital Ground.
CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump output into 3-state mode. Taking the pin high will power up the device depending on the status of the power-down bit F2.
CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, the latch being selected using the control bits.
MUXOUT	This multiplexer output allows either the Lock Detect, the scaled RF or the scaled Reference Frequency to be accessed externally.
DV_{DD}	Digital Power Supply. This may range from 2.7V to 3.3V. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. DV_{DD} must be the same value as AV_{DD}.
V_P	Charge Pump Power Supply. This should be greater than or equal to V_{DD}. In systems where V_{DD} is 3V, it can be set to 5V and used to drive a VCO with a tuning range of up to 5V.

PIN CONFIGURATIONS

TOP VIEW



TOP VIEW



TRANSISTOR COUNT: 6425 (CMOS) and 303 (Bipolar).