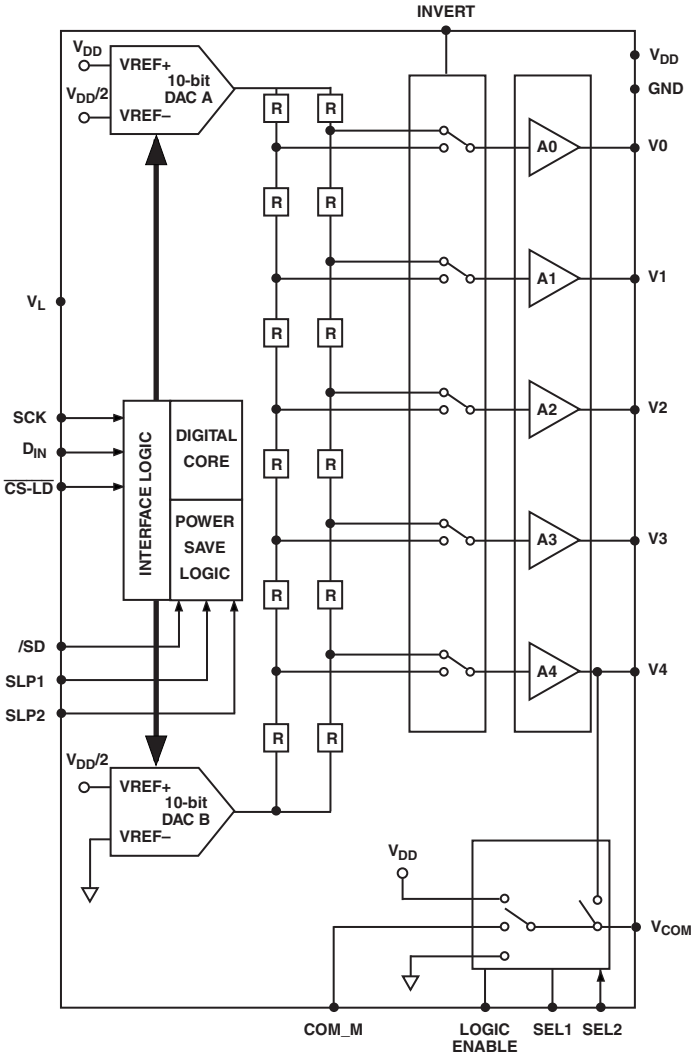
Integrated LCD Grayscale Generator

Preliminary Technical Data — ADD8502

FEATURES
2 Mask Programmable Sets of 5 Reference Levels
Dual 10-Bit DACs for Flicker Offset and Range Adjustment
Integrated V_{COM} Switching
Single-Supply Operation: 5.0 V
Low Supply Current: 300 μA
Global Power Save Mode: 1 μA Max
Fast Settling Time for Load Change: 20 μs
Stable with 20 nF/100 Ω Loads
CMOS/TTL Input Levels

APPLICATIONS
Color TFT Cell Phones
Color TFT PDAs

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADD8502 is an integrated, high-accuracy programmable grayscale generator. Two sets of five output reference voltages are mask programmed to 0.2% resolution and the outputs switch between the two sets of five levels. The reference levels are selected from a 512 tap resistor network using a via mask.

ADD8502 includes two serially addressable, 10-bit digital to analog converters (DACs) and five fast low current buffers. The dual DACs set the endpoint voltages applied to the resistor network to adjust for flicker and range. Two modes of Power Save can reduce total current to less than 1 μA and feature fast recovery time from Shutdown/Sleep mode. The ADD8502 accepts CMOS or TTL inputs for all controls including the common drive circuit levels.

ADD8502 operates over the industrial temperature range from –40°C to +85°C and is available in a space saving 24 lead 4 mm × 4 mm lead-frame chip-scale package.

REV. PrA

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ADD8502–SPECIFICATIONS (@ V_{DD} = +5.0 V, −40°C ≤ T_A ≤ +85°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SYSTEM ACCURACY						
V_{OUT} Error				5	25	mV
Swing Error[1]		$(V_{Pn} – V_{Nn}) – (V_{Pi} – V_{Ni})$		8	35	mV
Mean Error[2]		$(V_{Pn}+ V_{Nn})/2 – (V_{Pi} + V_{Ni})/2)$		5	18	mV
Mean Error Between Adjacent Channels[3]				2	20	mV
Mean Error Between V_0 and V_4[4]				10	35	mV
DAC ACCURACY						
Resolution				10		Bits
Differential Nonlinearity	DNL			±0.25		LSB
Integral Nonlinearity[5]	INL			±0.5		LSB
Offset Error				±0.4		% of FSR
Gain Error				±0.15		% of FSR
OUTPUT CHARACTERISTICS						
Output Current	I_{OUT}	$(V_{DD} – 1 V)$		25		mA
Short Circuit Current	I_{SC}	Short to Ground		60		mA
Output Leakage Current in High Z Mode	$I_{LEAKAGE}$	High Z Mode		0.01	1.0	µA
Slew Rate	SR	R_L = 100 kΩ		1.25		V/µs
Settling time to 1%	t_S	V_0 to V_4 Step Size		8	12	µs
Slew Rate[5]	SR	L_D =100 Ω series 16 nF		0.7		V/µs
Settling time to 1%[5]	t_S	V_0 to V_4 Step Size		8	12	µs
Phase Margin	ϕo			67		Degrees
V_{COM} SWITCHES ACTIVE IMPEDANCE						
COM to VDD	Z	See Table IV		25	50	Ω
COM to GND	Z			25	50	Ω
COM to COM_M	Z	I = 20 mA		25	50	Ω
COM to V4	Z			25	50	Ω
MASK PROGRAMMABLE RESISTOR CHAIN						
Total Resistor Chain	R_{TOTAL}	512 resistor segments		205		kΩ
Step Matching	R_{MATCH}	Any two segments		1		%
POWER SUPPLY						
Supply Voltage	V_{DD}		4.5	5	5.5	V
Supply Current	I_{SY}	V_{DD} = 5 V; No Load	190	270	400	µA
Shutdown Supply Current	I_{SY-GLB}	Full shutdown mode		0.2	1	µA
Sleep Supply Current	$I_{SY-SLP1-3}$	Mid 3 Buffers shutdown	140	175	210	µA
Shut Down Recovery Time		Global PD to 1%		23	30	µs
Sleep Recovery Time		V1-V3 off to 1%		10	15	µs
LOGIC SUPPLY						
Logic Input Voltage Level	V_L		2.3	3.3	5.5	V
Logic Input Current	I_{VL}			0.01	1	µA
DIGITAL I/O						
Digital Input High Voltage	V_{IH}		V_L * 0.7			V
Digital Input Low Voltage	V_{IL}				V_L * 0.3	V
Digital Input Current	I_{IN}	GND ≤ V_{IN} ≤ 5.5 V			±1	µA
Digital Input Capacitance	C_{IN}				10	pF

[1]Swing error is comparison of measured V_{OUT} step vs. theoritical V_{OUT} step. Theoritical values can be found on the Mask Tap Point Option sheet
[2]Mean error is measured V_{OUT} mean vs. theoritical V_{OUT} mean. See Figure 3.
[3]Mean errors between two adjacent channels vs theoritical. See Figure 3.
[4]Mean errors between V0 and V4 vs theoritical. See Figure 3.
[5]Slew Rate and Settling Time is measured between the output resistor in series with the capacitor. See Figure 1.

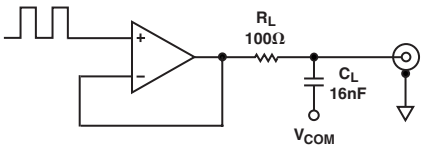


Figure 1. Slew Rate Diagram

Table I. Serial Data Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Units
SCK Cycle Time	t1	100			ns
SCK High Time	t2	45			ns
SCK Low Time	t3	45			ns
/CS-LD Setup Time	t4	20			ns
Data Setup Time	t5	5			ns
Data Hold Time	t6	5			ns
LSB SCK High to /CS-LD High	t7	5			ns
Minimum /CS-LD High Time	t8	10			ns
SCK to /CS-LD Active Edge Setup Time	t9	5			ns
/CS-LD High to SCK Positive Edge	t10	10			ns
SCK Frequency (Square Wave)				10	MHz

NOTES
[1]All input signals are specified with rise/fall time – 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_S + V_{IH})/2$.
[2]See Figure 2

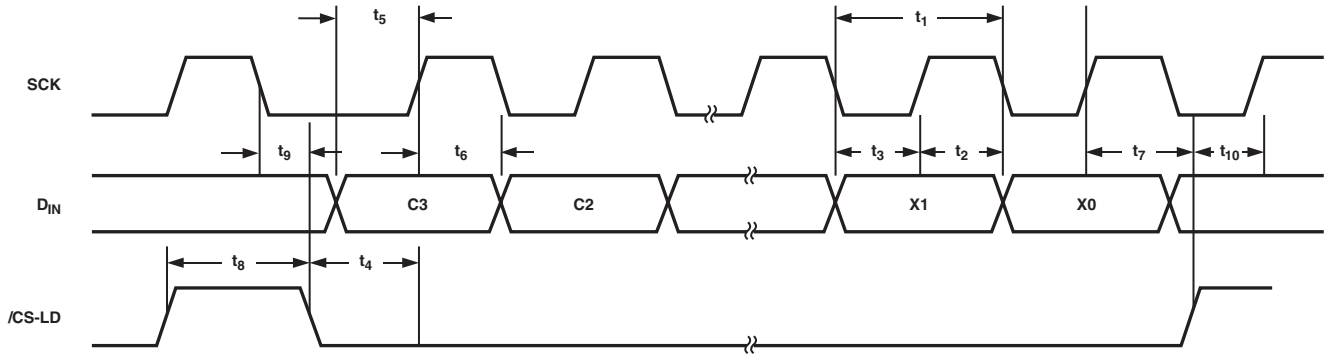


Figure 2. Serial Write Interface

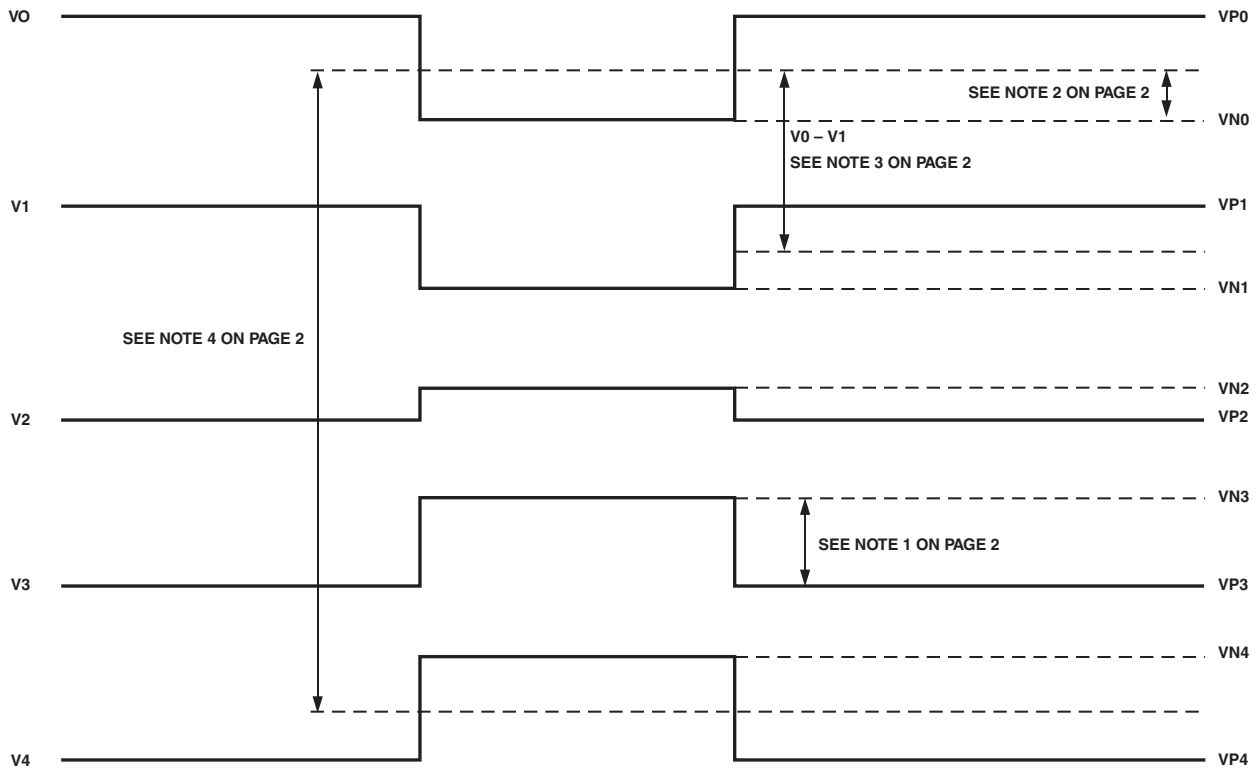


Figure 3. Output Wave Form Diagram

ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} to GND . . . . . –0.3 V to +7 V
V_L to GND . . . . . –0.3 V to +7 V
Digital Input Voltage to GND . . . . . –0.3 V to +7 V
V_{OUT} to GND . . . . . –0.3 V to V_{DD} +0.3 V
V_{COM} to GND . . . . . –0.3 V to V_{DD} +0.3 V
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 10 sec)
Vapor Phase (60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

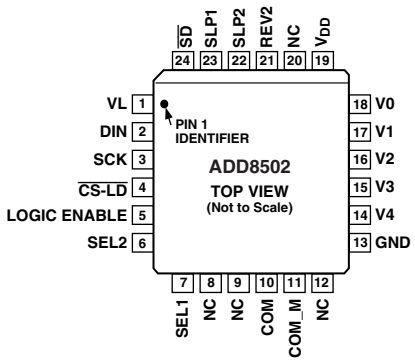
Package Type	θ_{JA}[1]	Ψ_{JB}	Units
24-Lead LFCSP (ACP)	34.8	13	°C/W

NOTEs
[1]θ_{JA} is specified for worst case conditions, i.e., θ_{JA} is specified for device soldered in circuit board for surface mount packages.
[1]ψ_{JB} is applied for calculating the junction temperature by reference to the board temperature.

Model	Temperature Range	Package Description	Package Option
ADD8502ACP	–40°C to +85°C	24-Lead LFCSP	CP-24

Available in 7" reel only.

PIN CONFIGURATION

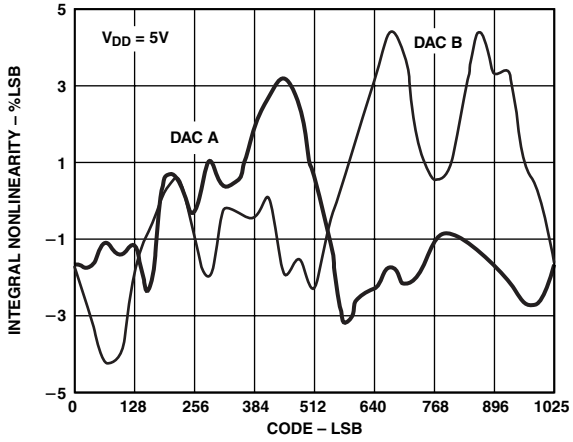


NC = NO CONNECT

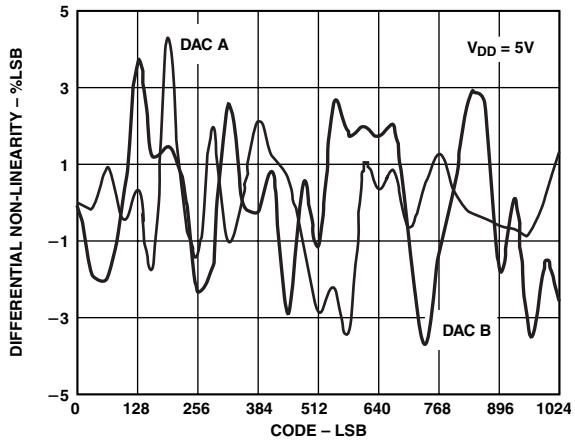
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADD8502 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

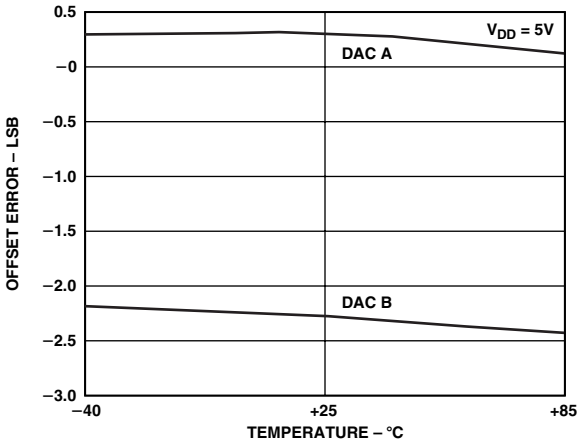
ADD8502–Typical Performance Characteristics



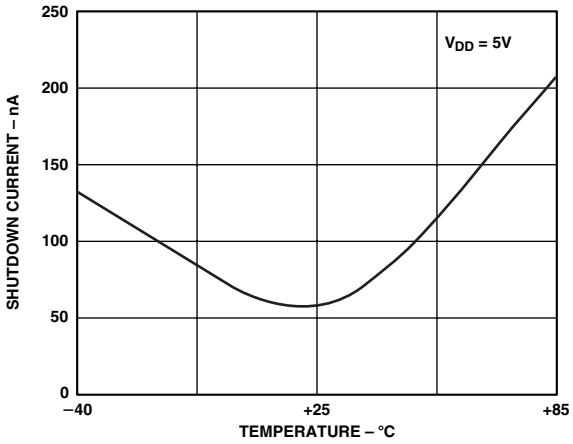
TPC 1. DAC Integral Nonlinearity



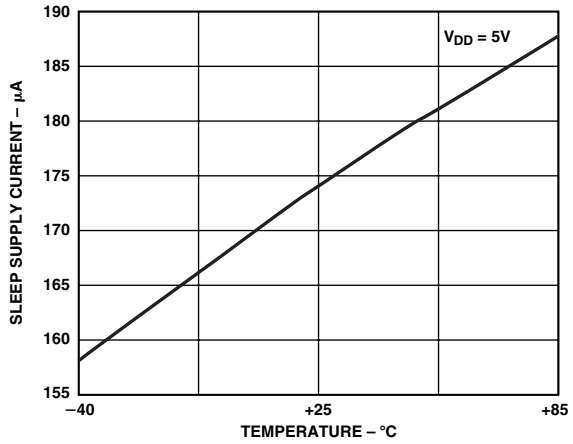
TPC 2. DAC Differential Nonlinearity



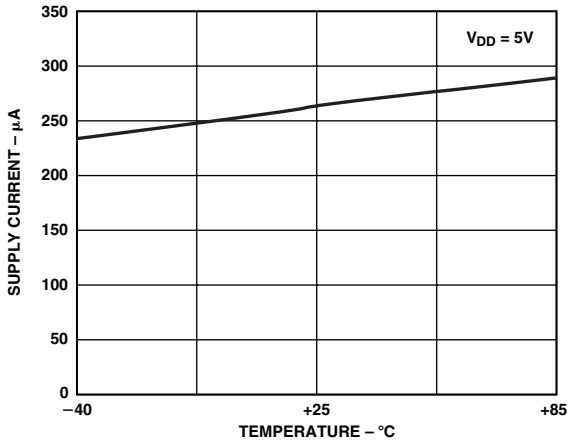
TPC 3. Offset Error vs. Temperature



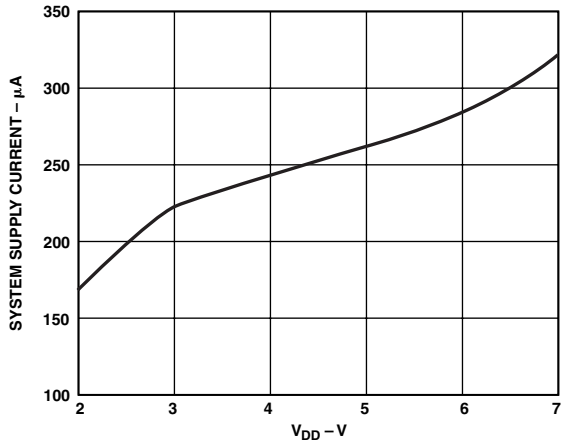
TPC 4. Shutdown Current vs. Temperature



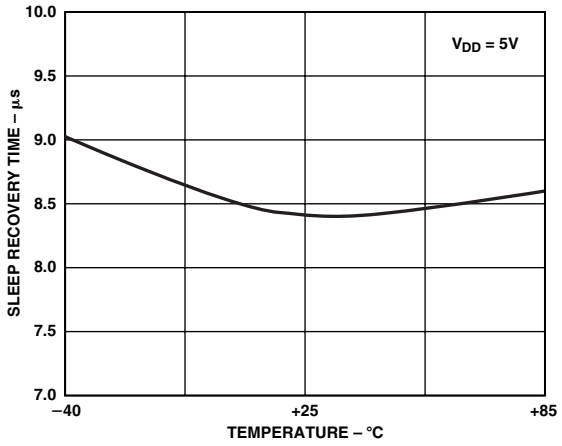
TPC 5. Sleep Supply Current vs. Temperature



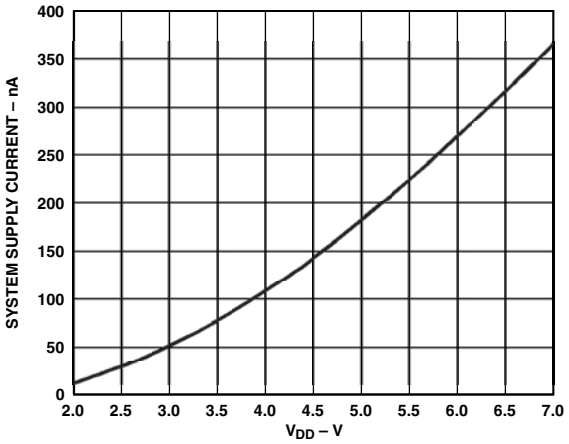
TPC 6. Supply Current vs. Temperature



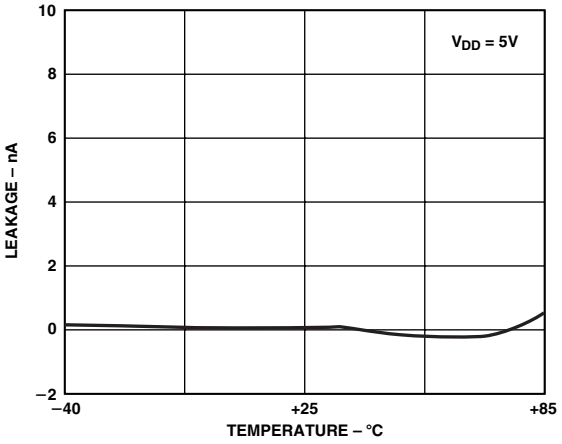
TPC 7. System Supply Current at Full Power



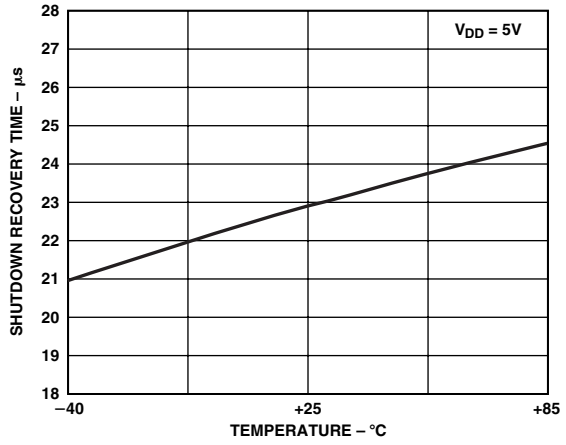
TPC 10. Sleep Recovery Time vs. Temperature



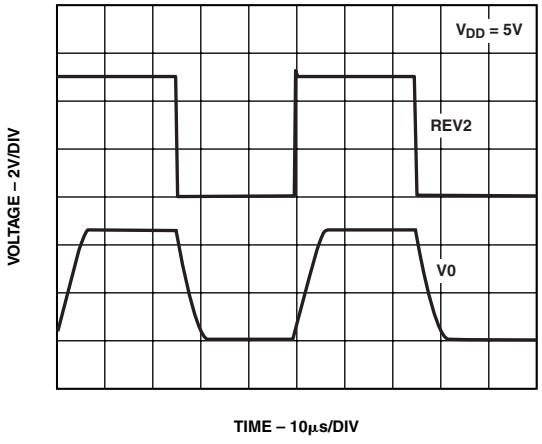
TPC 8. Syetem Supply Current at Shutdown



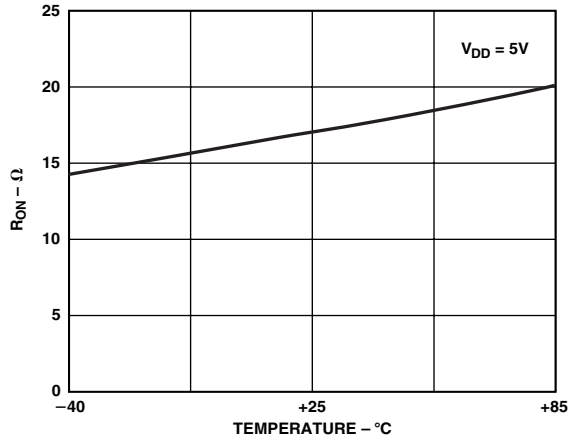
TPC 11. Output Leakage



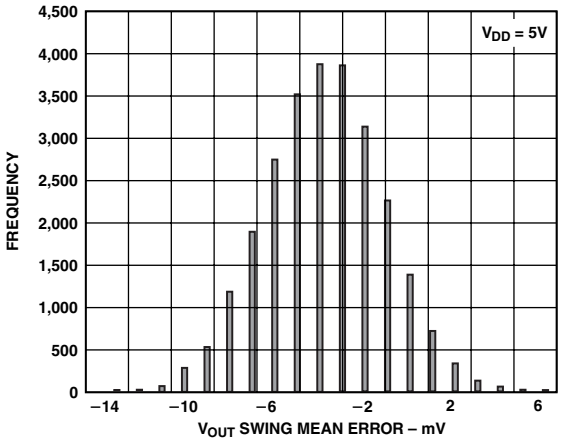
TPC 9. Shutdown Recovery Time vs. Temperature



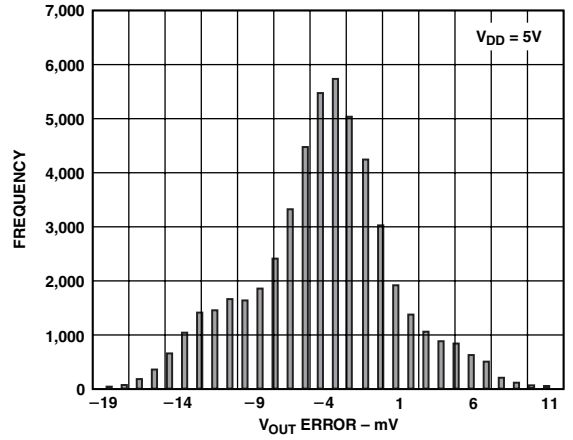
TPC 12. V0 Output Swing Response to REV2



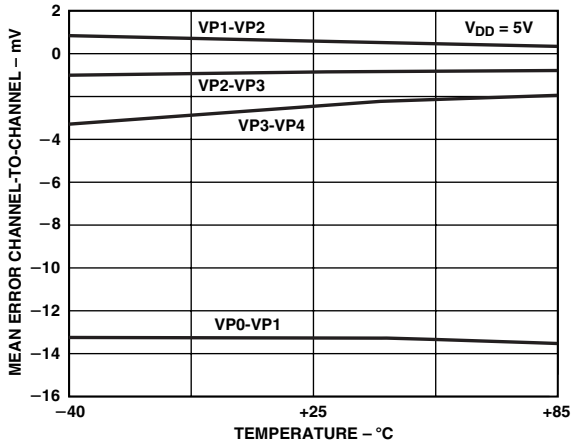
TPC 13. V_{COM} Switch-On-Resistance vs. Temperature



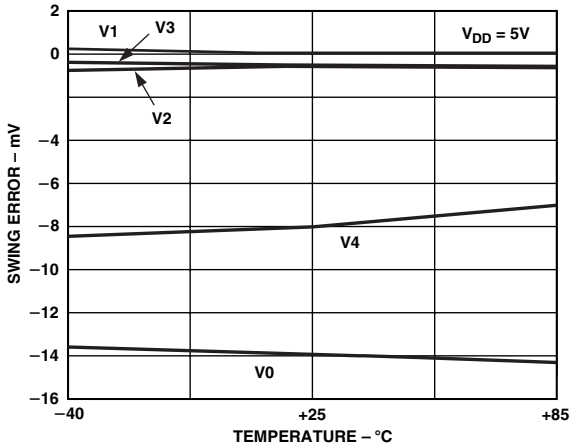
TPC 16. V_{OUT} Swing Mean vs. Distribution



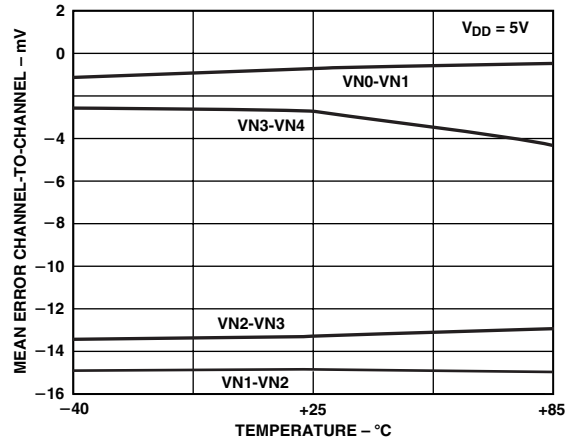
TPC 14. V_{OUT} Error Distribution



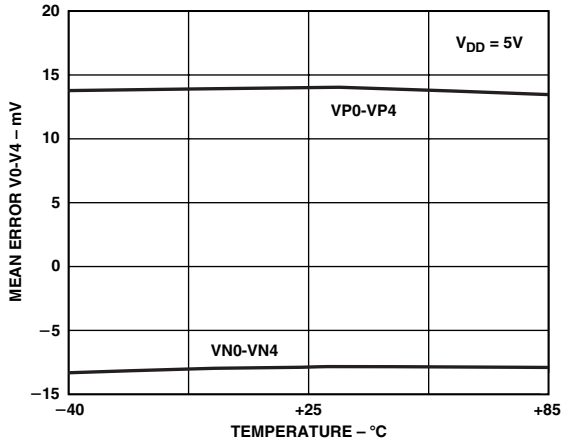
TPC 17. Mean Error Between Adjacent Channel vs. Temperature



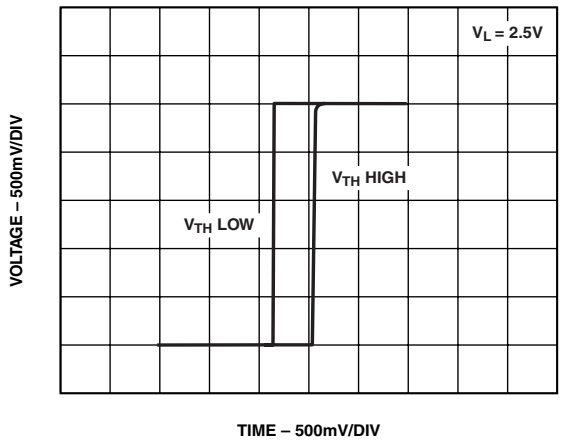
TPC 15. Swing Error vs. Temperature



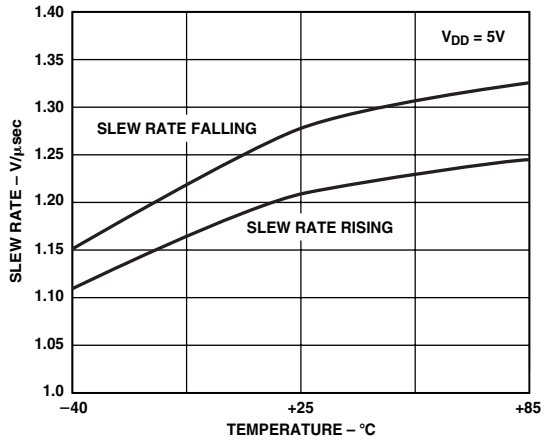
TPC 18. Mean Error Between Adjacent Channel vs. Temperature



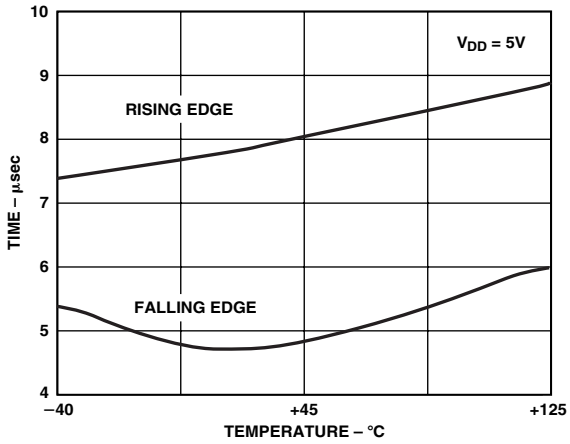
TPC 19. Mean Error Between VO and V4 vs. Temperature



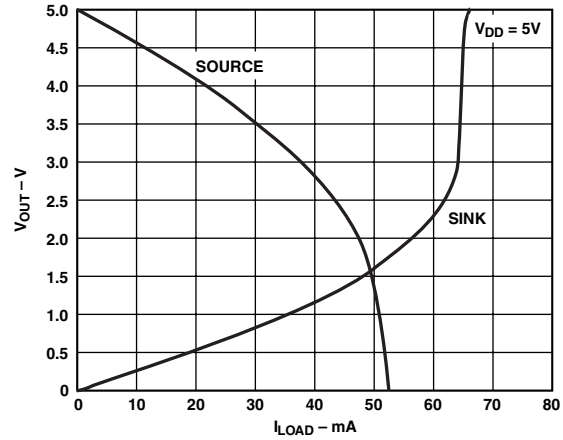
TPC 20. REV1 Hysteresis



TPC 21. Slew Rate vs. Temperature



TPC 22. Settling Time at V_{OUT} vs. Temperature



TPC 23. Output Current Source and Sink

OPERATION

Transfer Function

The transfer function for the ADD8502 is given the following equations:

1. Digital to analog transfer function for DAC A. An output can be derived from Equation 1 as:

$$V_{OUTA} = \left(\frac{V_{DD}}{2}\right)\left(1 + \frac{D_A}{1024}\right) \quad (1)$$

2. Digital to analog transfer function for DAC B. An output can be derived from Equation 2 as:

$$V_{OUTB} = \left(\frac{D_B}{1024}\right)\left(\frac{V_{DD}}{2}\right) \quad (2)$$

Where D_A and D_B are decimal equivalents of the binary codes that are loaded to the DAC register from 0 to 1023.

3. Using any programmed tap point from the 512 resistor string, the system output can be derived from Equation 3:

$$V_{TX} = (V_{OUTA} - V_{OUTB})\left(\frac{T_X}{512}\right) + V_{OUTB} \quad (3)$$

Where T_X is any tap point of the 512-resistor string. It is mask programmable. V_{TX} is the voltage output at any output (VO, ...V4), and will switch between two voltages depending on the mask programmed tap points.

Example: V_{DD} = 5 V, D_A = 1,000, D_B = 100 and T_X = 500.

V_{OUTA} = 4.941 V
V_{OUTB} = 0.244 V
V_{TX} = 4.831 V

The above equations will provide a theoretical calculation the outputs. The actual will vary with load, process and architecture. See specifications table.

SERIAL INTERFACE

The ADD8502 has a three-wire serial interface (/CS-LD, SCK, and D_{IN}). The writing sequence begins by bringing the /CS-LD line LOW. Data on the DIN line is clocked into the 16-bit shift register on the rising edge of SCK. The serial clock frequency can be as high as 10 MHz. When the last data bit is clocked in, /CS-LD line needs to be brought HIGH to load the DAC registers and the operation mode is dependent upon the control bits.

Input Shift Register

The input shift register is 16 bits wide (See Figure 4). The first four control bits (C3, C2, C1, C0) are used to set different operating modes of the device. The next 10 bits are the data bits and last two bits are “don’t cares”. This composes a full word which is transferred to the DAC register on the rising edge of /CS-LD.

In a normal write sequence, the /CS-LD line is kept LOW for at least 16 rising edges of SCK and then it is brought HIGH to update the DACs. However, if /CS-LD is brought HIGH before the 16th rising edge this acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents or a change in the operation mode occurs.

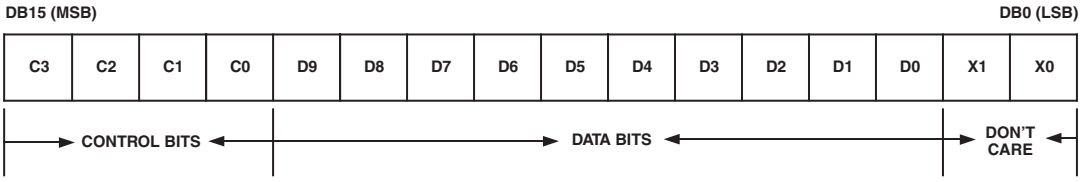


Figure 4. Input Register Contents

Table III. DAC Control Function

Control Code C3	C2	C1	C0	Input Register Status	DAC Register Status	Power-Down Status (Sleep/Wake)	Comments
0	0	0	0	No Change	No Update	No Change	No operation; power-down status unchanged (Part stays in Wake or Sleep Mode)
0	0	0	1	Load DAC A	No Update	No Change	Load input register A with data. DAC outputs unchanged. Power down status unchanged.
0	0	1	0	Load DAC B	No Update	No Change	Load input register B with data. DAC outputs unchanged. Power down status unchanged.
0	0	1	1		Not Used		
0	1	0	0		Not Used		
0	1	0	1		Not Used		
0	1	1	0		Not Used		
0	1	1	1		Not Used		
1	0	0	0	No Change	Update Outputs	Wake	Load both DAC registers with existing contents of input registers. Update DAC outputs. Part wakes up.
1	0	0	1	Load DAC A	Update Outputs	Wake	Load input register A. Load DAC registers with new contents of input register A and existing contents of register B. Update DAC outputs. Part wakes up.
1	0	1	0	Load DAC B	Update Outputs	Wake	Load input register B. Load DAC registers with new contents of input register B and existing contents of register A. Update DAC outputs. Part wakes up.
1	0	1	1		Not Used		
1	1	0	0		Not Used		
1	1	0	1	No Change	No Update	Wake	Part wakes Up. Input and DAC registers unchanged. DAC outputs reflect existing contents of DAC registers
1	1	1	0	No Change	No Update	Sleep	Power down the IC, put in into sleep mode
1	1	1	1	Load DACs A, B with same 10-bit code	Update Outputs	Wake	Load both input registers. Load both DAC registers with new contents of input registers. Update DAC outputs. Part wakes up.

Modes of Operation

The ADD8502 has various modes of operation such as updating both DACs simultaneously or changing the power-down status (Sleep/Wake). These are selected by writing the appropriate 4-bit Control Code (C0-C3). The details for each mode are summarized in Table II.

Low Power Serial Interface

To reduce the power consumption of the device ever further, the interface only powers up fully when the device is being written to. As soon as the 16-bit control word has been written to the part, the SCK and DIN input buffers are powered down. They only power-up again following a falling edge of /CS-LD.

Double-Buffered Interface

The ADD8502 has double-buffered interfaces consisting two banks of registers: input registers and DAC registers. The input register is connected directly to the input shift register and the digital code is transferred to the relevant input register on completion of a valid write sequence. The DAC register contains the digital code used by the resistor string.

Access to the DAC register is controlled by the control codes, C0 to C3. The user can update both DACs simultaneously and as well as individually. It depends on the selected control codes to update individual output or both outputs simultaneously.

Initial Power Up Condition

The ADD8502 has a pre-set DAC conditions when it's initially powered on. The DACs are loaded with 1110 1011 11 for the Upper DAC and Lower DAC with 0000 1010 00. And the part is powered up in a normal operation mode (Wake Status).

Power Down Modes

The ADD8502 has two shutdown modes. One mode is to fully shut-down the device using /SD or using the digital serial control code and the other mode is to shut-down V1 to V3 buffers using SLP1 and SLP2. See Table IV for priority of shutdown control functions.

The ADD8502 will have quiescent current less than 1uA when it is fully shutdown and all the output buffers are switched to high impedance state. The only active circuitries are the digital logics and the latches for the serial control. When the device is brought back from sleep mode to normal operation, it will use the last serial word to update the DACs or a new control code or data if any was loaded when the part was in the sleep mode; i.e., the contents of input register, DAC register and power down status shown in Table II is retained as long as V_{DD} and V_L are on.

The second power save mode (mid 3 buffers are shut-down) is using SLP1 and SLP2. In a condition where both SLP1 and SLP2 logics are HIGH, the output buffers, (V1, V2, V3) are shutdown and switched into high impedance state.

Table IV. Shutdown Control Function

/SD	Serial Control	SLP1	SLP2	Operation Mode
H	Wake	L	L	Normal Operation
H	Wake	L	H	Normal Operation
H	Wake	H	L	Normal Operation
H	Wake	H	H	Mid 3 buffers are shutdown
H	Sleep	X	X	Full Shut-down
L	X	X	X	Full Shut-down

X = Don't Care

V_{COM} LOGIC

V_{COM} operation is described in Table V. The Vcom logic is always active and its logic inputs are LOGIC ENABLE, SEL1, and SEL2. When LOGIC ENABLE is LOW, COM is connected COM_M. When LOGIC ENABLE is HIGH, COM is determined by the logic input of SEL1. If SEL1 is High, COM is connected to COM_H and when SEL1 is LOW, COM is connected to COM_L.

SEL2 controls the V4 output. If SEL2 goes LOW, V4 is connected to COM and A4 is shutdown with its output in a Hi-Z state. When SEL2 is HIGH, the switch connecting V4 to COM is open and A4 is in normal operation mode.

Table V. V_{COM} Logic Control

Inputs			Outputs	
LOGIC ENABLE	SEL1	SEL2	V_{COM}	V4
L	X	L	COM_M	COM
L	X	H	COM_M	A4
H	L	L	GND	COM
H	H	L	VDD	COM
H	L	H	GND	A4
H	H	H	VDD	A4

X = Don't Care

Table VI. ADD8502 Pin Descriptions

Pin #	Pin	Name	I/O	Description
1	VL	Logic Select Pin	I	Logic supply voltage. Connect to supply used for system logic can accept 2.7 V to V_{DD}
2	DIN	Serial Data Input	I	When CS is LOW, the input on this pin is shifted into the internal shift register on the rising edge of SCK.
3	SCK	Serial Clock	I	Accepts up to 10 MHz input. The rising edge on this clock will shift the data on DIN pin into the internal shift registers
4	/CS-LD	Load	I	When /CS-LD is LOW, SCK is enabled for shifting data on the DIN input into the internal shift register on the rising edge of SCK. Data is loaded MSB-first.
5	LOGIC ENABLE	Logic Control 2 for V_{COM}	I	When LOGIC ENABLE is LOW, COM will output the voltage level input on COM_M. When LOGIC ENABLE is HIGH, COM levels will be determined by the input on SEL1.
6	SEL2	Logic control V4	I	If SEL2 is HIGH, V4 output is the output of the op amp A4. If SEL2 is LOW, V4 is connected to COM and op amp A4 is shutdown. Refer to Table 3.
7	SEL1	Logic Control 1 for V_{COM}	I	With LOGIC ENABLE HIGH, a HIGH on SEL1 will cause COM to output the voltage level input at COM_H. A LOW on SEL1 will cause COM to output the voltage level input at COM_L.
8	N/C	No Connect		Unused Pin.
9	N/C	No Connect		Unused Pin.
10	COM	Common Output	O	If LOGIC ENABLE is LOW, COM will output the voltage input at COM_M. If LOGIC ENABLE is HIGH, COM will output the voltage input at COM_H when SEL1 is HIGH, and will output the voltage input at COM_L when SEL1 is LOW. Refer to Table 3.
11	COM_M	Common System V_{REF}	I	COM_M is a system voltage reference input between 2.5 V and 3.5 V. This may be the system 3.3 V supply.
12	NC	No Connect		Unused Pin.
13	GND	Ground	I	Ground. Nominally 0 V.
14	V4	Output	O	Buffers are rail to rail buffers that can drive high capacitive loads(>16.5 nF). When /SD is LOW, these outputs will be Hi-Z.
15	V3	Output	O	Buffers are rail to rail buffers that can drive high capacitive loads(>16.5 nF). When /SD is LOW or SLP1 and SLP2 = HIGH, these outputs will be Hi-Z.
16	V2	Output	O	Buffers are rail to rail buffers that can drive high capacitive loads(>16.5 nF). When /SD is LOW or SLP1 and SLP2 = HIGH, these outputs will be Hi-Z.
17	V1	Output	O	Buffers are rail to rail buffers that can drive high capacitive loads(>16.5 nF). When /SD is LOW or SLP1 and SLP2 = HIGH, these outputs will be Hi-Z.
18	V0	Output	O	Buffers are rail to rail buffers that can drive high capacitive loads(>16.5 nF). When /SD is LOW, these outputs will be Hi-Z.
19	VDD	Supply	I	Supply voltage. Nominally 5 V.
20	NC	No Connect		Unused Pin.
21	INVERT	Reference Output Select	I	When /SD is HIGH and SLP1 or SLP2 is LOW, then INVERT selects the out put levels on V0 to V4. If INVERT is HIGH, outputs V0 to V4 are connected to reference levels VP0 to VP4 respectively. If INVERT is LOW, outputs V0 to V4 are connected to reference levels VN0 to VN4 respectively. When /SD is HIGH and SLP1& SLP2 are HIGH, V1-V3 are High-Z state, but V0 and V4 are still connected to reference levels VP0 and VP4 when INVERT is High. Outputs V0 and V4 switches to VN0 and VN4 when REV is LOW.

Pin #	Pin	Name	I/O	Description
22	SLP2	Sleep Mode Select	I	When SLP1 and SLP2 are HIGH, the middle three output buffers are shut down, and V1, V2 and V3 are put into Hi-Z states. Other combinations of SLP1 and SLP2 leave the outputs of A1 to A3 fully active.
23	SLP1	Sleep Mode Select	I	When SLP1 and SLP2 are HIGH, the middle three output buffers are shut down, and V1, V2 and V3 are Hi-Z. Other combinations of SLP1 and SLP2 leave the outputs of A1 to A3 fully active.
24	/SD	Global Power Shutdown	I	When /SD is pulled LOW, the chip will be put into the full power down mode. The DACs, resistor ladder network Pre-Amps, and output buffers will all be shut down, and A0 to A4 will be in Hi-Z states. Recovery from full power down to normal operation is within 30 µs.

All digital inputs accept CMOS or TTL logic levels.

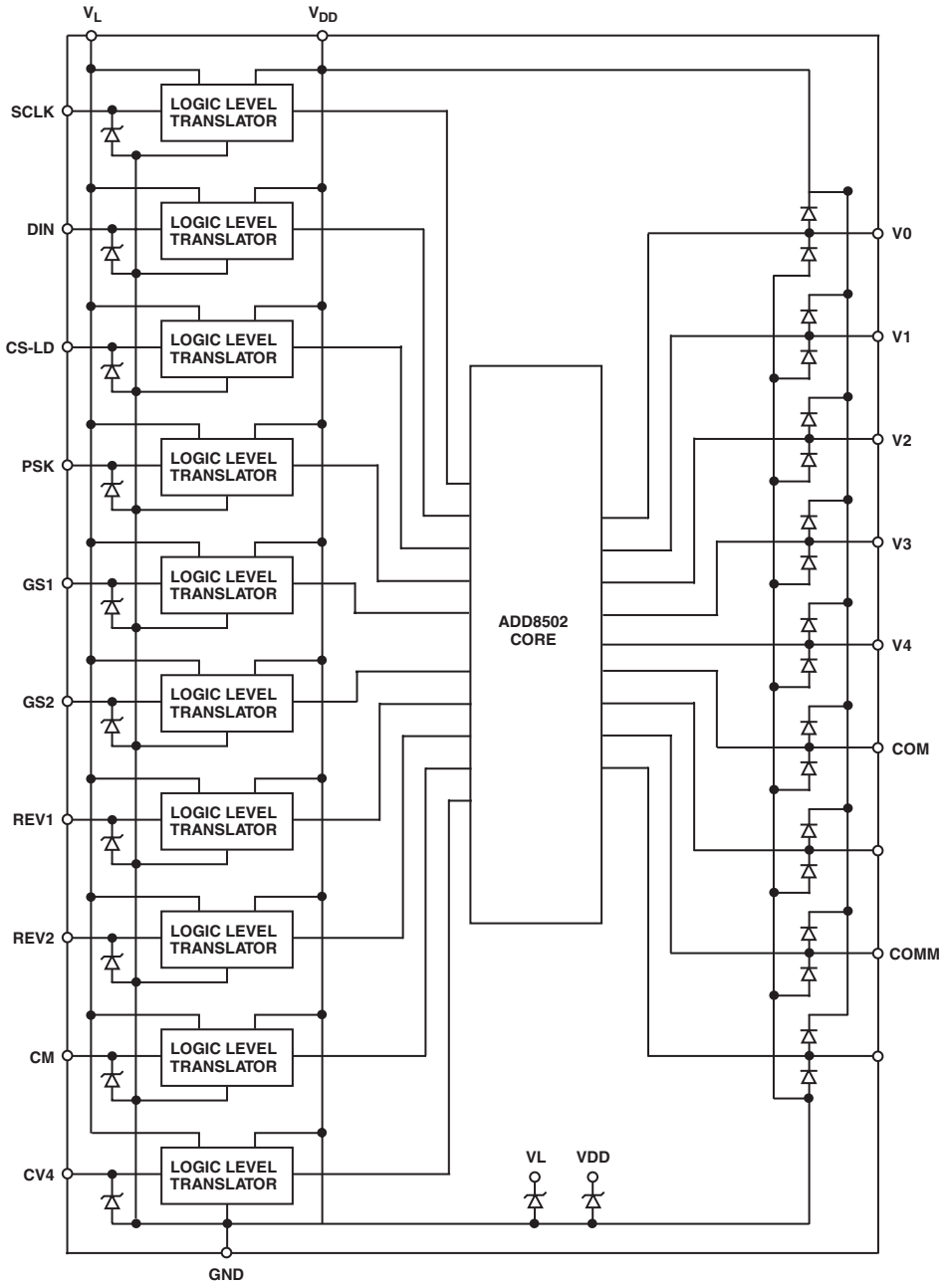


Figure 5. CST ESD & Logic Level Translation Scheme

ADD8502 Description

• The ADD8502 uses logic level translators to convert external logic levels to levels suitable for use in the ADD8502 core.

• The logic level translators are intended to be powered from the same supply voltage as is used to power external logic driving the ADD8502

• V_{DD} may be powered down while normal voltages are present on the V_L & logic input pins.

• V_{DD} and V_L are independent and can be in the range 0 V to 5.5 V

• No damage to the digital inputs will occur with applied voltages up to 7 V (see absolute maximum ratings section of datasheet)

• No current will flow between V_{DD} and V_L under normal operating conditions

• Logic voltages can be present on the logic input pins even if V_L is powered down. Inputs are limited by max supply rating of 7 V.

• Digital input pins have ESD protection connected to GND

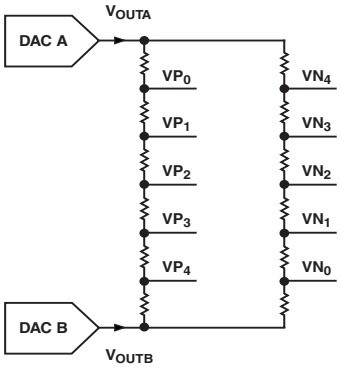
• All other input and output pins have ESD protection connected to GND and V_{DD}

ADD8502-002 MASK OPTION

Table C. Default Power-Up Conditions

DAC Set-Points (0 ≤ D ≤ 1023)			
	Decimal Code	**Voltage**	**Unit**
Upper DAC	943	4.8022	V
Lower DAC	40	0.0977	V
Resistor Tap-Points (0 ≤ X ≤ 512)			
	Tap Point	**Voltage**	**Unit**
VP0	450	4.2325	V
VP1	271	2.5878	V
VP2	203	1.9630	V
VP3	137	1.3565	V
VP4	3	0.1252	V
VN0	31	0.3825	V
VN1	215	2.0732	V
VN2	290	2.7624	V
VN3	367	3.4699	V
VN4	509	4.7747	V

NOTE
Supply voltage = 5 V



Tap Point voltages can be derived from the following equation:

$$Vx = V_{OUTB} + \frac{X}{512}\left[V_{OUTA} - V_{OUTB}\right]$$

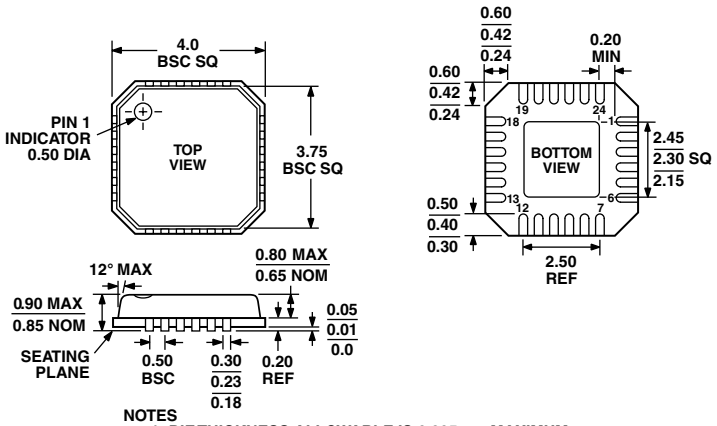
Where: V_{OUTA} and V_{OUTB} can be derived from the transfer functions under the Operation Section of the datasheet.

Note:
The ADD8502 utilizes a single resistor string consisting of 512 individual elements. Both sets of reference voltages ($V_{P0} - V_{P4}$, $V_{N0} - V_{N4}$) are generated from this single string. Two separate resistor networks are shown to demonstrate the tap points, which are changeable b y mask option and completely independent of each other.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

24-Lead LFCSP
(CP Suffix)



NOTES
1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM.
2. DIMENSIONING AND TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
4. PACKAGE WARPAGE IS 0.05mm MAXIMUM.

Tape and Reel Pin #1 Orientation