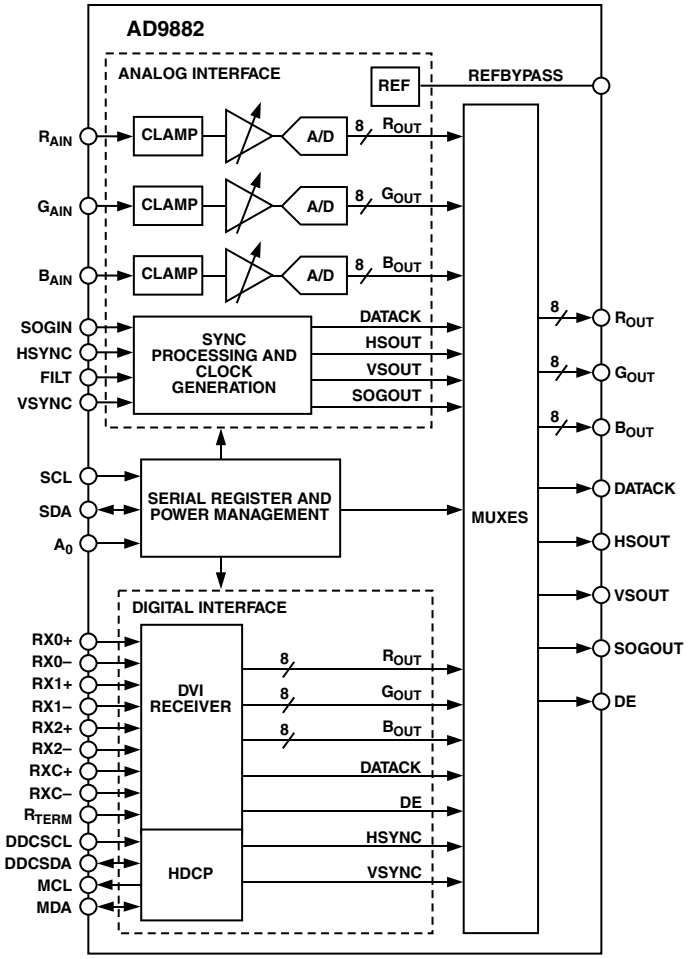
Dual Interface for Flat Panel Displays

Preliminary Technical Data AD9882

FEATURES
Analog Interface
140 MSPS Maximum Conversion Rate
Programmable Analog Bandwidth
0.5 V to 1.0 V Analog Input Range
500 ps p-p PLL Clock Jitter at 140 MSPS
3.3 V Power Supply
Full Sync Processing
Midscale Clamping
4:2:2 Output Format Mode
Digital Interface
DVI 1.0 Compatible Interface
112 MHz Operation
High Skew Tolerance of 1 Full Input Clock
Sync Detect for "Hot Plugging"
Supports High-Bandwidth Digital Content Protection

APPLICATIONS
LCD Monitors and Projectors
Plasma Display Panels
Scan Converter
Microdisplays
Digital TV

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9882 offers designers the flexibility of an analog interface and Digital Visual Interface (DVI) receiver integrated on a single chip. Also included is support for High-Bandwidth Digital Content Protection (HDCP).

Analog Interface

The AD9882 is a complete 8-bit 140 MSPS monolithic analog interface optimized for capturing RGB graphics signals from personal computers and workstations. Its 140 MSPS encode rate capability and full-power analog bandwidth of 300 MHz supports resolutions up to SXGA (1280 × 1024 at 75 Hz).

The analog interface includes a 140 MHz triple ADC with internal 1.25 V reference, a Phase Locked Loop (PLL), and programmable gain, offset, and clamp control. The user provides only a 3.3 V power supply, analog input, and Hsync. Three-state CMOS outputs may be powered from 2.5 V to 3.3 V.

The AD9882's on-chip PLL generates a pixel clock from Hsync. Pixel clock output frequencies range from 12 MHz to 140 MHz. PLL clock jitter is 500 ps p-p typical at 140 MSPS. The AD9882 also offers full sync processing for composite sync and Sync-on-Green (SOG) applications.

Digital Interface

The AD9882 contains a DVI 1.0 compatible receiver and supports display resolutions up to SXGA (1280 × 1024 at 60 Hz). The receiver operates with true color (24-bit) panels and also features an intra-pair skew tolerance of up to one full clock cycle.

With the inclusion of HDCP, displays may now receive encrypted video content. The AD9882 allows for authentication of a video receiver, decryption of encoded data at the receiver, and renewability of that authentication during transmission as specified by the HDCP v1.0 protocol.

Fabricated in an advanced CMOS process, the AD9882 is provided in a space-saving 100-lead LQFP surface-mount plastic package and is specified over the 0°C to 70°C temperature range.

Rev. PrA

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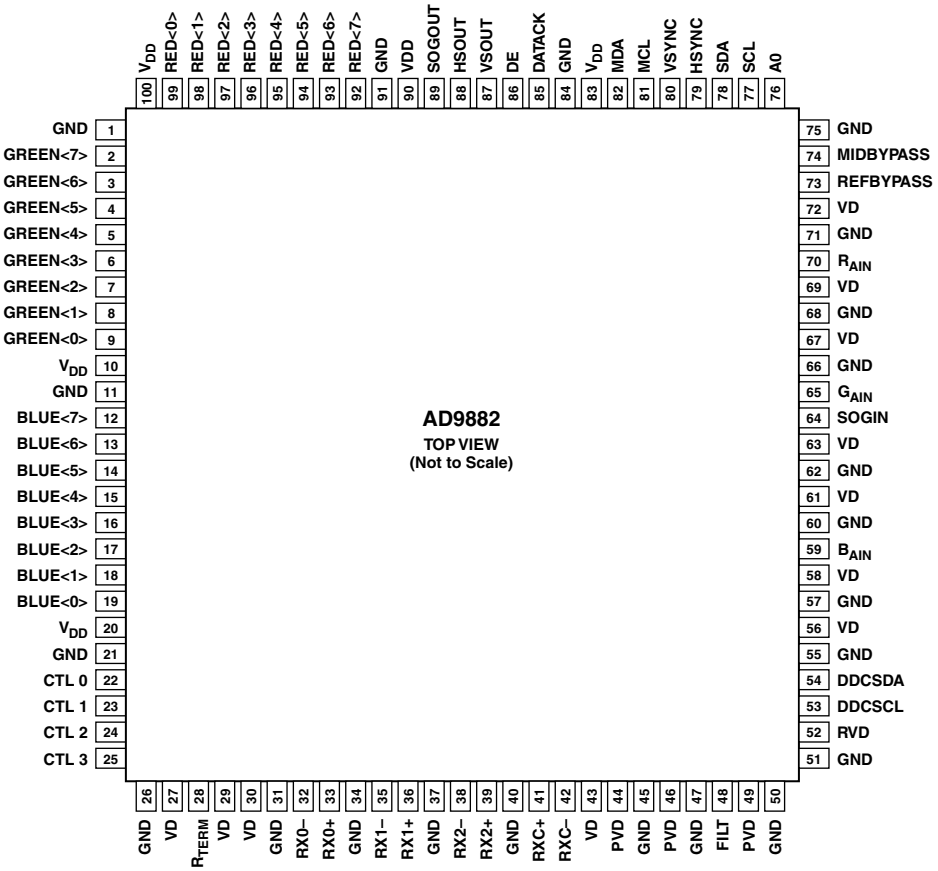
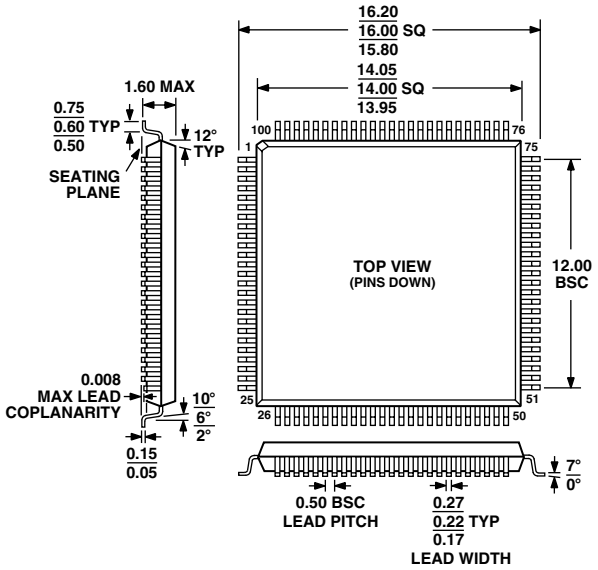
PIN CONFIGURATION



OUTLINE DIMENSIONS

Dimensions shown in millimeters.

100-Lead LQFP Package
(ST-100)



NOTE:
THE ACTUAL POSITION OF EACH LEAD IS WITHIN 0.08 FROM ITS IDEAL POSITION WHEN MEASURED IN THE LATERAL DIRECTION.

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