IF Digitizing Subsystem

Preliminary Technical Data — AD9874

FEATURES

10-300 MHz Input Frequency
Baseband (I/Q) Digital Output
10-270 kHz Output Signal Bandwidth
8.7 dB SSB NF (typ.)
+1.1 dBm IIP3 (typ.; max. bias)
AGCFree Range up to -28 dBm
12 dB Continuous AGC Range
16 dB Front End Attenuator
LO and Sampling Clock Synthesizers
Programmable decimation factor, output format, AGC and synthesizer settings
370 Ω Input Impedance
2.7-3.6 V Supply Voltage
Low Current: 22 mA (typ., max. bias)
48-Pin LQFP package (1.4mm thick)

APPLICATIONS

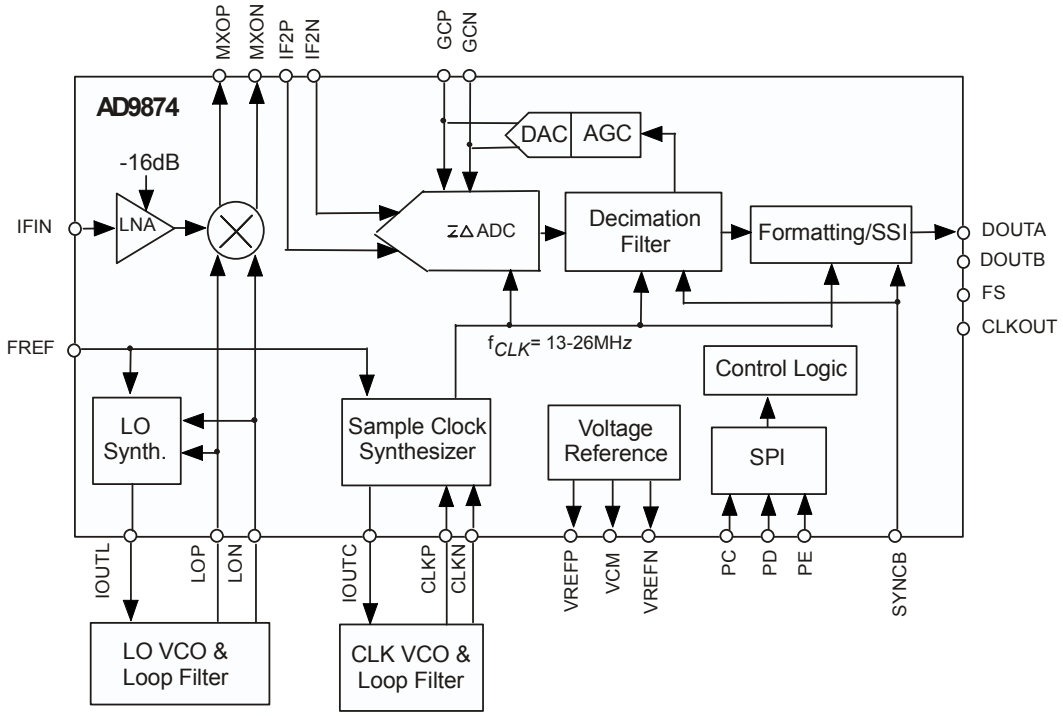
Portable and Mobile Radio Products
Digital UHF/VHF FDMA products
TETRA, APCO25, GSM/EDGE

PRODUCT DESCRIPTION

The AD9874 is a general-purpose IF subsystem which digitizes a low-level 10-300 MHz IF input with a bandwidth up to 270 kHz. The signal chain of the AD9874 consists of a low-noise amplifier, a mixer, a bandpass sigma-delta analog-to-digital converter and a decimation filter with programmable decimation factor. An automatic gain control (AGC) circuit provides the AD9874 with 12 dB of continuous gain adjustment. The high dynamic range and inherent anti-aliasing provided by the bandpass sigma-delta converter allow the AD9874 to cope with blocking signals 80 dB stronger than the desired signal. Auxiliary blocks include clock and LO synthesizers as well as a serial peripheral interface (SPI) port.

The SPI port programs numerous parameters of the AD9874, including the synthesizer divide ratios; the AGC attenuation, attack time, decay time and target signal level; the decimation factor; the output data format; the 16 dB attenuator; as well as selected bias currents. Reducing bias currents allows the user to reduce power consumption at the expense of reduced performance.

FUNCTIONAL BLOCK DIAGRAM



REV. PrB

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AD9874–SPECIFICATIONS

(VDDI = VDDF = VDDA = 3.0 V, VDDC = VDDL = 3.0 V, VDDD = VDDH = 3.0 V, VDDQ =VDDP = 5.0 V, F_{CLK} = 18 MSPS, F_{IF} = 109.65 MHz, F_{LO} = 107.4 MHz, F_{REF} = 16.8 MHz,unless otherwise noted)[1]

Parameter	Temp	Test Level	Min	Typ	Max	Unit
SYSTEM DYNAMIC PERFORMANCE[2]						
SSB Noise Figure @ Min VGA Attenuation[3,4]	Full	IV		8.7		dB
@ Max VGA Attenuation[3,4]	Full	IV		TBD		dB
Dynamic Range w/ AGC Enabled[3,4]	Full	IV		92		dB
IF Input Clip Point @ Max VGA Attenuation[3]	Full	IV		-18		dBm
@ Min VGA Attenuation[3]	Full	IV		-30		dBm
Input Third-Order Intercept (IIP3)	Full	IV		0		dBm
Gain Variation Over Temperature	Full	IV		TBD		dB
LNA + MIXER						
Maximum RF and LO Frequency Range	Full	IV		300		MHz
LNA Input Impedance	25°C	V		370//1.4		Ω//pF
Mixer LO Drive Level	Full	IV	0.30		1	Vp.p.
Mixer LO Input Resistance	25°C	V		1		kΩ
LO SYNTHESIZER						
LO Input Frequency	Full	IV	7.75		300	MHz
LO Input Amplitude	Full	IV	0.3		1.0	V p-p
FREF (Reference) Frequency	Full	IV		0.1		25 MHz
FREF Input Amplitude	Full	VI	0.3		3	V p-p
Minimum Charge Pump Output Current[5]	Full	VI	0.625			mA
Maximum Charge Pump Output Current[5]	Full	VI	5.000			mA
Charge Pump Output Compliance Voltage[6]	Full	VI	0.25		V_{DDP} – 0.25	V
Synthesizer Resolution	Full	IV	6.25			kHz
CLOCK SYNTHESIZER						
CLK Input Frequency	Full	IV	13		26	MHz
CLK Input Amplitude	Full	IV	0.3		V_{DDC}	V p-p
Minimum Charge Pump Output Current[5]	Full	VI	0.625			mA
Maximum Charge Pump Output Current[5]	Full	VI	5.000			mA
Charge Pump Output Compliance Voltage[6]	Full	VI	0.25		V_{DDQ} – 0.25	V
Synthesizer Resolution	Full	IV	2.2			kHz
SIGMA-DELTA ADC						
Resolution	Full	IV	16		24	Bits
Clock Frequency (f_{CLK})	Full	VI	13		26	MHz
Center Frequency	Full	IV		$f_{CLK}/8$		MHz
Passband Gain Variation	Full	IV			0.5	dB
Alias Attenuation	Full	IV	80			dB
GAIN CONTROL						
Programmable Gain Step	Full	VI		16		dB
AGC Gain Range (Continuous)	Full	VI		12		dB
AGC Attack Time (Programmable)	Full	IV	40		7000	µs
OVERALL						
Analog Supply Voltage (VDDA, VDDF, VDDI)	Full	VI	2.7	3.0	3.6	V
Digital Supply Voltage (VDDD, VDDC, VDDL)	Full	VI	2.7	3.0	3.6	V
Interface Supply Voltage[8] (VDDH)	Full	VI	1.8		3.6	V
Charge Pump Supply Voltage (VDDP, VDDQ)	Full	VI	2.7	3.0	5.5	V
Total Current						
High Performance Setting	Full	VI		22		mA
Low Power Mode	Full	VI		18		mA
Standby	Full	VI		0.1		mA
OPERATING TEMPERATURE RANGE						
Basic Functions			–40		+85	°C
Meets All Specifications			–30		+85	°C

NOTES

1 Standard operating mode: high IIP3 setting, synthesizers in normal (not fast acquire) mode, f_{CLK} = 18 MHz, decimation fator = 900, 16-bit Digital Output, 25 pF load on SSI output pins .

2 Includes 0.9 dB Loss of Matching Network

3 AGC w/ DVGA enabled,

4 Measured in 10 kHz bandwidth

5 Programmable in 0.625 mA Steps

6 Voltage span in which LO (or CLK) charge pump output current is maintained within 5% of nominal value of VDDP/2 (or VDDQ/2).

7 Clock VCO Off

8 VDDH must be less than VDDD + 0.5 V

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS

(VDDI = VDDF = VDDA = 3.0 V, VDDC = VDDL = 3.0 V, VDDD = VDDH = 3.0 V, VDDQ = VDDP = 5.0 V, CLK = 18 MSPS, F_{IF} = 109.65 MHz, F_{LO} = 107.4 MHz, unless otherwise noted)[1]

Parameter	Temp	Test Level	Min	Typ	Max	Unit
DECIMATOR						
Decimation Factor[2]	Full	IV	48		960	
Passband Width	Full	IV		50%		f_{CLKOUT}
Passband Gain Variation	Full	IV			1.2	dB
Alias Attenuation	Full	IV	88			dB
SPI-READ OPERATION (see figure 1a)						
PC Clock Frequency	Full	I			10	MHz
PC Clock Period (t_{CLK})	Full	I	100			ns
PC Clock HI (t_{HI})	Full	V	TBD			ns
PC Clock LOW (t_{LOW})	Full	V	TBD			ns
PD Set-up Time (t_{DS})	Full	V		TBD		ns
PD Hold Time (t_{DH})	Full	V		TBD		ns
PE Set-up Time (t_S)	Full	V		TBD		ns
PE Hold Time (t_H)	Full	V		TBD		ns
SPI-WRITE OPERATION (see figure 1b)						
PC Clock Frequency	Full	I			10	MHz
PC Clock Period (t_{CLK})	Full	I	100			ns
PC Clock HI (t_{HI})	Full	V	TBD			ns
PC Clock LOW (t_{LOW})	Full	V	TBD			ns
PD Set-up Time (t_{DS})	Full	V		TBD		ns
PD Hold Time (t_{DH})	Full	V		TBD		ns
PD Data Valid Time (t_{DV})	Full	V		TBD		ns
PD Output Valid to Hi-Z (t_{EZ})	Full	V		TBD		ns
PE Set-up Time (t_S)	Full	V		TBD		ns
SSI (see figure 2b)						
CLKOUT Frequency	Full	IV	f_{CLK}/15		f_{CLK}	
CLKOUT Period (t_{CLK})	Full	VI			38.4	ns
CLKOUT HI (t_{HI})	Full	V		TBD		ns
CLKOUT LOW (t_{LOW})	Full	V		TBD		ns
FS Valid Time (t_V)	Full	V		TBD		ns
DOUT Data Valid Time(t_{DV})Full		V		TBD		ns

1 Standard operating mode: high IIP3 setting, synthesizers in normal (not fast acquire) mode, f_{CLK} = 18 MHz, decimation fator = 300, 25 pF load on SSI output pins: VDDx = 3.0 V.
2. Programmable in Steps of 48 or 60
3. CMOS Output Mode w/ C_{LOAD}= 25pF

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Unit
VDDF, VDDA, VDDC, VDDD, VDDH, VDDL, VDDI	GNDF, GNDA, GNDC, GNDD, GNDH GNDL, GNDI, GNDS	–0.3	+4.0	V
VDDF, VDDA, VDDC, VDDD, VDDH, VDDL, VDDI	VDDR, VDDA, VDDC, VDDD, VDDH, VDDL, VDDI	–4.0	+4.0	V
VDDP, VDDQ	GNDP, GNDQ	–0.3	+6.0	V
GNDF, GNDA, GNDC, GNDD, GNDH GNDL, GNDI, GNDQ, GNDP, GNDS	GNDF, GNDA, GNDC, GNDD, GNDH GNDL, GNDI, GNDQ, GNDP, GNDS	–0.3	+0.3	V
MXOP, MXON, LOP, LON, IFIN, CXIF, CXVL, CXVM	GNDI	–0.3	VDDI + 0.3	V
PC, PD, PE, CLKOUT, DOUTA, DOUTB, FS, SYNCB	GNDH	–0.3	VDDH + 0.3	V
IF2N, IF2P, GCP, GCN	GNDF	–0.3	VDDF + 0.3	V
VREFP, VREFN, RREF	GNDA	–0.3	VDDA + 0.3	V
IOUTC	GNDQ	–0.3	VDDQ + 0.3	V
IOUTL	GNDP	–0.3	VDDP + 0.3	V
CLKP, CLKN	GNDC	–0.3	VDDC + 0.3	V
FREF	GNDL	–0.3	VDDL + 0.3	V
Junction Temperature			150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

THERMAL CHARACTERISTICS

Thermal Resistance

48-Lead LQFP

θ_{JA} = 91°C/W

θ_{JC} = 28°C/W

EXPLANATION OF TEST LEVELS

TEST LEVEL

I. 100% production tested.

II. 100% production tested at 25°C and sample tested at specified temperatures. AC testing done on sample basis.

III. Sample tested only.

IV. Parameter is guaranteed by design and characterization testing.

V. Parameter is a typical value only.

VI. All devices are 100% production tested at 25°C; guaranteed by design and characterization for industrial temperature range.

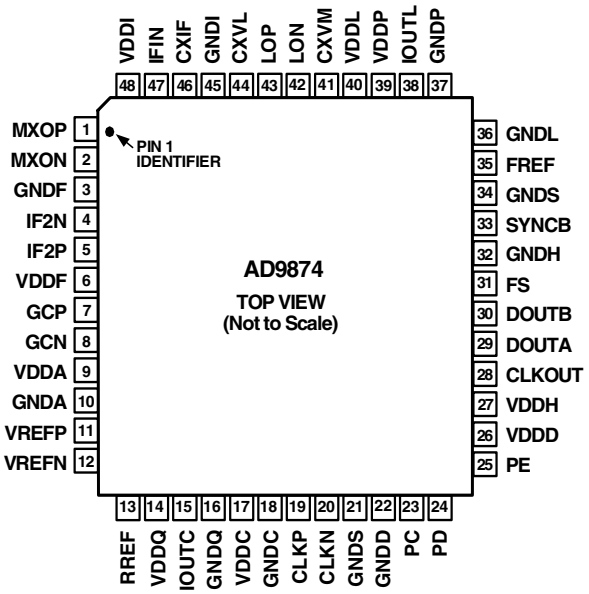
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9874	–40°C to +85°C	48-Lead Thin Plastic Quad Flatpack (LQFP)	ST-48
AD9874EB		Evaluation Board	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9874 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Description	Pin	Mnemonic	Description
1	MXOP	Mixer Output, Positive	25	PE	Enable Input for SPI Port
2	MXON	Mixer Output, Negative	26	VDDD	Positive Power Supply for Internal Digital Functions
3	GNDF	Ground for Front End of ADC	27	VDDH	Positive Power Supply for Digital Interface
4	IF2N	Second IF Input (to ADC), Negative	28	CLKOUT	Clock Output for SSI Port
5	IF2P	Second IF Input (to ADC), Positive	29	DOUTA	Data Output for SSI Port
6	VDDF	Positive Power Supply for Front End of ADC	30	DOUTB	Data Output for SSI Port, Inverted
7	GCP	Filter Capacitor for ADC Full-Scale Control	31	FS	Frame Sync for SSI Port
8	GCN	Full-Scale Control Ground	32	GNDH	Ground for Digital Interface
9	VDDA	Positive Power Supply for ADC Back End	33	SYNCB	Resets SSI and Decimator Counters; Active Low
10	GNDA	Ground for ADC Back End	34	GNDS	Substrate Ground
11	VREFP	Voltage Reference, Positive	35	FREF	Reference Frequency Input for Both Synthesizers
12	VREFN	Voltage Reference, Negative	36	GNDL	Ground for LO Synthesizer
13	RREF	Reference Resistor: Requires 100kΩ to GNDA	37	GNDP	Ground for LO Synthesizer Charge Pump
14	VDDQ	Pos. Power Supply for Clock Synth. Charge Pump	38	IOUTL	LO Synthesizer Charge Pump Output Current
15	IOUTC	Clock Synthesizer Charge Pump Output Current	39	VDDP	Positive Power Supply for LO Synth. Charge Pump
16	GNDQ	Ground for Clock Synthesizer Charge Pump	40	VDDL	Positive Power Supply for LO Synthesizer
17	VDDC	Positive Power Supply for Clock Synthesizer	41	CXVM	External Filter Capacitor; DC Output of LNA
18	GNDC	Ground for Clock Synthesizer	42	LON	LO Input to Mixer and LO Synthesizer, Negative
19	CLKP	Sampling Clock Input/Clock VCO tank, Positive	43	LOP	LO Input to Mixer and LO Synthesizer, Positive
20	CLKN	Sampling Clock Input/Clock VCO tank, Negative	44	CXVL	External Bypass Capacitor for LNA Power Supply
21	GNDS	Substrate Ground	45	GNDI	Ground for Mixer and LNA
22	GNDD	Ground for Digital Functions	46	CXIF	External Capacitor for Mixer V-I Converter Bias
23	PC	Clock Input for SPI port	47	IFIN	First IF Input (to LNA)
24	PD	Data I/O for SPI Port	48	VDDI	Positive Power Supply for LNA and Mixer

DEFINITION OF SPECIFICATIONS/TEST METHODS

SINGLE-SIDEBAND NOISE FIGURE(SSB NF)

Noise Figure(NF) is defined as the degradation in SNR performance (in dB) of an IF input signal after it passes through a component or system. It can be expressed with the following equation:

$$\text{Noise Figure} = 10*\text{LOG}(\text{SNR}_{IN}/\text{SNR}_{OUT})$$

The term SSB is applicable for heterodyne systems containing a mixer. It indicates that the desired signal spectrum resides on only one side of the LO frequency (i.e. single sideband) thus a "noiseless" mixer has a Noise Figure of 3 dB.

The AD9874's SSB noise figure is determined by the following equation:

$$\text{SSB NF} = P_{IN} - (10*\text{LOG}(BW)) - 174 \text{ dB/Hz} - \text{SNR}$$

where... P_{IN} is the input power of an unmodulated carrier
BW is the noise measurement bandwidth
-174 dB/Hz is the thermal noise floor at 293° K
SNR is the measured signal-to-noise ratio in dB of the AD9874.

Note, PIN is set to -85 dBm to minimize any degradation in measured SNR due to phase nosie from the RF and LO signal generators. The IF frequency , CLK frequency, and decimation factorare selected to minimize any "spurious" components falling within the measurement bandwidth. A bandwidth of 10 kHz is used for characterization. See figure 18a and 18b for an indication of how NF varies with BW.

INPUT THIRD-ORDER INTERCEPT (IIP3)

IIP3 is a figure of merit to determine a component or systems succeptibility to intermodulation distortion (IMD) arising from its 3rd order nonlinearities. Two unmodulated carriers at a specified frequency relationship (f_1 and f_2) are injected into a nonlinear system exhibiting 3rd order nonlinearites producing IMD components at $2f_1 - f_2$ and $2f_2-f_1$. IIP3 graphically represents the extrapolated intersection of the carriers input power with the 3rd order IMD component when plotted in dB. The difference in power (Δ in dBc) between the two carriers and the resulting 3rd order IMD components can be determined from the following equation:

$$\Delta = 2*(\text{IIP3} - P_{IN}).$$

DYNAMIC RANGE(DR)

Dynamic Range is the ability to measure a small target input signal (P_{TARGET}) in the presence of a large unwanted interferer signal (P_{INTER}). Typically, the large signal will cause some unwanted characteristic of the component or system under test to degrade thus making it unable to correctly detect the smaller target signal.

The test method for the AD9874 is as follows. The small target signal (an unmodulated carrier) is input at the center of the IF frequency and its power level (P_{TARGET}) is adjusted to achieve an SNR_{TARGET} of 6 dB. The power of the signal is then increased by 3 dB prior to injecting the interferer signal. The offset frequency of the interferer signal is selected such that aliases produced by the decimation filter's response do not fall back within the measurement bandwidth. The interferer signal (also, an unmodulated carrier)is then injected into the input and its power level is increased to the point (P_{INTER}) at which the target signals SNR is reduced to 6 dB. The dynamic range is determined from the following equation:

$$DR = P_{INTER} - P_{TARGET} + \text{SNR}_{TARGET}$$

Note, the AD9874's AGC is enabled for this test.

IF INPUT CLIP POINT

The IF Input Clip Point is defined to be 2 dB *below* the input power level (P_{IN}) which results in " clipping" of the AD9874's ADC. Unlike other linear components which typically exhibit a "soft" compression (characterized by its 1 dB commpression point), ADC's exhibit a "hard" compression once its input signal exceeds its rated maximum input signal range. In the case of the AD9874 which contains a SD ADC, "hard" compression should be avoided since it causes severe SNR degradation.

SERIAL PERIPHERAL INTERFACE (SPI)

The Serial Peripheral Interface (SPI) is a bidirectional serial port. It is used to load configuration information into the registers listed below as well as to read back their contents. Table I provides a list of the registers that may be programmed through the SPI port. Addresses and default values are given in hexadecimal form.

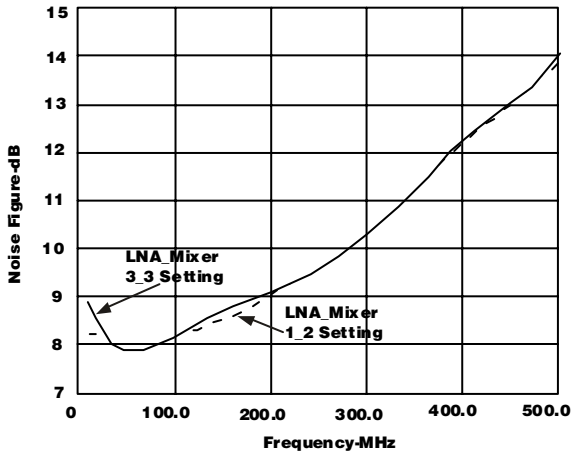
Table I. SPI Address Map

Address (Hex)	Bit Breakdown	Width	Default Value	Name	Description
POWER CONTROL REGISTERS					
0x00	(7:0)	8	0xFF	STBY	Standby Control Bits (REF, LO, CKO, CK, GC, LNAMX, unused, ADC).
0x01	(7:6) (5:4) (3:2) (1:0)	2 2 2 2	0 0 0 0	LNAB MIXB CKOB ADCB	LNA Bias Current (0 = 0.5 mA, 1 = 1 mA, 2 = 2 mA, 3 = 3 mA). Mixer Bias Current (0 = 0.5 mA, 1 = 1.5 mA, 2 = 2.7 mA, 3 = 4 mA). CK Oscillator Bias (0 = 0.25 mA, 1 = 0.35 mA, 2 = 0.53 mA, 3 = 0.85 mA). Do Not Use
0x02	(7:0)	8	0x00	TEST	Factory Test Mode.
AGC					
0x03	(7) (6:0)	1 7	0 0x00	ATTEN AGCG(14:8)	Apply 16 dB attenuation in the front end. AGC Attenuation Setting (7 MSBs of a 15-bit two's-complement word).
0x04	(7:0)	8	0x00	AGCG(7:0)	AGC Attenuation Setting (8 LSBs of a 15-bit two's-complement word). Default corresponds to maximum gain.
0x05	(7:4) (3:0)	4 4	0 0	AGCA AGCD	AGC Attack Time Setting. Default yields 50 Hz raw loop bandwidth. AGC Decay Time Setting. Default is decay time = attack time.
0x06	(7) (6:4) (3) (2:0)	1 3 1 3	0 0 0 0	AGCV AGCO AGCF AGCR	Enable Digital VGA to increase AGC range by 12 dB. AGC Overload Update Setting. Default is slowest update. Fast AGC (Minimizes resistance seen between GCN and GCP). AGC Enable/Reference Level (disabled, 3 dB, 6 dB, 9 dB, 12 dB, 15 dB below clip).
DECIMATION FACTOR					
0x07	(7:5) 4 (3:0)	3 1 4	 0 4	unused K M	 Decimation Factor = 60 x (M + 1), if K=0; 48 x (M + 1), if K=1. Default is decimate-by-300.
LO SYNTHESIZER					
0x08	(5:0)	6	0x00	LOR(13:8)	Reference Frequency Divisor (6 MSBs of a 14-Bit word).
0x09	(7:0)	8	0x38	LOR(7:0)	Reference Frequency Divisor (8 LSBs of a 14-Bit word). Default (56) Yields 300 kHz from f_{REF} = 16.8 MHz.
0x0A	(7:5) (4:0)	3 5	0x5 0x00	LOA LOB(12:8)	"A" Counter (Prescaler Control Counter). "B" Counter MSBs (5 MSBs of a 13-Bit Word). Default LOA and LOB Values Yield 300 kHz from 73.35 MHz–2.25 MHz.
0x0B	(7:0)	8	0x1D	LOB(7:0)	"B" Counter LSBs (8 LSBs of a 13-Bit Word).
0x0C	(6) (5) (4:2) (1:0)	1 1 3 2	0 0 0 3	LOF LOINV LOI LOTM	Enable Fast Acquire. Invert Charge Pump (0 = Pump_Up with IOUTL Sourcing Current). Charge Pump Current in Normal Operation. I_{PUMP} = (LOI + 1) x 0.625 mA. Manual Control of LO Charge Pump (0 = Off, 1 = Up, 2 = Down, 3 = Normal).
0x0D	(5:0)	4	0x0	LOFA(13:8)	LO Fast Acquire Time Unit (6 MSBs of a 14-Bit Word).
0x0E	(7:0)	8	0x04	LOFA(7:0)	LO Fast Acquire Time Unit (8 LSBs of a 14-Bit Word).
CLOCK SYNTHESIZER					
0x10	(5:0)	6	00	CKR(13:8)	Reference Frequency Divisor (6 MSBs of a 14-Bit Word).
0x11	(7:0)	8	0x38	CKR(7:0)	Reference Frequency Divisor (8 LSBs of a 14-Bit Word). Default Yields 300 kHz from f_{REF} =16.8 MHz. Min = 3, Max = 16383.
0x12	(4:0)	5	0x00	CKN(12:8)	Synthesized Frequency Divisor (5 MSBs of a 13-Bit Word).
0x13	(7:0)	8	0x3C	CKN(7:0)	Synthesized Frequency Divisor (8 LSBs of a 13-Bit Word). Default Yields 300 kHz from f_{CLK} = 18 MHz. Min = 3, Max = 8191.

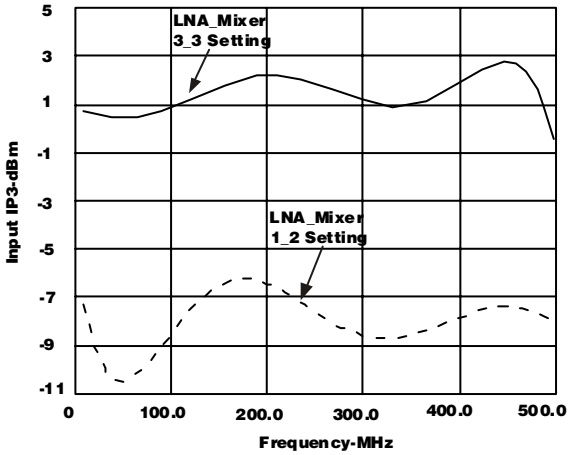
Address (Hex)	Bit Breakdown	Width	Default Value	Name	Description
CLOCK SYNTHESIZER (Continued)					
0x14	(6) (5) (4:2) (1:0)	1 1 3 2	0 0 0 3	CKF CKINV CKI CKTM	Enable Fast Acquire. Invert Charge Pump (0 = Pump_Up IOUTC Sources Current). Charge Pump Current in Normal Operation. I_{PUMP} = (CKI + 1) ∞ 0.625 mA. Manual Control of CLK Charge Pump (0 = Off, 1 = Up, 2 = Down, 3 = Normal).
0x15	(5:0)	6	0x0	CKFA(13:8)	CK Fast Acquire Time Unit (6 MSBs of a 14-Bit Word).
0x16	(7:0)	8	0x04	CKFA(7:0)	CK Fast Acquire Time Unit (8 LSBs of a 14-Bit Word).
SSI CONTROL					
0x18	(7:0)	8	0x12	SSICRA	SSI Control Register A. See Table II. (Default is FS and CLKOUT Three-Stated.)
0x19	(7:0)	8	0x07	SSICRB	SSI Control Register B. See Table II. (Default is CMOS mode, 16-bit data, max. drive strength)
0x1A	(3:0)	4	1	SSIORD	Output Rate Divisor. $f_{CLKOUT} = f_{CLK}/SSIORD$.
ADC TUNING					
0x1C	(1) (0)	1 1	0 0	TUNE_LC TUNE_RC	Perform Tuning on the LC portion of the ADC (cleared when done) Perform Tuning on the RC portion of the ADC (cleared when done)
0x1D	(2:0)	3	0	CAPL1(2:0)	Coarse Capacitance Setting for LC Tank (LSB is 25 pF, differential)
0x1E	(5:0)	6	0x00	CAPL0(5:0)	Fine Capacitance Setting for LC Tank (LSB is 0.4 pF, differential)
0x1F	(7:0)	8	0x00	CAPR	Capacitance Setting for RC Resonator (+64 LSB's of fixed capacitance)
TEST REGISTERS AND SPI PORT READ ENABLE					
0x37-0x39	(7:0)	8	0x00	TEST	Factory Test Mode.
0x3A	(7:4, 2:0) (3)	7 1	0x0 0	TEST SPIREN	Factory Test Mode. Enable Read from SPI Port.
0x3B	(7:4, 2:0) (3)	7 1	0x0 0	TEST TRI	Factory Test Mode. Tri-state DOUTB
0x3C–0x3E	(7:0)	1	0x00	TEST	Factory Test Mode.
0x3F	(7:0)	8	Subject to Change	ID	Revision ID (Read Only) A write of 0x99 to this register is eqivalent to a power-on Reset.

Typical Performance Characterization Curves

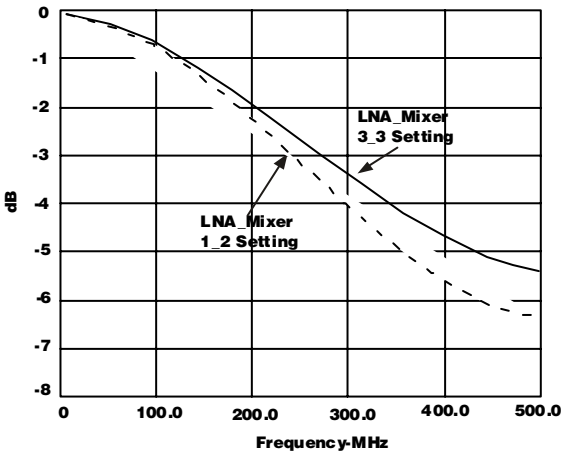
(VDDI = VDDF = VDDA = 3.0 V, VDDC = VDDL = 3.0 V, VDDD = VDDH = 3.0 V, VDDQ = VDDP = 5.0 V, CLK = 18 MSPS, T_A=25C^o , unless otherwise noted)[1]



TPC1a. Noise Figure vs. Frequency



TPC1b. Input IP3 vs. Frequency



TPC1c. IF Input_Frequency Response

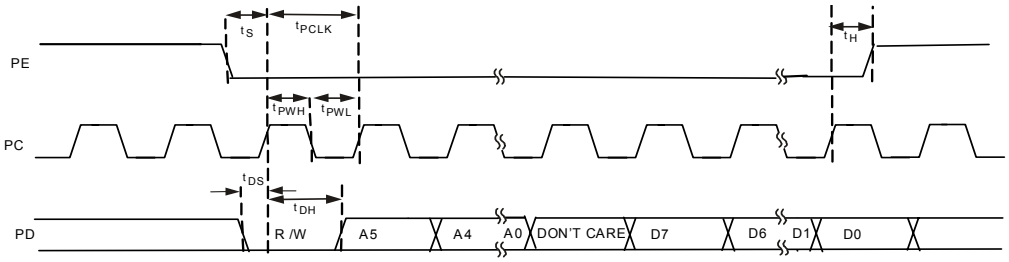


Figure 1a. SPI Write Operation Timing

SERIAL PORT INTERFACE (SPI)

The serial port of the AD9874 has 3- or 4-wire SPI capability allowing either interface read/write access to all registers that configure the devices internal parameters. The default 3- wire serial communication port consists of a clock (PC), periperal enable (PE), and a bidirectional data (PD) signal. The 4-wire SPI interface can be enabled by setting the MSB of the SSICRB register(Reg. 0x19, Bit 7) resulting in the output data also appearing on the DOUTB pin. Note, the default power-up state sets DOUTB low thus bus contention is possible for systems sharing the SPI output line. To avoid any bus contention, the DOUTB pin can be three-stated by setting the 4th control bit in the three-state bit (Reg 0x3B, Bit 3). This bit can than be toggled to gain access to the shared SPI output line.

An 8-bit instruction header must accompany each read and write operation. Only the write operation supports an auto-increment mode allowing the entire chip to be configured in a single write operation. The instruction header is shown in Table I. It includes a read/not-write indicator bit, 6 address bits and a Don't Care bit. The data bits immediately follow the instruction header for both read and write operations. Note, address and data are given MSB first.

MSB LSB

I7	I6	I5	I4	I3	I2	I1	I0
R/W	A5	A4	A3	A2	A1	A0	X

Table I. Instruction header information

Figure 1a illustrates the timing requirements for a write operation to the SPI port. After the peripheral enable (PE) signal goes low, data (PD) pertaining to the instruction header is read on the *rising edges* of the clock (PC). To initiate a write operation, the read/not-write bit is set low. After the instruction header is read, the eight data bits pertaining to the specified register are shifted into the data pin (PD) on the *rising edge* of the next eight clock cycles. PE stays low during the operation and goes high at the end of the transfer. If PE rises before the eight clock cycles have passed, the operation is aborted.

If PE stays low for an additional eight clock cycles, the destination address is incremented and another eight bits of data are shifted in. Again, should PE rise early, the current byte is ignored. By using this implicit addressing mode, the entire chip can be configured with a single write operation. Registers identified as being subject to frequent updates, namely those associated with power control and AGC operation, have been assigned adjacent addresses to minimize the time required to update them. Note, multibyte registers are "big-endian" (the most significant byte has the lower address) and are updated when a write to the least significant byte occurs.

Figure 1b illustrates the timing for a read operation to the SPI port. Although the AD9874 does not require read access for proper operation, it is often useful in the product development phase or for system authentification. Note, the read-back enable bit (Reg. 0x3A, Bit 3) *must* be set for a read operation with a 3-wire SPI interface. After the peripheral enable (PE) signal goes low, data (PD) pertaining to the instruction header is read on the *rising edges* of the clock (PC). A read operation occurs if the read/not-write indicator is set high. After the address bits of the instruction header are read, the eight data bits pertaining to the specified register are shifted out of the data pin (PD) on the *falling edges* of the next eight clock cycles. If the 4-wire SPI interface is enabled, the eight data bits will also appear on the DOUTB pin with the same timing relationship as those appearing at PD. After the last data bit is shifted out, the user should return PE high causing PD to become tristated and return to its normal status as an input pin. Since the auto-increment mode is not supported for read operations, an instruction header is

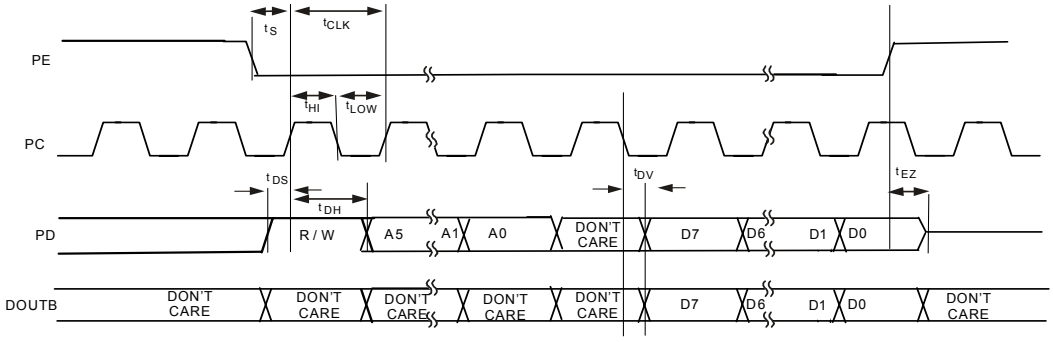


Figure 1b. SPI Read Operation Timing

required for each register read operation and PE must return high before initiaiting the next read operation.

SYNCHRONOUS SERIAL INTERFACE (SSI)

The AD9874 provides a high degree of programability of its SSI output data format, control signals, and timing parameters to accomodate various digital interfaces. In a 3-wire digital interface, the AD9874 provides a frame sync signal (FS), a clock output (CLKOUT), and serial data stream (DOUTA) signal to the host device. In a 2-wire interface, the frame sync information is *embedded* into the data stream thus only a CLKOUT and DOUTA output signal are provided to the host device.

The primary output of the AD9874 is the converted signal available from the SSI port as a serial bit stream contained within a frame. The output frame rate is equal to the modulator clock frequency (f_{CLK}) divided by the digital filter's decimation factor that is programmed in the decimator register (0x07). The bit stream consists of an I word followed by a Q word, where each word is either 24 or 16 bits long and is given MSB first in *2's-complement* form. Two optional bytes may also be included within the SSI frame following the Q word. One byte contains the AGC attenuation and the other byte contains both a count of modulator reset events and an estimate of the signal amplitude relative to full-scale. Figure 3 illustrates the structure of the SSI data frames in a number of SSI modes.

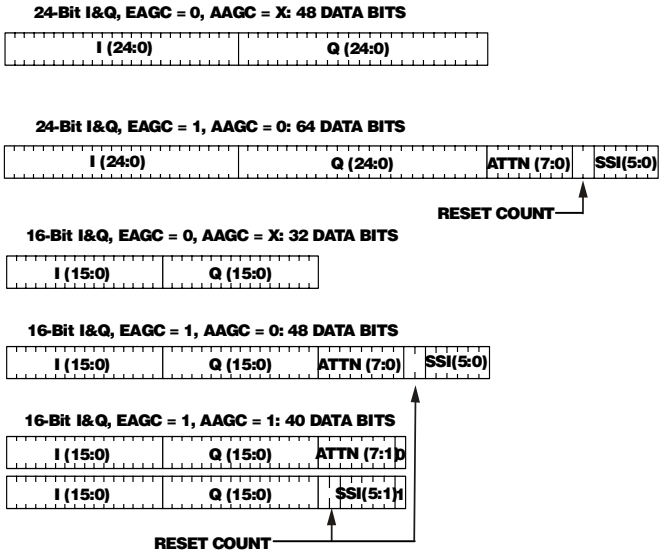


Figure 3. SSI Frame Structure

The two optional bytes are output if the EAGC bit of SSICRA is set. The first byte contains the 8-bit attenuation setting (0 = no attenuation, 255 = 24 dB of attenuation) setting while the second byte contains a 2-bit reset field and 6-bit signal signal field. The reset field contains the number of modulator reset events since the last report, saturating at 3. The signal strength field is a *linear* estimate of the signal strength at the output of the first decimation stage; 60 corresponds to a full-scale signal.

The two optional bytes follow the I and Q data as a 16-bit word provided the AAGC bit of SSICRA is not set. If the AAGC bit is set, the two bytes follow the I and Q data in an *alternating* fashion. In this "alternate AGC data" mode, the LSB of the byte containing the AGC attenuation is a 0 while the LSB of the byte containing reset and signal strength information is always a 1.

In a 2-wire interface, the embedded frame sync bit (EFS) within the SSICRA register is set to one. In this mode, the framing information is embedded in the data stream with each eight bits of data surrounded by a start bit (low) and a stop bit (high), and each frame ends with at least 10 high bits. FS remains either low or in a high Z state(default) depending on the state of the SFST bit. Other control bits can be used to invert the frame sync (SFSI), to delay the frame sync pulse by one clock period (SLFS), to invert the clock (SCKI), or to set the clock (SCKT) to a high Z state. Note that if EFS is set, SLFS is a don't care.

The SSI control registers are SSICRA, SSICRB, and SSIORD. Table II shows the different bit fields associated with the SSICRA and SSICRB registers. The SSIORD register controls the output bit rate, f_{CLKOUT}.

Name	Width	Default	Description
SSICRA (ADDR = 0x18)			AAGC | EAGC | EFS | SFST | SFSI | SLFS | SCKT | SCKI
AAGC	1	0	Alternate AGC Data Bytes
EAGC	1	0	Embed AGC Data
EFS	1	0	Embed Frame Sync
SFST	1	1	Three-State Frame Sync
SFSI	1	0	Invert Frame Sync
SLFS	1	0	Late Frame Sync (1 = Late, 0 = Early)
SCKT	1	1	Three-State CLKOUT
SCKI	1	0	Invert CLKOUT
SSICRB (ADDR = 0x19)			DW | DS_2 | DS_1 | DS_0
DW	1	0	I/Q data word width (0=16 bit, 1-24 bit) Automatically 16-bit when the AGCV=1
DS	3	7	FS, CLKOUT, and DOUT Drive Strength

Table II. SSI Control Registers

The output bit rate (f_{CLKOUT}) of the serial bit stream can be set to equal the modulator clock frequency (f_{CLK}) or an integer fraction of it. It is equal to f_{CLK} divided by the contents of the SSIORD register. Note, f_{CLKOUT} should be chosen such that it does not introduce harmful spurs within the passband of the target signal. Users must verify that the output bit rate is sufficient to accommodate the required number of bits per frame for a selected word size and decimation factor. Idle (high) bits are used to fill out each frame.

DW	EAGC	EFS	AAGC	#Bits per Frame
0 (16-bit)	0	0	NA	32
	0	1	NA	49
	1	0	0	48
	1	0	1	40
	1	1	0	48
	1	1	1	40
1 (24-bit)	0	0	NA	48
	0	1	NA	69
	1	0	0	64
	1	0	1	56
	1	1	0	89
	1	1	1	79

Table II. Number of Bits per Frame for different SSICR Settings

The *maximum* SSIORD setting can be determined by the following equation:

(1) SSIORD $\leq$ *TRUNC*{(Dec. Factor)/(# of Bits per Frame)}

whereSSIORD is the truncated interger value.

Table III lists the number of bits within a frame for 16-bit and 24-bit output data formats for all of the different SSICR settings. Note, the frame lengthst with embedded frame sync (EFS = 1) assume at least 10 idle bits are desired. The decimation factor is determined by the contents of Reg 0x07.

An example helps illustrate how the *maximum* SSIORD setting is determined. Suppose a users selects a decimation factor of 600 (Reg 0x07, K=0, M=9) and prefers a 3-wire interface (EFS=0) containing 24-bit data (DW=1) with non-alternating embedded AGC data included (EAGC=1, AAGC=0). Referring to Table II, each frame will consist of 64 data bits. Using equation (1), the *maximum* SSIORD setting is 9 (=*TRUNC*(600/64). Hence, the user can select any SSIORD setting between 1 and 9.

Figure 2a illustrates the output timing of the SSI port for several SSI control register settings while Figure 2b shows the associated timing parameters. In the default mode of operation, data is shifted out on rising edges of CLKOUT after a pulse equal to a clock period is output from the frame sync (FS) pin. As described above, the output data consists of a 16(or 24) bit I sample followed by a 16 (or 24) bit Q sample plus two optional bytes containing AGC and status information.

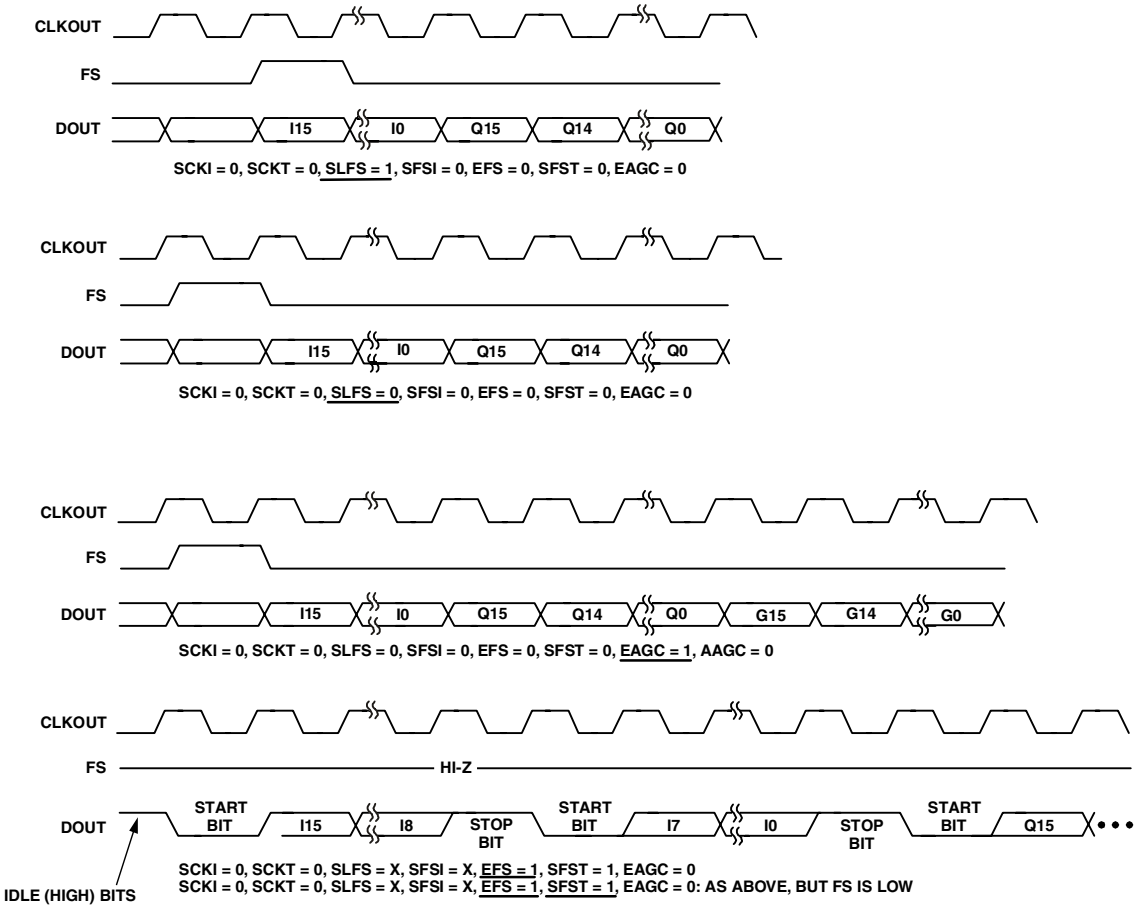


Figure 2a. SSI Timing for Several SSICR Settings

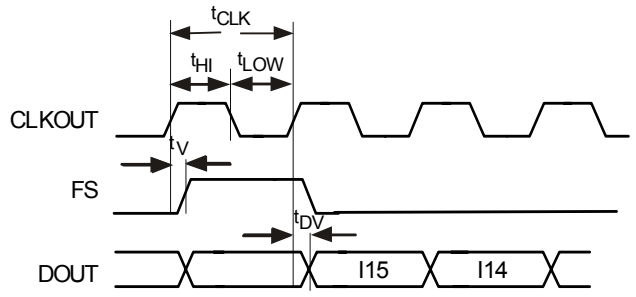


Figure 2b. Timing Parameters for SSI Timing[1]

The AD9874 also provides the means for controlling the switching characteristics of the digital output signals via the DS (drvie strength) field of SSICRB. This feature is useful in limiting spurious emissions from the digital output that may ultimately couple back into the passband of the desired signal. Table VII. lists the typical output rise/fall times as a function of DS for a 25 pF load. Rise/fall times for other capacitor loads can be determined by multiplying the typical values presented in Table VII. by a scaling factor equal to the desired capacitive load divided by 25 pF.

DS	typ. (ns)
0	31
1	16
2	11
3	8.5
4	7
5	6
6	5
7	4.5

Table VII. Typical Rise/Fall times (+/-25 %) with a 25 pF capacitive load for each DS setting

SYNCHRONIZATION

Applications such as receiver diversity employing more than one AD9874 device may desire synchronization of the digital output data. SYNCB can be used for this purpose and applied upon system initiation. It is an active-low signal which clears the clock counters in both the decimation filter and the SSI port. The counters in the clock synthesizers are not reset, as it is presumed that the CLK signals of multiple chips would be connected together. SYNCB also clears the registers in the decimation filter and resets the modulator. As a result, valid data representative of the input signal will be available once the digital filters have been flushed.

Figure 4. shows the timing relationship between SYNCB and the SSI port's CLKOUT and FS signals. SYNCB is an asynchronus active-low signal that must remain low for at least half an *input* clock period (i.e $1/(2*f_{CLK})$). CLKOUT returns high while FS remains low upon SYNCB going low. CLKOUT will become active within 1 to 2 output clock periods upon SYNCB returning high. FS will reappear several output clock cycles latter depending on the digital filter's decimation factor as well as the SSIORD setting. To verify proper synchronization, the FS signals of the multiple AD9874 devices should be monitored.

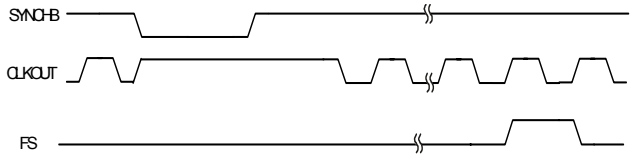


Figure 4. SYNCB Timing

POWER CONTROL

To allow power consumption to be minimized, the AD9874 possesses numerous SPI-programmable power-down and bias control bits.

The AD9874 powers up with all of its functional blocks placed into a stand-by state (i.e. STBY register default is 0xFF). Each major block may then be powered up by writing a 0 to the appropriate bit of the STBY register. This scheme provides the greatest flexibility for configuring the IC to a specific application as well as for tailoring the IC's power-down and wake-up characteristics. Table VIII summarizes the function of each of the STBY bits. Note, when all the blocks are in standby, the master reference circuit is also put into standby and thus the current is reduced by a further 0.4 mA.

The AD9874 also allows control over the bias current in several key blocks. The effects on current consumption and system performance are described in the section dealing with the affected block.

Table VIII. Standby Control Bits

STBY Bit	Effect	Current Reduction (mA)[2]	Wake-Up Time (ms)
7:REF	Voltage Reference Off; all biasing shut down.	TBD	<0.1 (C_{REF} =4.7 nF)
6:LO	LO Synthesizer Off, IOUTL tristate.	TBD	Note 3
5:CKO	Clock Oscillator Off.	TBD	Note 3
4:CK	Clock Synthesizer Off, IOUTC tristate. Clock Buffer Off if ADC is off.	TBD	Note 3
3:GC	Gain Control DAC Off.	TBD	De-
pends	GCP, GCN tristate.		on C_{GC}
2:LNAMX	LNA and Mixer Off. CXVM, CXVL, CXIF tristate.	TBD	TBD
1:Unused			
0:ADC	ADC Off; Clock Buffer off if CK synth. off; VCM tristate; Clock to the digital filter halted; Digital outputs static.	TBD	<0.1

NOTES

[1] Timing parameters also apply to inverted CLKOUT or FS modes with t_{DV} relative to falling edge of CLK and/or FS

[2] When all blocks are in standby, the master reference circuit is also put into standby and thus the current is reduced by a further 0.4 mA.

[3] Wake-up time is dependent on programming and/or exteranal components.

LO SYNTHESIZER

The LO synthesizer shown in figure 5 is a fully programmable PLL capable of 6.25 kHz resolution at input frequencies up to 300 MHz and reference clocks of up to 25 MHz. It consists of a low-noise digital Phase-Frequency Detector (PFD), a variable output current charge pump (CP), a 14-bit reference divider, programmable A and B counters and a dual-modulus 8/9 prescaler. The A (3-bit) and B (13-bit) counters, in conjunction with the dual 8/9 modulus prescaler , implement an N divider with N = 8 x B + A. In addition, the 14-bit reference counter (R Counter), allows selectable input reference frequencies, f_{REF}, at the PFD input. A complete PLL (Phase-Locked Loop) can be implemented if the synthesizer is used with an external loop filter and VCO (Voltage Controlled Oscillator).

The A, B, and R counters can be programmed via the following registers: LOA, LOB, and LOR . The charge pump output current is programmable via the LOI register from 0.625 mA to 5.0 mA using the following equation:

(1) IPUMP = (LOI+1) x 0.625mA .

An on-chip lock detect function (enabled by the LOF bit) automatically increases the output current for faster settling during channel changes. The synthesizer may also be disabled using the LO standby bit located in the STBY register .

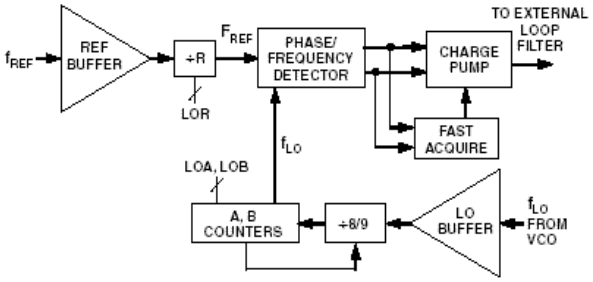


Figure 5. AD9874 LO Synthesizer

The LO (and CLK) Synthesizer works in the following manner. The externally supplied reference frequency, F_{REF}, is buffered and divided by the value held in the R counter. The internal f_{ref} is then compared to a divided version of the VCO frequency, f_{lo}. The Phase/Frequency detector provides UP and DOWN pulses whose width vary depending upon the difference in phase and frequency of its two input signals. The UP/DOWN pulses control the Charge Pump, making current available to charge the external low-pass loop filter when there is a discrepancy between the inputs of the PFD. The output of the low pass filter feeds an external VCO whose output frequency, F_{LO}, is driven such that its divided down version, f_{lo} , matches that of f_{ref} thus closing the feedback loop.

The synthesized frequency is related to the reference frequency and the LO register contents as follows:

(2) F_{LO} = (8 x LOB + LOA)/LOR x F_{REF}

Note, the minimum allowable value in the LOB register is 3 and its value must always be greater than that loaded into LOA . The stability, phase noise, spur performance, and transient response of the AD9874's LO (and CLK) synthesizers are determined by the external loop filter, the VCO, the N-divide factor, and the reference frequency, f_{REF}. A good overview on the theory and practical implementation of PLL sythesizers (featured as a 3-part series in Analog Dialogue within volumes 33-03, 33-05, and 33-07) can be found at http://www.analog.com/library/analogDialogue/archives/33-0X.

An example may help illustrate how the values of LOA, LOB, and LOR can be selected. Consider an application employing a 13 MHz crystal oscillator (i.e. F_{REF}= 13 MHz) with the requirement that f_{REF}=100 kHz and F_{LO}=143 MHz (i.e. high-side injection with IF=140.75 MHz and F_{SAMPLE}=18 MSPS). LOR is selected to be 130 such that f_{REF}=100 kHz. The N-divider factor is 1430 which can be realized by selecting LOB=178 and LOA=6.

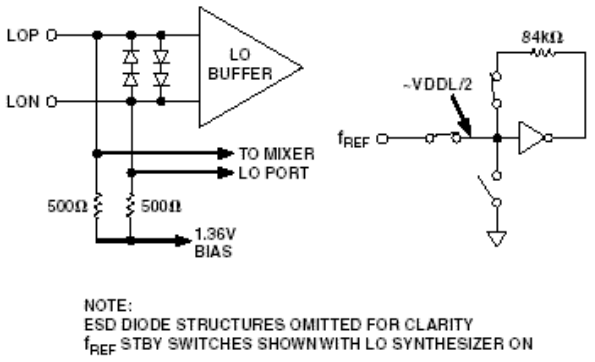


Figure 6.0 Equivalent Input of LO and REF Buffers

Figure 6.0. shows the equivalent input structures of the synthesizers' LO and REF buffers (excluding the ESD structures). The LO input is fed to the LO synthesizers buffer as well as the AD9874's mixer's LO port. Both inputs are self-biasing and thus tolerate AC coupled inputs. The LO input can be driven with a single-ended or differential signal. Single-ended DC coupled inputs should ensure sufficient signal swing above and below the common-mode bias of the LO and REF buffers (i.e. 1.38 V and VDDL/2).

Fast Acquire Mode

The fast acquire circuit attempts to boost the output current when the phase difference between the divided-down LO (i.e. f_{lo}) and the divided-down reference frequency (i.e. f_{ref}) exceeds the threshold determined by the LOFA register. The LOFA register specifies a divisor for the F_{REF} signal, and it is the period (T) of this divided-down clock that specifies the time interval which controls the fast acquire algorithm.

Assume for the moment that the nominal charge pump current is at its lowest setting (i.e. LOI=0) and denote this minimum current by I_0. When the output pulse from the phase comparator exceeds T, the output current for the next pulse is $2I_0$; when the pulse is wider than 2T, the output current for the next pulse

is $3I_0$, and so forth, up to eight times the minimum output current. If the nominal charge pump current is more than the minimum value (i.e. LOI > 0), the preceding rule is only applied if it results in an increase in the instantaneous charge pump current. If the charge pump current is set to its lowest value (LOI = 0) and the fast acquire circuit is enabled, the instantaneous charge pump current will never fall below $2I_0$, even when the pulse width is less than T. Thus the charge pump current when fast acquire is enabled is given by

(3) $I_{PUMP\text{-}FA} = I_O * (1 + \max(1, LOI, Pulse\_Width/T))$.

The recommended setting for LOFA is LOR/16. Choosing a larger value for LOFA will increase T. Thus, for a given phase difference between the LO input and the FREF input, the instantaneous charge pump current will be less than that available for a LOFA value of LOR/16. Similarly, a smaller value for LOFA will decrease *T*, making more current available for the same phase difference. In other words, a smaller value of LOFA will enable the synthesizer to settle faster in response to a frequency hop than will a large LOFA value. Care must be taken to choose a value of LOFA which is large enough (values greater than 4 recommended) to prevent the loop from oscillating back and forth in response to a frequency hop.

Table IV. SPI Registers associated with LO Synthesizer

Address (Hex)	Bit Breakdown	Width	Default Value	Name
0x00	(7:0)	8	0xFF	STBY
0x08	(5:0)	6	0x00	LOR(13:8)
0x09	(7:0)	8	0x38	LOR(7:0)
0x0A	(7:5)	3	0x5	LOA
	(4:0)	5	0x00	LOB(12:8)
0x0B	(7:0)	8	0x1D	LOB(7:0)
0x0C	(6)	1	0	LOF
	(5)	1	0	LOINV
	(4:2)	3	0	LOI
	(1:0)	2	0	LOTM
0x0D	(3:0)	4	0x0	LOFA(13:8)
0x0E	(7:0)	8	0x04	LOFA(7:0)

CLOCK SYNTHESIZER

The clock synthesizer is a fully programmable integer-*N* PLL capable of 2.2 kHz resolution at clock input frequencies up to 18 MHz and reference frequencies up to 25 MHz. It is similar to the LO synthesizer described previously in figure 4 with the following exceptions:

-it does not include an 8/9 prescaler nor an A counter

-it includes a negative-resistance core which when used in conjunction with an external LC tank and varactor serves as the VCO.

The 14-bit reference counter and 13-bit N-divider counter can be programmed via the following registers: CKR and CKN .

The charge pump current is programmable via the CKI register from 0.625 mA to 5.0 mA using the following equation:

(4) $I_{PUMP} = (CKI+1) \times 0.625mA$.

The fast acquire subcircuit of the charge pump is controlled by the CKFA register in the same manner as the LO synthesizer is controlled by the LOFA register. An on-chip lock detect function (enabled by the CKF bit automatically increases the output current for faster settling during channel changes. The synthesizer may also be disabled using the CKOB standby bit located in the STBY register .

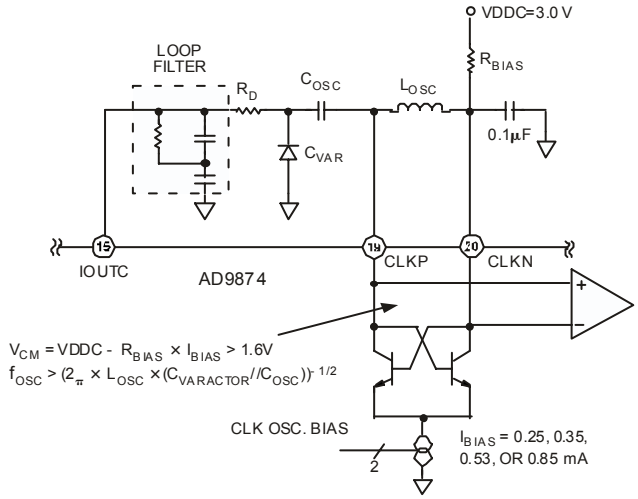


Figure 7.0 External loop filter, varactor and L-C tank are required to realize a complete Clock Synthesizer

The AD9874 clock synthesizer circuitry includes a negative-resistance core so that only an external LC tank circuit with a varactor is needed to realize a voltage controlled oscillator (VCO). Figure 7.0 shows the external components required to complete the clock synthesizer along with the equivalent input of the CLK input. The resonant frequency of the VCO is approximately determined by L_{OSC} and the series equivalent capacitance of C_{OSC} and C_{VAR}. As a result, L_{OSC} , C_{OSC} and C_{VAR} should be selected to provide sufficient tuning range to ensure proper locking of the clock synthesizer The bias , I_{BIAS}, of the negative-resistance core has four programmable settings. Lower equivalent Q of the L-C tank circuit may require a higher bias setting of the negative-resistance core to ensure proper oscillation. R_{BIAS} should be selected such that the common-mode voltage at CLKP and CLKN is approximately 1.6 V. The synthesizer may be disabled via the CK standby bit to allow the user to employ an external synthesizer and/or VCO in place of those resident on the IC.

Table V. SPI Registers associated with CLK Synthesizer

Address (Hex)	Bit Breakdown	Width	Default Value	Name
0x00	(7:0)	8	0xFF	STBY
0x01	(3:2)	2	0	CKOB
0x10	(5:0)	6	00	CKR(13:8)
0x11	(7:0)	8	0x38	CKR(7:0)
0x12	(4:0)	5	0x00	CKN(12:8)
0x13	(7:0)	8	0x3C	CKN(7:0)
0x14	(6) (5) (4:2) (1:0)	1 1 3 1	0 0 0 0	CKF CKINV CKI CKTM
0x15	(3:0)	4	0x0	CKFA(13:8)
0x16	(7:0)	8	0x04	CKFA(7:0)

IF1 LNA/MIXER

The AD9874 contains a single-ended LNA followed by "Gilbert-type" active mixer which is shown in figure 8 along with the required external components. The LNA uses negative shunt feedback to set its input impedance at the IFIN pin thus making it dependent on the LNA bias setting and input frequency. It can be modeled as approximately 370 Ω // 1.4pF (+/-20%) for the higher bias settings below 100 MHz. Figure 9a and 9b shows the equivalent input impedance vs. frequency characteristics of the AD9874 with all the LNA bias settings. The increase in shunt resistance vs. frequency can be attributed to the reduction in bandwidth, hence amount of negative feedback, of the LNA. Note, the input signal into IFIN should be ac coupled via a 10 nF capacitor since the LNA input is self biasing.

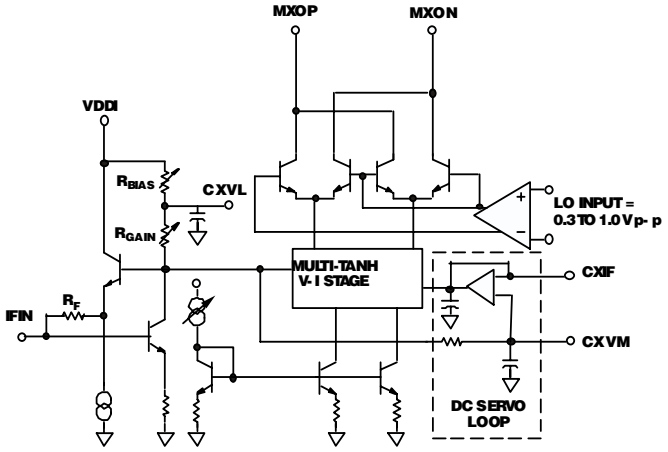


Figure 8. Simplified Schematic of AD9874's LNA/Mixer

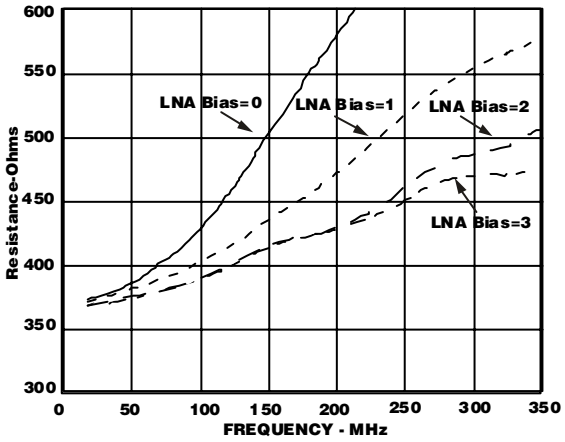


Figure 9a. Shunt Input Resistance vs. frequency of the AD9874's IF1 Input

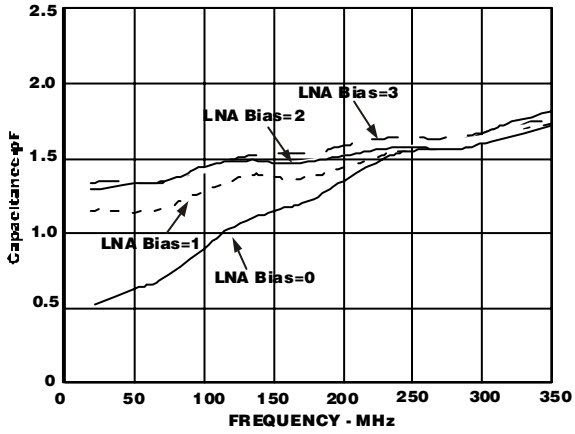


Figure 9b. Shunt Capacitance vs. frequency of the AD9874's IF1 Input

The mixer's differential LO port is driven by a LO buffer stage shown in figure 6 that can be driven single-ended or differential. Since it is self-biasing, the LO signal level can be ac coupled and range from 0.3 to 1.0 Vp.p. with negligible effect on performance. The mixer's open collector outputs, MXOP and MXON, drive an external resonant tank consisting of a differential L-C network tuned to the IF of the bandpass ΣΔ ADC (i.e. $f_{IF2\_ADC} = f_{CLK}/8$). The two inductors provide a dc bias path for the mixer core via a series resistor of 50Ω which is included to dampen the common-mode response. The mixer's ouput *must* be ac coupled to the input of the bandpass ΣΔ ADC, IF2P and IF2N, via two 100 pF capacitors to ensure proper tuning of the L-C center frequency.

The external differential L-C tank forms the resonant element for the first resonator of the bandpass ΣΔ modulator and so must be tuned to the $f_{CLK}/8$ center frequency of the modulator.

The inductors should be chosen such that their impedance at $f_{CLK}/8$ is about 140 ohms (i.e. L=560/(pi*f_{CLK}). An accuracy of 20% is considered to be adequate. For example, at f_{CLK}=18MHz L=10uH is a good choice. Once the inductors have been selected, the required tank capacitance may be calculated using the relation $f_{CLK}/8$ = 1/(2*pi*sqrt(2L*C)).

For example, at f_{CLK}=18MHz and L=10uH, a capacitance of 250pF is needed. However, in order to accomodate an inductor tolerance of +/-10%, the tank capacitance must be adjustable from 227pF to 278pF. Selecting an external capacitor of 180pF ensures that even with a 10% tolerance and stray capacitances as high as 30pF, the total capacitance will be less than the minimum value needed by the tank. Extra capacitance is supplied by the AD9874's on-chip programmable capacitor array. Since the programming range of the capacitor array is at least 160pF, the AD9874 has plenty of range to make up for the tolerances of low-cost external components. Note, if f_{CLK} is increased by a factor of 1.44 to 26 MHz such that $f_{CLK}/8$ becomes 3.25 MHz, reducing L and C by approximately the same factor (i.e. L=6.9 uH and C=120 pF) satisfies the above stated requirements.

The selection of the inductors is an important consideration in realizing the full linearity performance of the AD9874. This is especially the case when operating the LNA and mixer at maximum bias and low clock frequency. Figure 10 shows how the two-tone input-referred IMD vs. input level performance at an IF of 109 MHz and f_{CLK} of 18 MHz varies between Toko's FSLM series and Coilcraft's 1812CS series inductors. The graph also shows the extrapolated point of intersection used to determine the IIP3 performance. Note, the Coilcraft inductor provides a 7-8 dB improvement in performance and closely approximates the 3:1 slope associated with a 3rd order linearity compared to the 2.65:1 slope associated with the Toko inductor. The Coilcraft 1008CS series showed similar performance to the 1812CS series It is worth noting that the difference in IMD performance between these two inductor families with an f_{CLK} of 26 MHz is in significant.

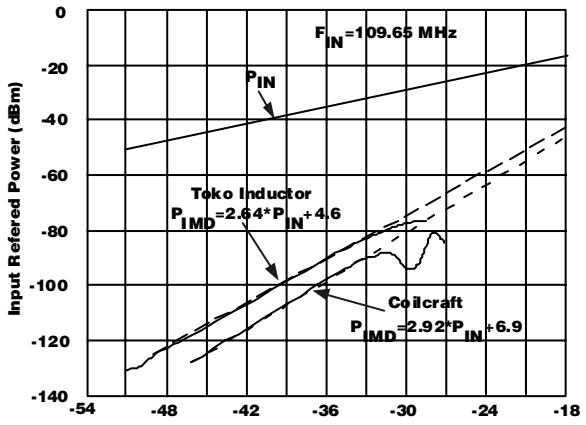


Figure 10. IMD performance between different inductors with LNA and Mixer at full bias and f_{CLK} of 18 MHz

Both the LNA and mixer have four programmable bias settings so that current consumption can be minimized for a given application. Figures 11a, 11b, and 11c show how the LNA and mixer's noise figure (NF), linearity (IIP3), conversion gain, current consumption and frequency response are all affected for a given LNA/Mixer bias setting. The measurements were taken at an IF=73.35 MHz, an LO=71.1 MHz, and supplies set to 3.0 V.

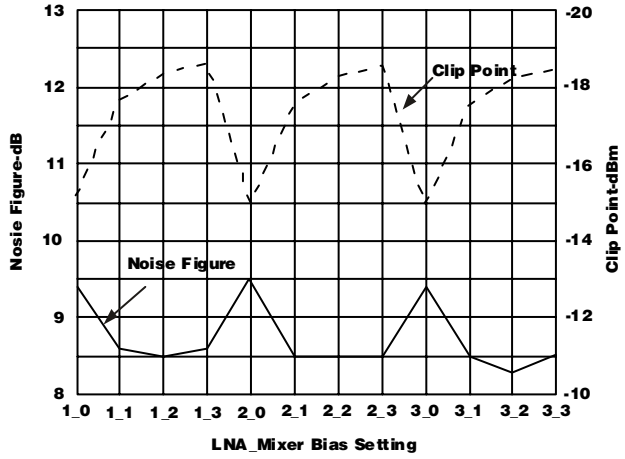


Figure 11a. LNA/Mixer Noise Figure and Conversion Gain vs. Bias Setting

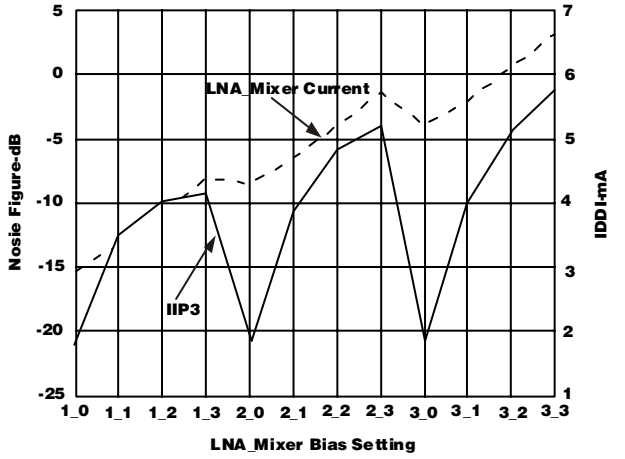


Figure 11b. LNA/Mixer IIP3 and Current Consumption vs. Bias Setting

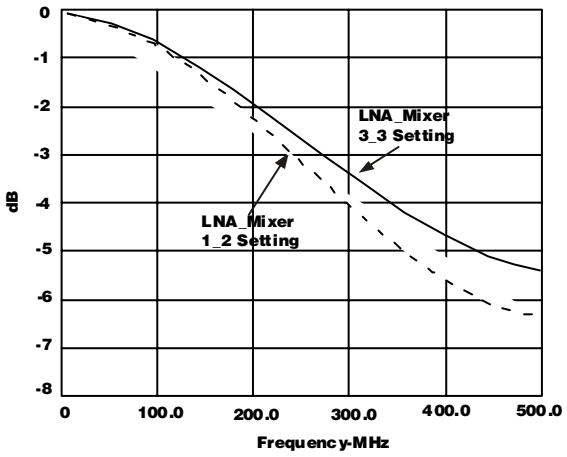


Figure 11c. LNA/Mixer Frequency Response vs Bias Setting

Table VI. SPI Registers associated with LNA/Mixer

Address (Hex)	Bit Breakdown	Width	Default Value	Name
0x01	(7:6)	2	0	LNAB
0x01	(5:4)	2	0	MIXB
0x03	(7)	1	0	ATTEN

BANDPASS SIGMA DELTA (ΣΔ) ADC

The ADC of the AD9874 shown in figure 12. The ADC contains a 6th order multibit **ΣΔ** modulator to achieve a high instantaneous dynamic range. The loop filter of the bandpass **ΣΔ** modulator consists of two continuous-time resonators followed by a discrete time resonator with each resonator stage contributing a pair of complex poles. The first resonator is an external LC tank while the second is an on-chip active-RC filter. The output of the LC resonator is ac coupled to the second resonator input via 100 pF capacitors. The center frequencies of these two continuous-time resonators *must be* tuned to $f_{CLK}/8$ in order for the ADC to function properly. The center frequency of the discrete-time resonator automatically scales with f_{CLK}, thus no tuning is required.

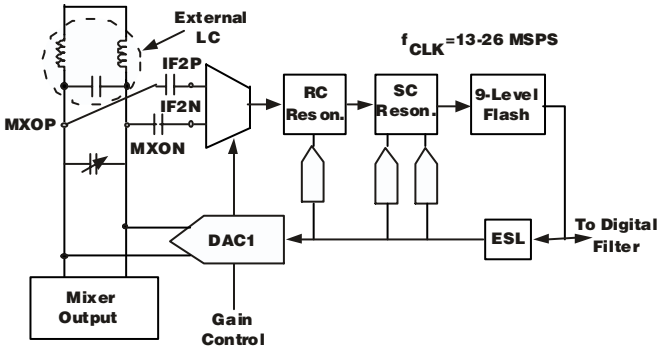


Figure 12. Equivalent circuit of 6th order bandpass **ΣΔ** modulator.

Figure 13a shows the measured power spectral density measured at the output of the undecimated bandpass **ΣΔ** modulator. Note, the wide dynamic range achieved at the center frequency, $f_{CLK}/8$, is achieved once the LC and RC resonators of the **ΣΔ** modulator has been succesfully tuned. The out-of-band noise is removed by the decimation filters following quadrature demodulation.

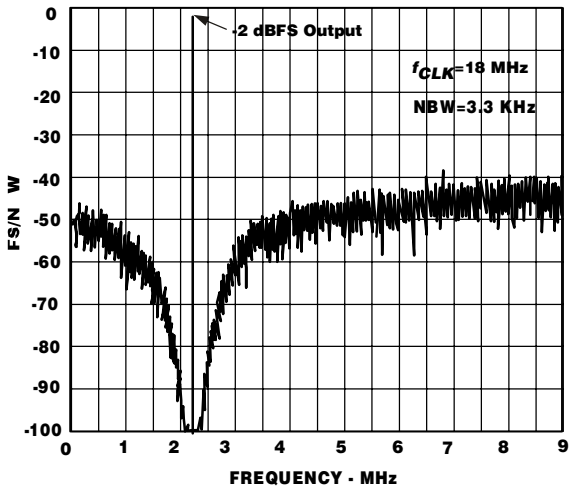


Figure 13a. Measure undecimated spectral Output of **ΣΔ** modulator ADC with f_{CLK} =18 MSPS and noise bandwidth of 3.3 kHz.

The signal transfer function of the AD9874 possesses inherent anti-alias filtering by virtue of the continuous-time portions of the loop filter in the bandpass **ΣΔ** modulator. Figure 13b. illustrates this property by plotting the nominal signal transfer function of the ADC for frequencies up to $2f_{CLK}$. The notches that naturally occur for all frequencies which alias to the $f_{CLK}/8$ passband are clearly visible. Even at the widest bandwidth setting, the notches are deep enough to provide greater than 80 dB of alias protection. Hence, the *wideband* IF filtering requirements preceding the AD9874 will be mostly determined by the mixer's image band that is offset from the desired IF input frequency by $f_{CLK}/4$ (i.e. $2*f_{CLK}/8$) rather than any aliasing associated with the ADC.

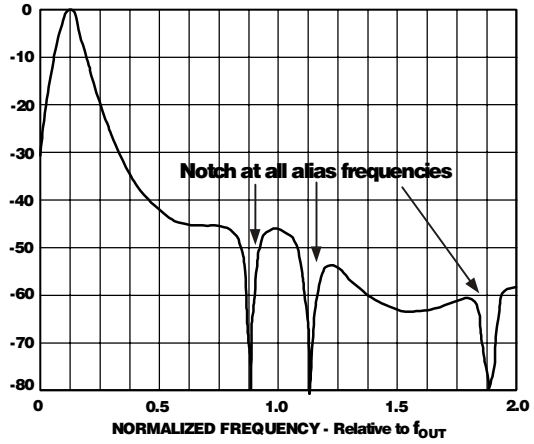


Figure 13b. Signal transfer function of the bandpass **ΣΔ** modulator from 0 to $2f_{CLK}$.

Figure 13c. shows the nominal signal transfer function magnitude for frequencies near the f_{CLK} /8 pass-band. The width of the passband determines the transfer function droop, but even at the lowest oversampling ratio (48) where the passband is f_{CLK} /192 (» 0.005 f_{CLK}), the STF gain variation is less than 0.5 dB. Note, the amount of attenuation offered by the signal transfer function near f_{CLK} /8 should also be considered when determining the *narrowband* IF filtering requirements preceding the AD9874.

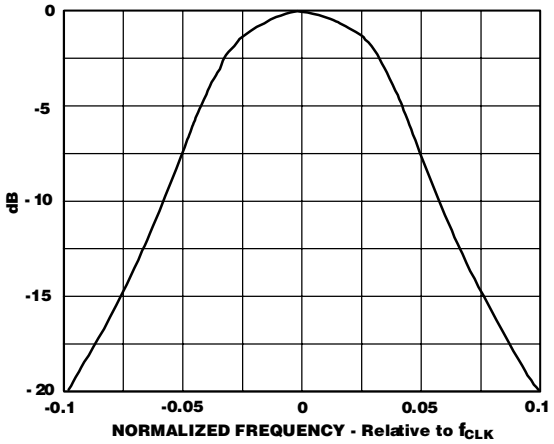


Figure 13c. Magnitude of the ADC's signal transfer function near f_{CLK}/8.

Tuning of the **ΣΔ** modulator's two continuous-time resonators is *essential* in realizing the ADC's full dynamic range and must be performed upon system start-up. To facilitate tuning of the LC tank, a capacitor array is internally connected to the MXOP and MXON pins. The capacitance of this array is programmable from 0 pF to 200 pF ±20% and can be programmed either automatically or manually via the SPI port. The capacitors of the active-RC resonator are similarly programmable. Note, the AD9874 can be placed in and out of its stand-by mode without re-tuning since the tuning codes are stored in the SPI registers.

When tuning the LC tank, the sampling clock frequency *must* be stable and the LNA/mixer, LO synthesizer, and ADC *must* all be placed in standby. Tuning is triggered when the ADC is taken out of standby if the TUNE_LC bit of register 0x1C has been set. This bit will clear when the tuning operation is complete (less than 6 ms). The tuning codes can be read from the 3-bit CAPL1 (0x1D) and the 6-bit CAPL0 (0x1E) registers.

In a similar manner, tuning of the RC resonator is activated if the TUNE_RC bit of register 0x1C is set when the ADC is taken out of standby and this bit will clear when tuning is complete. The tuning code can be read from the CAPR (0x1F) register. Setting both the TUNE_LC and TUNE_RC bits tunes the LC tank and the active-RC resonator in succession. During tuning, the ADC is not operational and neither data nor a clock are available from the SSI port. Table IX lists the recommended sequence of SPI commands for tuning the ADC while Table X lists the associated SPI registers.

Table IX. Tuning Sequence

Address	Value	Comments
0x01	0x45	LO synthesizer, LNA/Mixer and ADC in standby.
0x01	0x03	Set TUNE_LC and TUNE_RC. Wait for CLK to stabilize.
0x03	0x44	Take the ADC out of standby. Wait for 0x1C to clear (<6ms). LNA/Mixer can not be taken out of stand-by.

Table X. SPI Registers associated with bandpass **ΣΔ** ADC

Address (Hex)	Bit Breakdown	Width	Default Value	Name
0x1C	(1)	1	0	TUNE_LC
	(0)	1	0	TUNE_RC
0x1D	(2:0)	3	0	CAPL1(2:0)
0x1E	(5:0)	6	0x00	CAPL1(5:0)
0x1F	(7:0)	8	0x00	CAPR

DECIMATION FILTER

The decimation filter shown in figure 14. consists of a complex mix by *f CLK* /8 and a cascade of three linear phase FIR filters: DEC1, DEC2 and DEC3. DEC1 downsamples by a factor of 12 using a 4th-order comb filter. DEC2 also uses a 4th-order comb filter, but its decimation factor is set by the M field of register 0x07. DEC3 is either a decimate-by-5 FIR filter or a decimate-by-4 FIR filter depending on the value of the K bit within register 0x07. Hence, the composite decimation factor can be set to either 60*M or 48*M for K equal to 0 or 1 respectively.

The output data rate (f_{OUT}) is equal to the modulator clock frequency (f_{CLK}) divided by the digital filter's decimation factor. Due to the transition region associated with the decimation filter's frequency response, the decimation factor *must* be selected such that f_{OUT} is equal to or greater than *twice* the signal bandwidth. This ensures low amplitude ripple in the passband along with the ability to provide further application-specific digital filtering prior to demodulation.

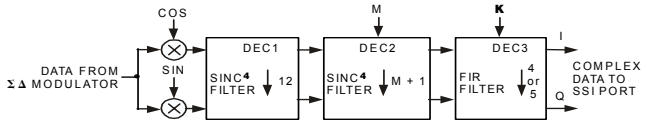


Figure 14. Decimation Filter Architecture

Figure 15a shows the response of the decimation filter at a decimation factor of 900 (K=0, M=14) and a sampling clock frequency of 18 MHz. In this example, the output data rate (f_{OUT}) is 20 KSPS with a usable complex signal bandwidth of 10 KHz centered around DC. As this figure shows, the first and second alias bands (occurring at *even* integer multiples of f_{OUT}/2) have the least attenuation, but nonetheless provide at least 88 dB of attenuation. Note, signals falling at frequency offsets that are *odd* integer multiples of

f_{OUT}/2 (i.e. 30 kHz and 50 kHz) will fall back into the transition band of the digital filter.

Figure 15b shows the response of the decimation filter with a decimation factor of 48 and a sampling clock rate of 26 MHz. The alias attenuation is now at least 94 dB and this attenuation occurs for frequencies at the edges of the fourth alias band. The difference between the alias attenuation characteristics of this figure and those of Fig. 15a. is due to the fact that the third decimation stage decimates by a factor of 5 for Fig. 15a., versus a factor of 4 for Fig. 15b.

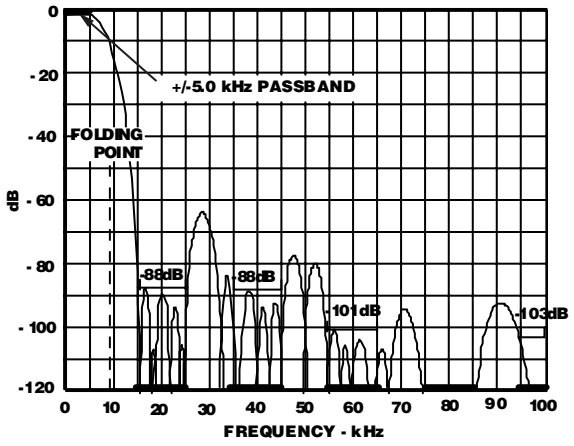


Figure 15a. Decimation filter frequency response for f_{OUT} = 20 KSPS. (f_{CLK}= 18 MHz, OSR=900)

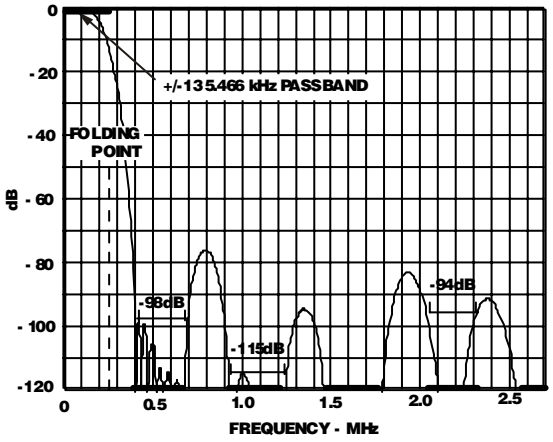


Figure 15b. Decimation filter frequency response for f_{OUT} = 541.666 KSPS. (f_{CLK}= 26 MHz, OSR=48)

Figures 16a. and 16b. show expanded views of the passband for the two possible configurations of the third decimation filter. When decimating by 60*n* (K=0) the passband gain variation is 1.2 dB and when decimating by 48*n* (K=1) the passband gain variation is 0.9 dB. Normalization of full-scale at band-center is accurate to within 0.14 dB across all decimation modes. Figures 17a and 17b show the folded frequency response of the decimator for K=0 and K=1, respectively.

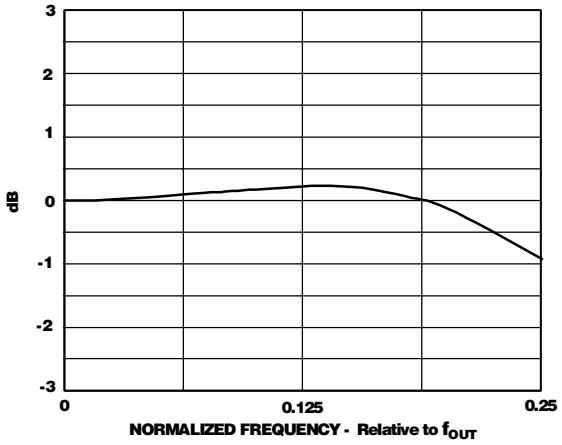


Figure 16a. Passband frequency response of the decimator for K=0.

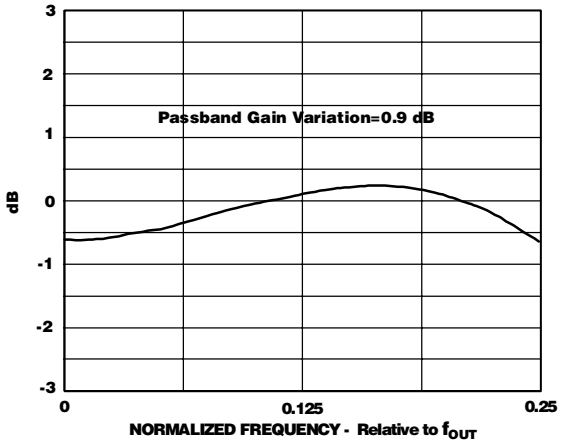


Figure 16b. Passband frequency response of the dec imator for K=1.

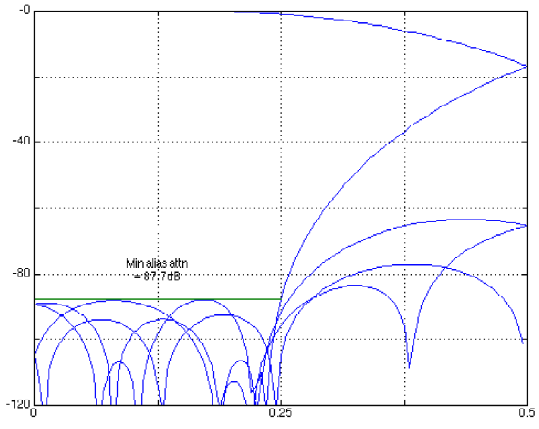


Figure 17a. Folded Decimator Frequency Response for K=0

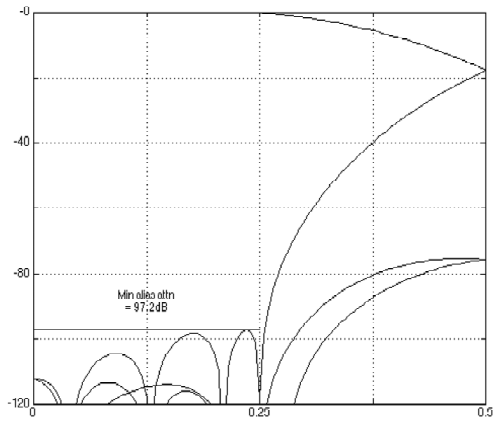


Figure 17b. Folded Decimator Frequency Response for K=1.

VARIABLE GAIN AMPLIFIER OPERATION WITH AUTOMATIC GAIN CONTROL

The AD9874 contains both a variable gain amplifer (VGA) and a "digital VGA" (DVGA) along with all of the necessary signal estimation and control circuitry to implement automatic gain control(AGC) as shown in figure 18. The AGC control circuitry provides a high degree of programability to allow the user to optimize the AGC response as well as the AD9874's dynamic range for a given application. The VGA is programmable over a 12 dB range and implemented within the ADC by adjusting its full-scale reference level. Increasing the ADC's full-scale is equivalent to attenuating the signal. An additional 12 dB of digital gain range is achieved by scaling the output of the decimation filter in the "digital VGA" (DVGA).

The purpose of the VGA is to extend the usuable dynamic range of the AD9874 by allowing the ADC to digitize low level signals in the presence of larger unfiltered interferer signals without saturation or "clipping" the ADC. The DVGA is most useful in extending the dynamic range in narrowband applications requiring a 16-bit I and Q data format. In these applications, quantization noise resulting from internal truncation to 16-bits as well as external 16-bit fixed point post-processing can degrade the AD9874's effective noise figure by one or more dB. The DVGA is enabled by writing a 1 to the AGCV field. The VGA (and the DVGA) can operate in either a user controlled variable gain mode or automatic gain control (AGC) mode.

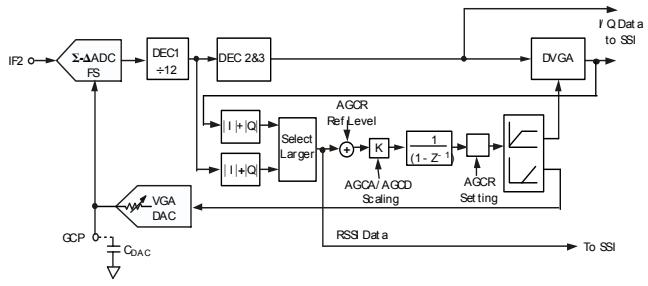


Figure 18. Functional block diagram of VGA and AGC

Variable Gain Control

The variable gain control is enabled by setting the AGCR register to 0. In this mode, the gain of the VGA (and the DVGA) can be adjusted by writing to the 16-bit AGC register. The maximum update rate of the AGC register via the SPI port is $f_{CLK}/240$. The MSB of this register is the bit which enables 16 dB of attenuation in the preamp. This feature allows the AD9874 to cope with large level signals beyond the VGA's range (i.e. > -18 dBm at LNA input) to prevent overloading of the ADC.

The lower 15 bits specify the attenuation in the remainder of the signal path. If the DVGA is enabled, the attenuation range is from -12 to +12 dB since the DVGA provides 12 dB of digital gain. In this case, all 15 bits are significant. However, with the DVGA disabled the attenuation range extends from 0 to +12 dB and only the lower 14 bits are useful. Figure 19. shows the relationship between the amount of attentuation and the AGC register setting for both cases.

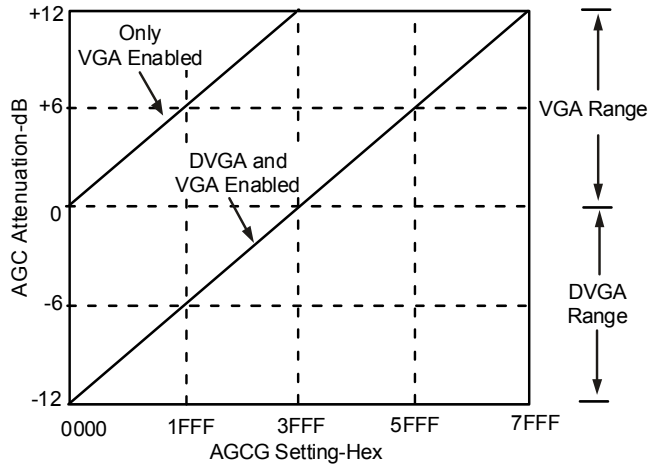


Figure 19. AGC gain range characteristics vs. AGCG register setting with and without DVGA enabled.

Referring to figure 18, the gain of the VGA is set by an 8-bit control DAC which provides a control signal to the VGA appearing at the GCP pin. For applications implementing automtic gain control, the DAC's output resistance can be reduced by a factor of 9 to decrease the attack time of the AGC response for faster signal acquistion. An external 2.2 nF capacitor, C_{DAC}, from GCP to analog ground is required to "smooth" the DAC's output each time it updates as well as to filter wideband noise. Note, C_{DAC} in combination with the DAC's programmable output resistance sets the -3 dB bandwidth and time constant associated with this RC network.

A *linear* estimate of the received signal strength is performed at the output of the first decimation stage (DEC1) as discussed in the following AGC section. This data is available as a 6-bit signal strength field within an SSI frame with 60 corresponding to a full-scale signal for a given AGC attenuation setting. The signal strength field is updated at $f_{CLK}/60$ and can be used with the 8-bit attenuation field (or AGCG attenuation setting) to

determine the absolute signal strength.

The accuracy of the *mean* SSI reading (relative to the IF input power) depends on the input signal's frequency offset relative to the IF frequency since both DEC1 filter's response as well as the ADC's signal transfer function attenuates the mixer's downconverted signal level centered at $f_{CLK}/8$. As a result, the estimated signal strengh of input signals falling within proximity to the IF are reported accurately while those signals at increasingly higher frequency offsets incur larger measurement errors. Figure 20. shows the normaized error of the SSI reading as a function of the frequency offset from the IF frequency. Note, the significance of this error becomes apparent when determining the maximum input inteferer (or blocker) levels with the AGC enabled.

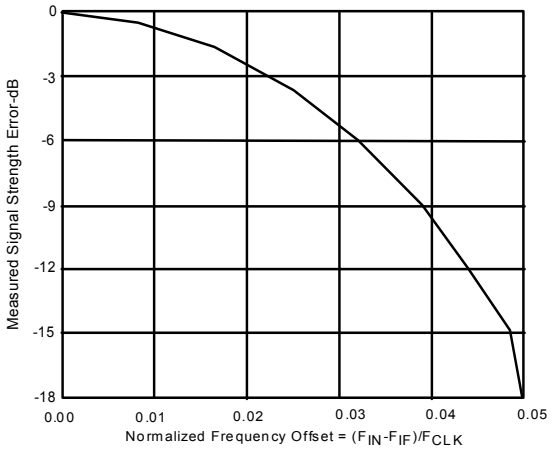


Figure 20. Normalized SSI error vs. normalized IF fequency offset.

Automatic Gain Control (AGC)

The gain of the VGA (and DVGA) is automatically adjusted when the AGC is enabled via the AGCR register. In this mode, the gain of the VGA is continuously updated at $f_{CLK}/60$ in an attempt to ensure that the maximum *analog* signal level into the ADC does not exceed the ADC clip level and that the rms output level of the ADC is equal to a programmable reference level. With the DVGA enabled, the AGC control loop also attempts to minimize the effects of 16-bit truncation noise prior to the SSI output by continuously adjusting the DVGA's gain to ensure maximum digital gain while not exceeding the programmable reference level.

This programable level can be set at 3, 6, 9, 12, and 15 dB below the ADC saturation (clip) level by writing values from 1 to 5 to the 3-bit AGCR field. Note, the ADC clip level is defined to be 2 dB below its full-scale (i.e. -18 dBm at the LNA input for a matched input and maximum attenuation). If AGCR is 0, automatic gain control is disabled. Since "clipping" of the ADC input will degrade the SNR performance, the reference level should also take into consideration the peak-to-rms characteristics of the target (or interferer) signals.

Referring again to figure 18, the majority of the AGC loop operates in the discrete time domain. The sample rate of the loop is $f_{CLK}/60$ thus registers associated with the AGC algorithm are updated at this rate. The number of overload and ADC reset occurances within the final I/Q update rate of the AD9874 as well as the AGC value (8 MSB's) can be read from the SSI data upon proper configuration.

The AGC performs digital signal estimation at the output of the 1st decimation stage (DEC1) as well as the DVGA output that follows the last decimation stage (DEC3). The rms power of the I and Q signal is estimated by the following equation:

(5) $Xest[n] = Abs(I[n]) + Abs(Q[n])$

Signal estimation after the 1st decimation stage allows the AGC to cope with out-of-band interferers and in-band signals which could otherwise overload the ADC. Signal estimation after the DVGA allows the AGC to minimize the effects of 16-bit truncation noise. When the estimated signal level falls within the range of the AGC, the AGC loop adjusts the VGA (or DVGA) attenuation setting such that the estimated signal level is equal to the programmed level specified in the AGCR field. The absolute signal strength can be determined from the contents of the attenuation setting and signal strength indicator that is available in the SSI data frame when properly configured.

A description of the AGC control algorithm and the user adjustable parameters follows. First, consider the case in which the in-band target signal is bigger than all out-of-band inteferers and the DVGA is *disabled*. With the DVGA disabled, a control loop based only on the target signal power measured after DEC1 is used to control the VGA gain and the target signal will be tracked to the programmed reference level. If the signal is too large, the attenuation is increased with a proportionality constant determined by the AGCA setting. Large AGCA values result in large gain changes thus rapid tracking of changes in signal strength. If the target signal is too small relative to the reference level, the attenuation is reduced but now the proportionality constant is determined by both the AGCA and AGCD settings. The AGCD value is effectively subtracted from AGCA, so large AGCD results in smaller gain changes and thus slower tracking of fading signals.

The 4-bit code in the AGCA field sets the raw bandwidth of the AGC loop. With AGCA=0, the AGC loop bandwidth is at its minimum of 50 Hz assuming f_{CLK}=18 MHz. Each increment of AGCA increases the loop bandwidth by a factor of $2^{1/2}$ thus the maximum bandwidth is 9 kHz. A general expression for the attack bandwidth is

(6) $BW_A = 50 \text{ x } (f_{CLK}/18MHz) \text{ x } 2^{(AGCA/2)}$ Hz

and the corresponding attack time is

(7) $t_{attack} = 2.2/(100 \star \pi \star 2^{AGCA/2}) = 0.35/BW_A$

assuming that the loop dynamics are essentially that of a single-pole system.

The 4-bit code in the AGCD field sets the ratio of the attack time to the decay time in the amplitude estimation circuitry.

When AGCD is zero, this ratio is one. Incrementing AGCD multiplies the decay time-constant by $2^{1/2}$, allowing a 180:1 range in the decay time relative to the attack time. The decay time may be computed from

(8) $t_{decay} = t_{attack} \times 2^{(AGCD/2)}$

Figure 21a. shows the AGC response to a 30 Hz pulse modulated IF burst for different AGCA and AGCD settings.

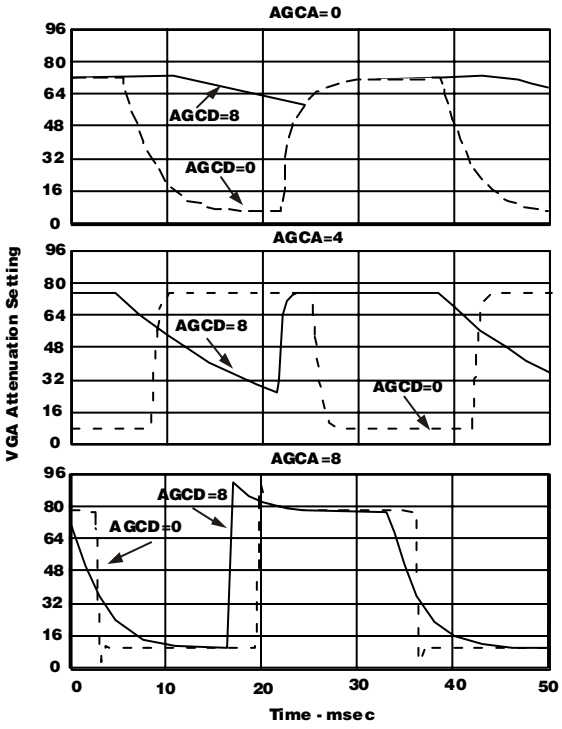


Figure 21a. AGC Response for Different AGCA and AGCD settings with f_{CLK}=18 MSPS and f_{CLK}=20 KSPS and AGCO=0.

The 3-bit value in the AGCO field determines the amount of attenuation added in response to a reset event in the ADC. Each increment in AGCO doubles the weighting factor. At the highest AGCO setting, the attenuation will change from 0 to 12 dB in approximately 10 us, while at the lowest setting the attenuation will change from 0 to 12 dB in approximately 1.2 ms. (Both times assume f_{CLK} = 18 MHz.). Figure 21b. shows the AGC attack time response for different AGCA settings.

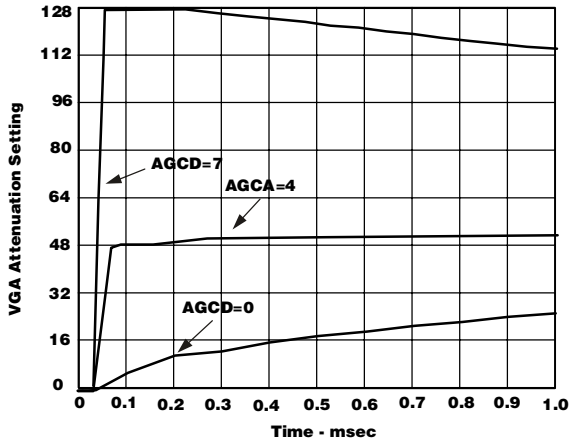


Figure 21b. AGC Response for Different AGCO settings with f_{CLK}=18 MSPS , f_{CLK}=300 KSPS and AGCA=AGCD=0.

Lastly, the AGCF bit reduces the DAC source resistance by at least a factor of 10. This facilitates fast acquisition by lowering the RC time constant which is formed with the external capacitors connected from the GCP pin to the GCN ground pin. For an overshoot-free step response in the AGC loop, the capacitors should be chosen such that the RC time constant is less than one quarter that of the raw loop. Specifically,

(9) $RC \leq 1/(8\pi BW)$

where *R* is the resistance between the GCP pin and GCN ground pin and ground (TBD Ω ±20% if AGCF = 0, <TBD Ω if AGCF = 1) and *BW* is the raw loop bandwidth. Note that with *C* chosen at this upper limit, the loop bandwidth increases by approximately 30%.

Now consider the same case as above *but* with the DVGA *enabled* to minimize the effects of 16-bit truncation. With the DVGA *enabled*, a control loop based on the larger of the two estimated signal levels (i.e. output of DEC1 and DVGA) is used to control the DVGA gain. The DVGA multiplies the output of the decimation filter by a factor ranging from 1 to 4 (i.e. 0 to 12 dB). When signals are small, the DVGA gain is 4 and the 16-bit output is extracted from the 24-bit data produced by the decimation filter by dropping 2 MSBs and taking the next 16 bits. As signals get larger, the DVGA gain decreases until the point where the DVGA gain is 1 and the 16-bit output data is simply the 16 MSBs of the internal 24-bit data. As signals get still larger, attenuation is accomplished by the normal method of increasing the ADC's full-scale.

The extra 12 dB of gain range provided by the DVGA reduces the input-referred truncation noise by 12 dB and makes the data

more tolerant of LSB corruption within the DSP. The price paid for this extension to the gain range is that the onset of AGC action is 12 dB lower and that the AGC loop will be unstable if its bandwidth is set too wide. The latter difficulty results from the large delay of the decimation filters, DEC2 and DEC3, when one implements a large decimation factor. As a result, given an option, the use of 24-bit data is preferable to using the DVGA.

Table XII indicates which AGCA values are reasonable for various decimation factors. The white cells indicate that the (decimation factor, AGCA) combination works well. The light gray cells indicate ringing and an increase in AGC settling time and the dark gray cells indicate that the combination results in instability or near-instability in the AGC loop. Setting AGCF=1 improves the time-domain behavior at the expense of increased spectral spreading.

Decimation Factor	M	AGCA 4	5	6	7	8	9	10	11	12	13	14	15
60	0												
120	1												
300	4												
540	8												
900	E												

Table XII. AGCA limits if the DVGA is enabled

Lastly, consider the case of a “strong” out-of-band interferer (i.e. -18 to -32 dBm for matched IF input) that is larger than the target signal and large enough to be tracked by the control loop based on the output of the DEC1. The ability of the control loop to track this interferer and set the VGA attenuation to prevent “clipping” of the ADC is limited by the accuracy of the digital signal estimation occuring at the output of DEC1. The accuracy of the digital signal estimation is a function of the frequency offset of the out-of-band interferer relative to the IF frequency as shown in figure 20. Interferers at increasingly higher frequency offsets incur larger measurement errors potentially causing the control loop to inadvertently reduce the amount of VGA attenuation which may subsequently result in “clipping” of the ADC. Figure 21c. shows the maximum measured interferer signal level vs. normalized IF offset frequency (relative to f_{CLK}) tolerated by the AD9874 relative to its maximum target input signal level (0 dBFS=-18 dBm). Note, the increase in allowable interferer level occuring beyond $0.04*F_{CLK}$ results from the inherent signal attenuation provided by the ADC’s signal transfer function.

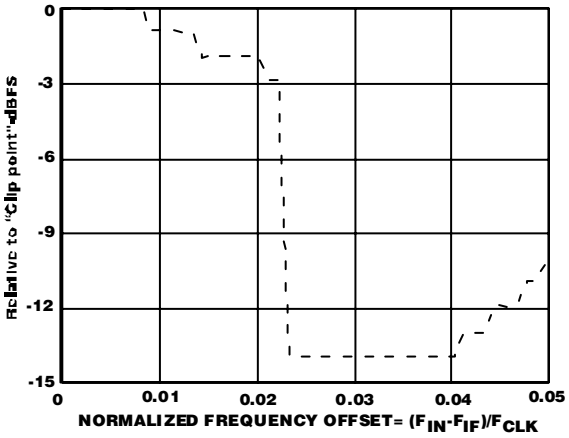


Figure 21c. Maximum Interferer (or Blocker) input level vs. normalized IF fequency offset.

Table XIII. SPI Registers associated with AGC

Address (Hex)	Bit Breakdown	Width	Default Value	Name
0x03	(7)	1	0	ATTEN
	(6:0)	7	0x00	AGC(14:8)
0x04	(7:0)	8	0x00	AGC(7:0)
0x05	(7:4)	4	0	AGCA
	(3:0)	4	0x00	AGCD
0x06	(7)	1	0	AGCV
	(6:4)	3	0	AGCO
	(3)	1	0	AGCF
	(2:0)	3	0	AGCR

System Noise Figure(NF) vs. VGA (or AGC) Control
The AD9874’s system noise figure is a function of the ACG attenuation and output signal bandwidth. Fig. 18a plots the nominal system NF as a function of the AGC attenuation for both narrowband (20 kHz) and wideband (150 kHz) modes with f_{CLK}=18MHz. Also shown on the plot is the SNR that would be observed at the output for a -2 dBFS input. The high dynamic range of the ADC within the AD9874 ensures that the system NF increases gradually as the AGC attenuation is increased. In narrowband (BW = 20 kHz) mode, the system noise figure increases by less than 2 dB over a 12 dB AGC range, while in wideband (BW = 150 kHz) mode the degradation is less than 5 dB. As a result, the highest instantaneous dynamic range for the AD9874 occurs with 12 dB of AGC attenuation since the AD9874 can accomodate an additional 12 dB peak signal level with only a moderate increase in its noise floor.

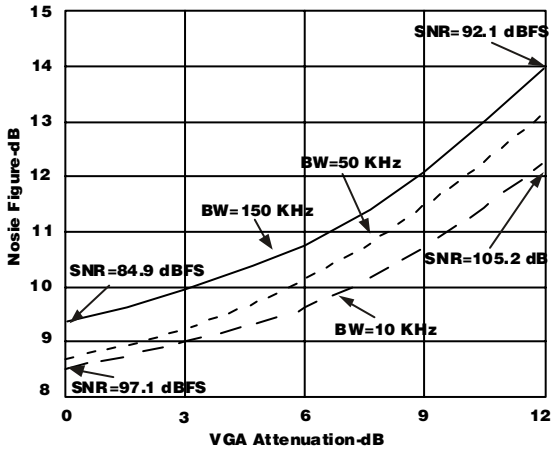


Figure 22a. Nominal system noise figure and peak SNR vs. AGC. f_{IF}=73.35 MHz and CLK=18 MSPS and 24-bit I/Q data.)

As figure. 22a. shows, the AD9874 can achieve a SNR in excess of 100 dB in narrowband applications. To realize the full performance of the AD9874 in such applications, it is recommended that the I/Q data be represented with 24 bits. If 16-bit data is used, the effective system NF will increase because of the quantization noise present in the 16-bit data after truncation.

Figure22b. plots the nominal system NF with 16-bit output data as a function of AGC in both narrowband and wideband mode. In wideband mode, the NF curve is virtually unchanged relative to the 24-bit output data because the output SNR before truncation is always less than the 96 dB SNR that 16-bit data can support. However, in narrowband mode, where the output SNR approaches or exceeds the SNR that can be supported with 16-bit data, the degradation in system NF is more severe. Furthermore, if the signal-processing within the DSP adds noise at the level of an LSB, the system noise figure can be degraded even more than Fig. 22b shows. For example, this could occur in a fixed 16-bit DSP whose code is not optimized to process the AD9874's 16-bit data with minimal quantization effects.

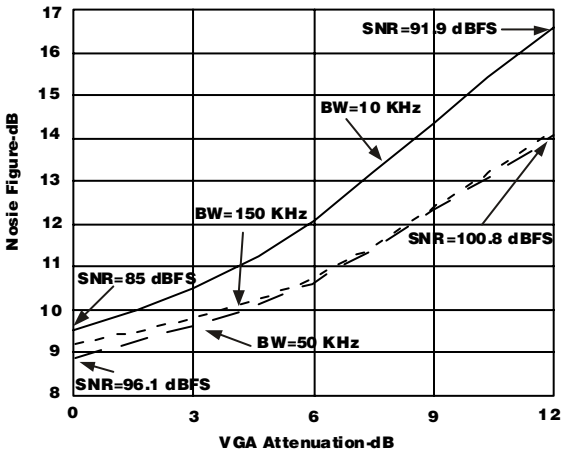


Figure 22b. Nominal system noise figure and peak SNR vs. AGC. f_{IF}=73.35 MHz and CLK=18 MSPS and 16-bit I/Q data.)

APPLICATION CONSIDERATIONS

FREQUENCY PLANNING

The LO frequency (and/or ADC clock frequency) must be chosen carefully in order to prevent known internally generated spurs from mixing down along with the desired signal thus degrading the SNR performance. The major sources of spurs in the AD9874 is the ADC clock and digital circuitry operating at 1/3 of f_{CLK}. Hence, the clock frequency (f_{CLK}) is the most important variable in determining which LO (and hence IF) frequencies are viable.

Many applications have frequency plans that take advantage of industry standard IF frequencies due to the large selection of low cost crystal or SAW filters. If the selected IF frequency and ADC clock rate results in a problematic spurious component, an alternative ADC clock rate should be selected by slightly modifying the decimation factor and CLK synthesizer settings (if used) such that the output sample rate remains the same. Also, applications requiring a certain degree of tuning range should take into consideration the location and magnitude of these spurs when determing the tuning range as well as optimum IF and ADC clock frequency.

Figure 23a. plots the measured in-band noise power as a function of the LO frequency for f_{CLK} = 18 MHz and an output signal bandwidth of 150 kHz when no signal is present. Any LO frequency resulting in large spurs should be avoided. As this figure shows, large spurs result when the LO is f_{CLK} /8 = 2.25 MHz away from a harmonic of 18 MHz (i.e. $n f_{CLK} \pm f_{CLK}/8$). Also problematic are LO frequencies whose odd order harmonics (i.e. $m f_{LO}$) mix with harmonics of f_{CLK} to f_{CLK} /8 . This spur mechanism is a result of the mixer being internally driven by a "squared-up" version of the LO input consisting of the LO frequency and its odd order harmonics. These spur frequencies can be calculated from the following relation:

(10) $m f_{LO} = n f_{CLK} \pm f_{CLK}/8$
where m= 1, 3, 5 ... and n= 1, 2, 3 ...

A second source of spurs is a large block of digital circuitry which is clocked at f CLK /3. Problematic LO frequencies associated with this spur source are given by

(11) $f_{LO} = f_{CLK}/3 + n f_{CLK} +/- f_{CLK}/8$
where n= 1, 2, 3 ...

Figure 23b shows that omitting LO frequencies given by (10) for m=1, 3, 5 and by (11) accounts for most of the spurs. tained elsewhere. Some of the remaining low-level spurs can be attributed to coupling from the SSI digital output. As a result, users are also advised to optimize the output bit rate (f_{CLKOUT} via the SSIORD register) as well as the digital output driver strength to achieve the lowest spurious and noise figure performance for a particular LO frequency and f_{CLK} setting.

Despite the many spurs, sweet spots in the LO frequency are generally wide enough to accommodate the maximum signal bandwidth of the AD9874. As evidence of this property, figure 24 shows that the in-band noise is quite constant for LO frequencies ranging from 70 to 71 MHz.

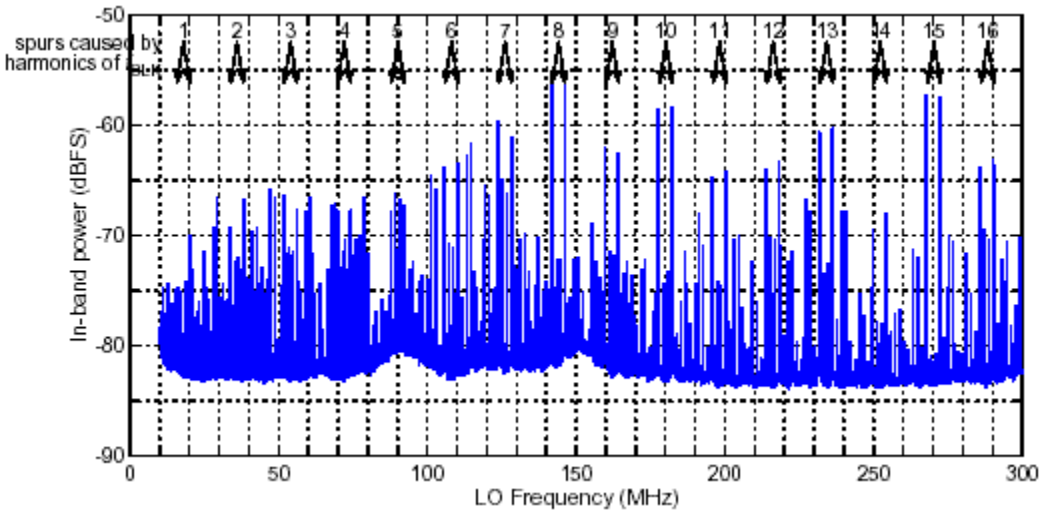


Figure 23a. Total in-band noise+spur power with no signal applied aas a function of the LO frequency (fCLK=18 MHz and output signal bandwidth of 150 kHz).

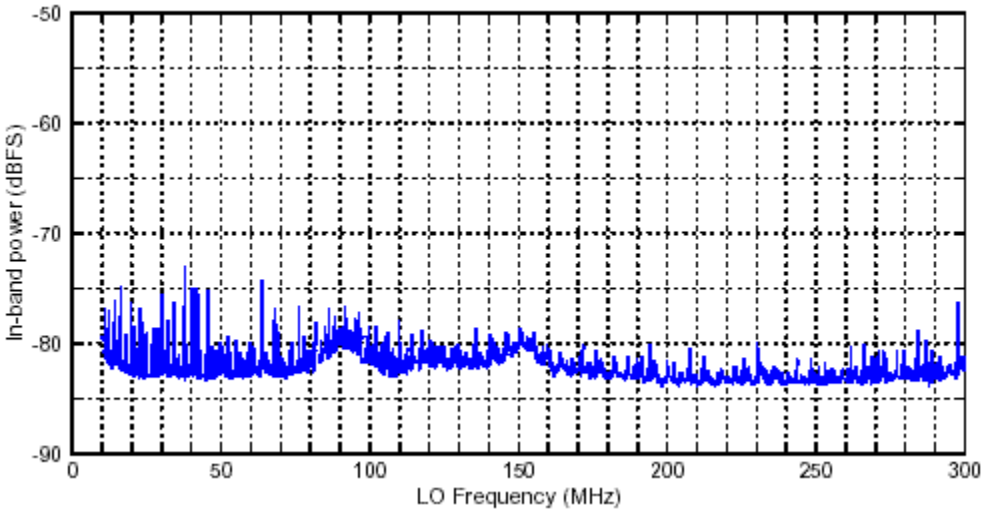


Figure 23b. Same as figure 23a excluding LO frequencies known to produce large in-band spurs

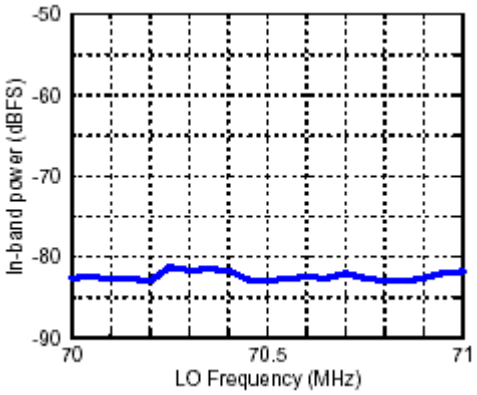


Figure 24. Expanded view from 70 to 71 MHz.

SPURIOUS RESPONSES

The spectral purity of the LO (including its phase noise) is an important consideration since LO spurs can mix with undesired signals present at the AD9874's IFIN input to produce an in-band response. To demonstrate the low LO spur level introduced *within* the AD9874 itself, figure. 25 plots the de-modulated output power as a function of the input IF frequency for an LO frequency of 71.1 MHz and a clock frequency of 18 MHz.

The two large -10 dBFS spikes near the center of the plot are the desired responses at $f_{LO} \pm f_{IF2\_ADC}$ where $f_{IF2\_ADC} = f_{CLK}/8$, i.e. at 68.85 and 73.35 MHz. LO spurs at $f_{LO} \pm f_{spur}$ would result in spurious responses at offsets of $\pm f_{spur}$ around the desired responses. Close-in spurs of this kind are not visible on the plot, but small spurious responses at $f_{LO} \pm f_{IF2\_ADC} \pm f_{CLK}$, i.e.

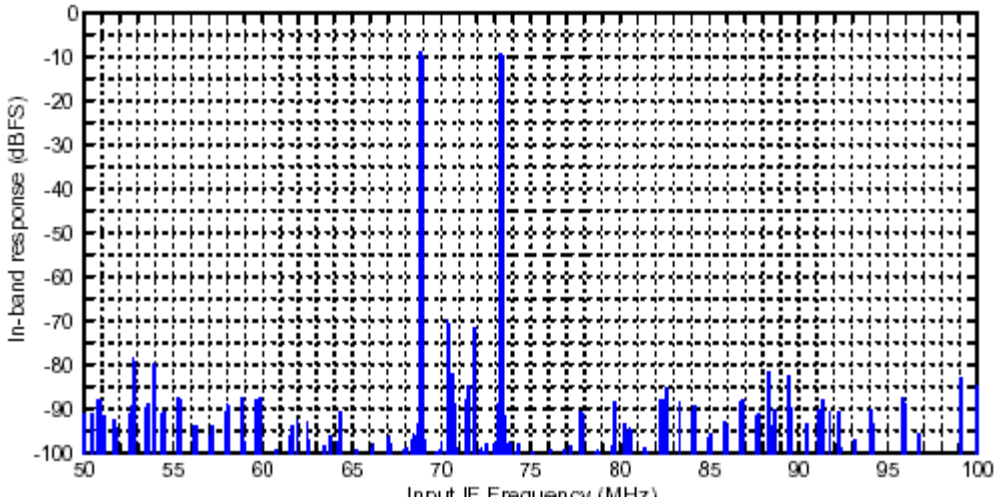


Figure 25. Response of AD9874 to a -20 dBm input IF input when f_{LO} = 71.1 MHz.

at 50.85, 55.35, 86.85 and 91.35 MHz, are visible at the -90 dBFS level. This data indicates that the AD9874 does an excellent job of preserving the purity of the LO signal.

Fig. 25can also be used to gauge how well the AD9874 is able to reject undesired signals. For example, the "half-IF" response at (69.975 and 72.225 MHz) is approximately -100 dBFS, giving a selectivity of 90 dB for this spurious response. The largest spurious response at approximately -70 dBFS occurs with input frequencies of 70.35 and 71.85 MHz. These spurs result from 3 rd-order nonlinearity in the signal path (i.e. $abs[3*f_{LO}-3*f_{IF\_Input}] = f_{CLK}/8$).

EXTERNAL PASSIVE COMPONENT REQUIREMENTS

Figure 26 shows an example circuit using the AD9874. The purpose is to show the various external passive components required by the AD9874. The LO, CLK and IFIN signals are coupled to their respective inputs using 10 nF capacitors. The output of the mixer is coupled to the input of the ADC using 100 pF. An external 100 kΩ resistor from the RREF pin to GND sets up the AD9874's internal bias currents. The remaining capacitors are used to decouple sensitive internal nodes to GND.

Although power supply decoupling capacitors are not shown, it is recommended that a 0.1 uF surface mount capacitor be placed as close as possible to each power supply pin for maximum effectiveness. Also not shown is the input impedance-matching network used to match the AD9874's IF input to the external IF filter. Lastly, the loop filter components associated with the LO and CLK synthesizers are not shown.

LC component values for f_{CLK} = 18 MHz are given on the diagram. For other clock frequencies, the two inductors and the capacitor of the LC tank should be scaled in inverse proportion to the clock. For example, if f_{CLK} = 26 MHz, then the two inductors should be = 6.9 µH and the capacitor should be about 120 pF. A tolerance of 10% is sufficient for these components since tuning of the LC tank is performed upon system start-up.

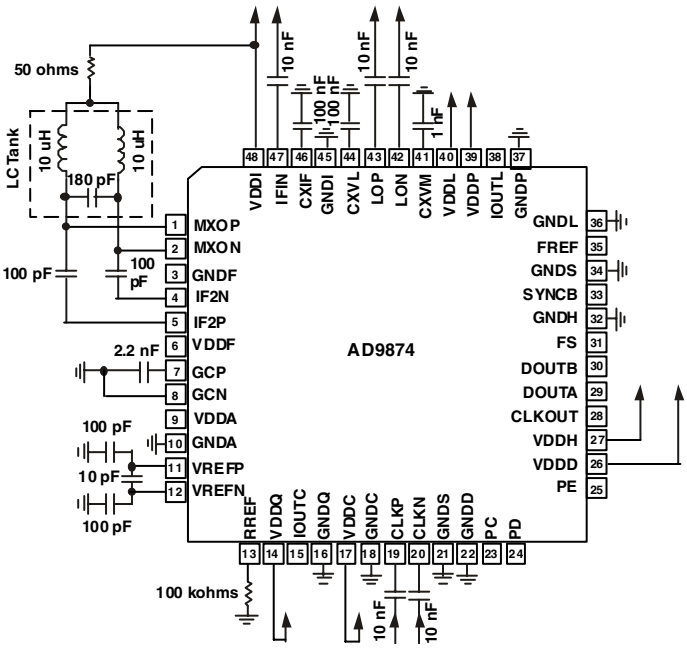


Figure 26. Example circuit showing recommended component values.

LAYOUT EXAMPLE, EVALUATION BOARD AND SOFTWARE

The evaluation board along with its accompanying software provide a simple means to evaluate the AD9874.The block diagram in Figure 27 shows the major blocks of the evaluation board. The evaluation board is designed to be flexible allowing the user to configure it for different potential applications. The power supply distribution block provides filtered, adjustable voltages to the various supply pins of the AD9874. In the IF Input signal path,component pads are available to implement different IF impedance matching networks. The LO and CLK signals can be externally applied or internally derived from a user-supplied VCO Module interface daughter board. The reference for the on-chip LO and CLK synthesizers can be applied via the external FREF input or an on-board crystal oscillator.

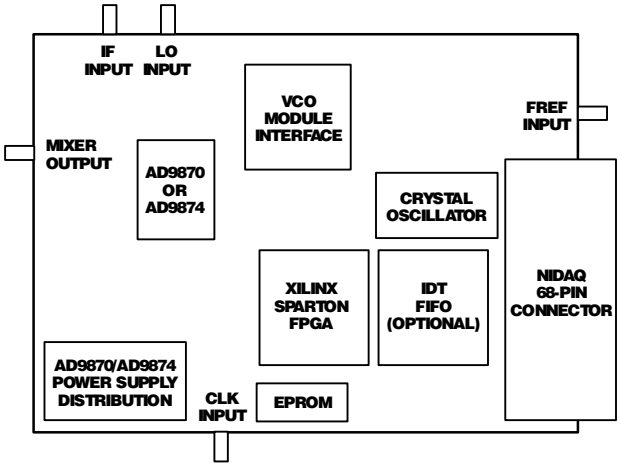


Figure 27. Evaluation Board Patform

The evaluation board is designed to interface to a PC via a National Instruments NI 6533 digital IO card. A XILINX FPGA formats the data between the AD9874 and digital I/O board. Software developed using National Instruments LabVIEW™ (and provided as MS Windows™ executable programs) is supplied for the configuration of the SPI port registers and evaluation of the AD9874 output data. These programs have a convenient graphical user interface allowing for easy access to the various SPI port configuration registers and real time frequency analysis of output data.

For more information on the AD9874 evaluation board including an example layout, please refer to the AD9874-EVB datasheet.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm.)

48-Lead LQFP
(ST-48)