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12-Bit, 160 MSPS 2×/4×/8× Interpolating Dual TxDAC+® D/A Converter

Preliminary Technical Data 8-16-00

AD9773

FEATURES

12 Bit Resolution, 160 MSPS Conversion Rate
Selectable 2×/4×/8× Interpolating Filter
Programmable Channel Gain and Offset Adjustment
Fs/8 Digital Quadrature Modulation Capability
Direct IF Transmission Mode for 70MHz+ IFs
Fully Compatible SPI Port
Excellent AC Performance
- SFDR -70dBc @ 2-35MHz
-WCDMA ACPR -70dB @ IF=16.25 MHz
Internal PLL Clock Multiplier
Selectable Internal Clock Divider
Versatile Clock Input
-Differential/Single Ended
-Sine Wave or TTL/CMOS/LVPECL Compatible
Versatile Input Data Interface
-2's Complement/Straight Binary Data Coding
-Dual Port or Single Port Interleaved Data
Single +3 V Supply Operation
Power Dissipation: <700 mW @ 3V
On-chip 1.2 V Reference, 64-Lead LQFP

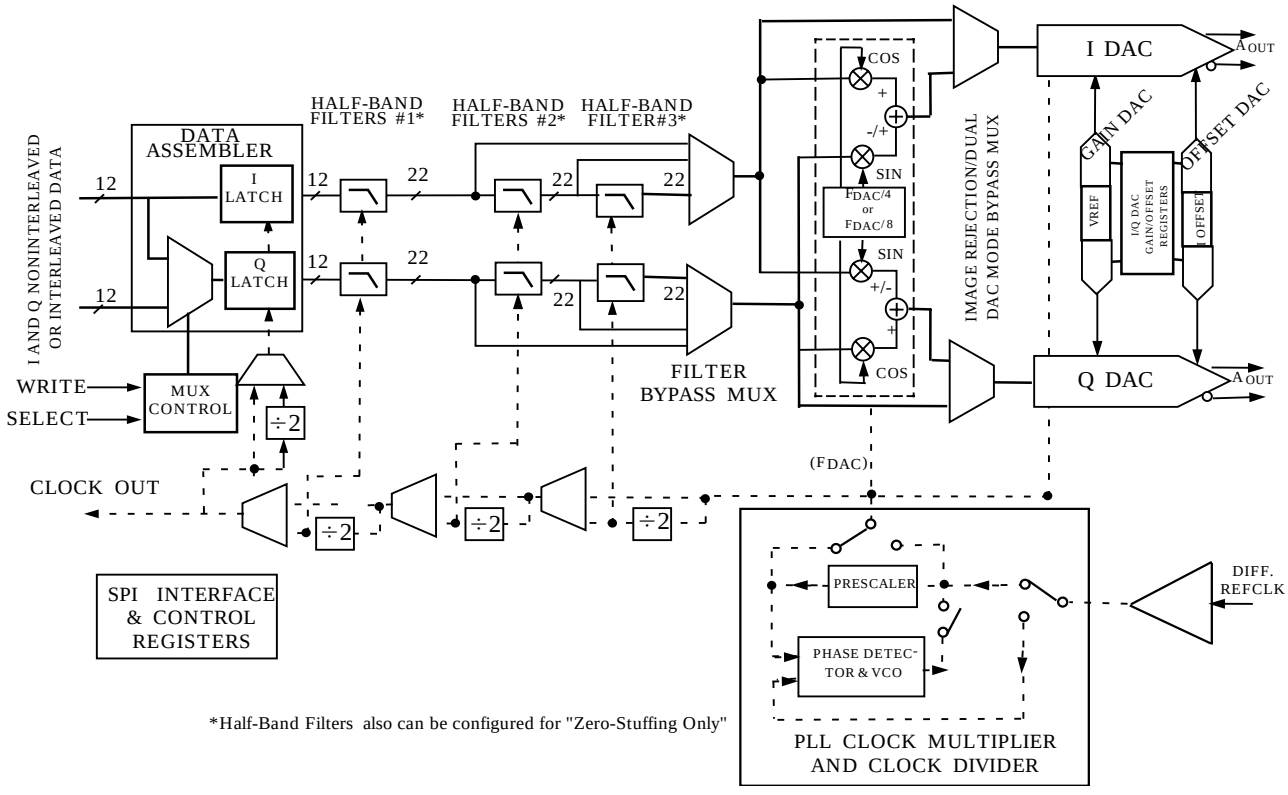
APPLICATIONS

Communications:
Analog Quadrature Modulation Architectures
3G, Multi-Carrier GSM, TDMA, CDMA Systems
Multi-Level QAM Modulators, Instrumentation

PRODUCT DESCRIPTION

The AD9773 is the 12 bit member of the AD977x family of pin-compatible, high performance, programmable 2×/4×/8× interpolating TxDAC+s. The AD977x family features a serial port interface (SPI) providing a high level of programmability thus allowing for enhanced system level options. These options include: selectable 2×/4×/8× interpolation filters; Fs/4 or Fs/8 digital quadrature modulation with image rejection; a direct IF mode; programmable channel gain and offset control; programmable internal clock divider; straight binary or two's complement data interface; and a single port or dual port data interface.

PROGRAMABLE DUAL INTERPOLATION DAC
WITH IMAGE REJECTION/DIGITAL MODULATION



*Half-Band Filters also can be configured for "Zero-Stuffing Only"

BLOCK DIAGRAM

The selectable 2×/4×/8× interpolation filters simplify the requirements of the reconstruction filters while simultaneously enhancing the TxDAC+ family's passband noise/distortion performance. The independent channel gain and offset registers allow the user to calibrate LO feedthrough and sideband suppression errors associated with analog quadrature modulators. The 6 dB of gain adjustment range also can be used to control the output power level of each DAC.

The AD9773 features the ability to perform Fs/4 and Fs/8 digital modulation and image rejection when combined with an analog quadrature modulator. In this mode, the AD9773 would accept I and Q complex data (representing a single or multicarrier waveform), generate a quadrature modulated IF signal along with its orthogonal representation via its dual DACs, and present these two reconstructed orthogonal IF carriers to an analog quadrature modulator to complete the image rejection upconversion process. Another digital modulation mode (i.e. the Direct IF Mode) allows the original baseband signal representation to be frequency translated such that pairs of images fall at multiples of 1/2 the DAC update rate.

The AD9773 family includes a flexible clock interface accepting differential or single-ended sinewave or digital logic inputs. An internal PLL clock multiplier is also included to generate the necessary on-chip high frequency clocks. It can also be disabled to allow the use of a higher performance external clock source. An internal programmable divider simplifies clock generation in the converter when using an external clock source. A flexible data input interface allows for straight binary or 2's complement formats as well as supports single port interleaved or dual port data.

Dual high performance TxDAC+s provides a differential current output programmable over a 2-20mA range. The AD977X is manufactured on an advanced 0.35 micron CMOS process, operates from a single supply of 2.7 V to 3.6 V and consumes <750 mW of power.

Targeted at wide dynamic range, Multi-Carrier and Multi-Standard systems, the superb baseband performance of the AD977X is ideal for Wideband-CDMA, Multi-Carrier CDMA, Multi-Carrier TDMA, Multi-Carrier GSM and high performance systems employing high order QAM modulation schemes. The image rejection feature simplifies and can help to reduce the number of signal band filters needed in an transmit signal chain. The direct IF mode helps to eliminate a costly mixer stage for a variety of communications systems.

PRODUCT HIGHLIGHTS

1. The AD9773 is the 12 bit member of the AD977x family of pin-compatible, high performance, programmable 2×/4×/8× interpolating TxDAC+s.

2. 2×/4×/8× User Selectable Interpolating Filter eases data rate and output signal reconstruction filter requirements.

3. User selectable 2's Complement/Straight Binary Data Coding.

4. User programmable Channel Gain Control over 1 dB range in 0.01dB increments

5. User programmable Channel Offset +/-10% over the FSR

6. Direct IF Transmission capability for 70MHz +IFs through a novel digital mixing process

7. Fs/8 Digital Quadrature Modulation and user selectable image rejection to simplify /remove cascaded SAW filter stages

8. Ultra high speed 400 MSPS DAC conversion rate.

9. Internal Clock Divider provides data rate clock for easy interfacing.

10. Flexible Clock Input with Single Ended or Differential Input, CMOS or 1V pk-pk LO Sinewave input capability.

11. Low Power: Complete CMOS DAC operates on <700 mW from a 2.7 V to 3.6 V single supply. The 20ma full-scale current can be reduced for lower power operation, and a several sleep functions are provided to reduce power during idle periods.

12. On-chip Voltage Reference: The AD9773 includes a 1.20 V temperature-compensated bandgap voltage reference.

13. Small 64 lead LQFP

AD9773–SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +3 V, CLKVDD = +3 V, DVDD = +3 V, PLLVDD = +3v, I_{OUTFS} = 20 mA, unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNITS
RESOLUTION	12			bits
DC Accuracy[1]				
Integral Non-Linearity				LSB
Differential Non_Linearity				LSB
Monotonicity				
ANALOG OUTPUT				
Offset Error				% of FSR
Gain Error (Without Internal Reference)				% of FSR
Gain Error (With Internal Reference)				% of FSR
Full-Scale Output Current[2]		20		mA
Output Compliance Range	–1.0		+1.25	V
Output Resistance		200		kΩ
Output Capacitance		3		pF
REFERENCE OUTPUT				
Reference Voltage	1.14	1.20	1.26	V
Reference Output Current[3]		1		µA
REFERENCE INPUT				
Input Compliance Range	0.1		1.25	V
Reference Input Resistance (REFLO = 3 V)			10	MΩ
Small Signal Bandwidth		0.5		MHz
TEMPERATURE COEFFICIENTS				
Unipolar Offset Drift				ppm of FSR/°C
Gain Drift (Without Internal Reference)				ppm of FSR/°C
Gain Drift (With Internal Reference)				ppm of FSR/°C
ReferenceVoltage Drift				ppm/°C
POWER SUPPLY				
AVDD				
Voltage Range	2.7	3.0	3.6	V
Analog Supply Current (I_{AVDD})				mA
I_{AVDD} in SLEEP Mode				mA
CLKVDD				
Voltage Range	2.7	3.0	3.6	V
Clock Supply Current (I_{CLKVDD})				mA
PLLVDD				
Voltage Range	2.7	3.0	3.6	V
PLL Multiplier Supply Current (I_{PLLVDD})				mA
DVDD				
Voltage Range	2.7	3.0	3.6	V
Digital Supply Current (I_{DVDD})				mA
Nominal Power Dissipation		<700		mW
Power Supply Rejection Ratio – AVDD				% of FSR/V
Power Supply Rejection Ratio – DVDD				% of FSR/V
OPERATING RANGE	–40		+85	°C

NOTES
[1]Measured at I_{OUTA} driving a virtual ground.
[2]Nominal full-scale current, I_{OUTFS}, is 32× the I_{REF} current.
[3]Use an external amplifier to drive any external load.

Specifications subject to change without notice.

AD9773–SPECIFICATIONS

DYNAMIC SPECIFICATIONS

(T_{MIN} to T_{MAX}, AVDD = +3 V, CLKVDD = +3 V, DVDD = +3 V, PLLVDD = 0 V, I_{OUTFS} = 20 mA, Differential Transformer Coupled Output, 50Ω Doubly Terminated, unless otherwise noted)

Parameter	Min	Typ	Max	Units
DYNAMIC PERFORMANCE				
Maximum DAC Output Update Rate (f_{DAC})	400			MSPS
Output Settling Time (t_{ST}) (to 0.025%)				ns
Output Propagation Delay[1] (t_{PD})				ns
Output Rise Time (10% to 90%)[2]				ns
Output Fall Time (10% to 90%)[2]				ns
Output Noise (I_{OUTFS} = 20 mA)				pA√Hz
AC LINEARITY–BASEBAND MODE				
Spurious-Free Dynamic Range (SFDR) to Nyquist (f_{OUT} = 0 dBFS)				
f_{DATA} = MSPS; f_{OUT} = MHz				dBc
f_{DATA} = MSPS; f_{OUT} = MHz				dBc
f_{DATA} = MSPS; f_{OUT} = MHz				dBc
f_{DATA} = MSPS; f_{OUT} = MHz				dBc
f_{DATA} = MSPS; f_{OUT} = MHz				dBc
f_{DATA} = MSPS; f_{OUT} = MHz				dBc
Two-Tone Intermodulation (IMD) to Nyquist (f_{OUT1} = f_{OUT2} = –6 dBFS)				
f_{DATA} = MSPS; f_{OUT1} = MHz; f_{OUT2} = MHz				dBc
f_{DATA} = MSPS; f_{OUT1} = MHz; f_{OUT2} = MHz				dBc
f_{DATA} = MSPS; f_{OUT1} = MHz; f_{OUT2} = MHz				dBc
f_{DATA} = MSPS; f_{OUT1} = MHz; f_{OUT2} = MHz				dBc
f_{DATA} = MSPS; f_{OUT1} = MHz; f_{OUT2} = MHz				dBc
f_{DATA} = MSPS; f_{OUT1} = MHz; f_{OUT2} = MHz				dBc
Total Harmonic Distortion (THD)				
f_{DATA} = MSPS; f_{OUT} = MHz; 0 dBFS				dB
f_{DATA} = MSPS; f_{OUT} = MHz; 0 dBFS				dB
Signal-to-Noise Ratio (SNR)				
f_{DATA} = MSPS; f_{OUT} = MHz; 0 dBFS				dB
f_{DATA} = MSPS; f_{OUT} = MHz; 0 dBFS				dB
Adjacent Channel Power Ratio (ACPR)				
WCDMA with MHz BW, MHz Channel Spacing				
IF = 16 MHz, f_{DATA} = 65.536 MSPS				dBc
IF = 32 MHz, f_{DATA} = 131.072 MSPS				dBc
Four-Tone Intermodulation				
MHz, MHz, MHz and MHz at –12 dBFS				dBFS
(f_{DATA} = MSPS, Missing Center)				
AC LINEARITY–IF MODE				
Four-Tone Intermodulation at IF = MHz				
MHz, MHz, MHz and MHz at dBFS				dBFS
f_{DATA} = MSPS, f_{DAC} = MHz				

NOTES

[1]Propagation delay is delay from CLK input to DAC update.

[2]Measured single-ended into 50 Ω load.

Specifications subject to change without notice.

AD9773–SPECIFICATIONS

DIGITAL SPECIFICATIONS

Parameter	Min	Typ	Max	Units
DIGITAL INPUTS				
Logic "1" Voltage	2.1	3		V
Logic "0" Voltage		0	0.9	V
Logic "1" Current[1]	–10		+10	µA
Logic "0" Current	–10		+10	µA
Input Capacitance		5		pF
CLOCK INPUTS				
Input Voltage Range	0		3	V
Common-Mode Voltage	0.75	1.5	2.25	V
Differential Voltage	0.5	1.5		V
PLL CLOCK ENABLED				
Input Setup Time (t_S)	0.2			ns
Input Hold Time (t_H)	1.8			ns
Latch Pulsewidth (t_{LPW})	1.5			ns
PLL CLOCK DISABLED				
Input Setup Time (t_S)	-1.2			ns
Input Hold Time (t_H)	3.2			ns
Latch Pulsewidth (t_{LPW})	1.5			ns
CLK/PLLLOCK Delay (t_{OD})		TBD		ns

Specifications subject to change without notice.

DIGITAL FILTER SPECIFICATIONS