12–Bit, 80 / 105 MSPS IF Sampler A/D Converter

Advanced Technical Data 1/7/00 AD9433

The AD9433 is an 12-bit monolithic sampling analog–to–digital converter with an on–chip track–and–hold circuit and is optimized for low cost, low power, small size and ease of use. The product operates up to 105 Msps conversion rate and is optimized for outstanding dynamic performance in wideband and high IF carrier systems.

The ADC requires a +5V and a +3.3V power supply and a flexible clock duty differential encode clock for full performance operation. No external reference or driver components are required for many applications. The digital outputs are TTL/CMOS compatible and a separate output power supply pin supports interfacing with 3.3V or 2.5V logic.

A user selectable on-chip dithering allows minimum SFDR performance of –90dBc from DC to 250MHz. An IF band select allows optimized SINAD vs SFDR for a particular carrier frequency.

The encode clock supports either differential or single-ended and is PECL compatible. Immunity to clock duty cycle variations and an output data format select option of two's complement or offset binary are also supported.

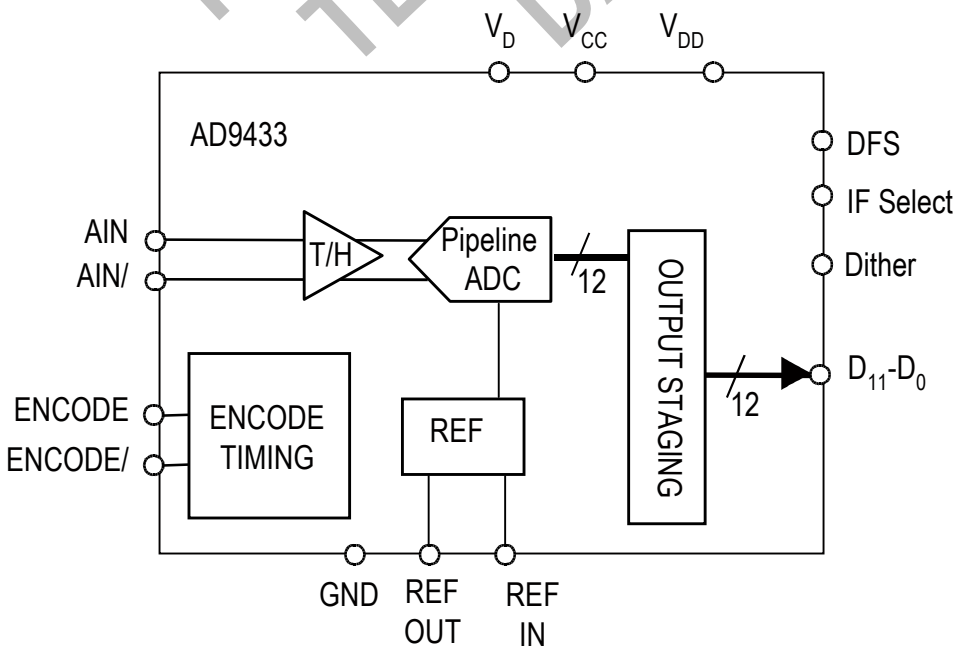
Fabricated on an advanced BiCMOS process, the AD9433 is available in a 52 pin surface mount plastic package (52 LQFP) specified over the industrial temperature range (–40°C to +85°C) and is pin compatible with the AD9432.

FEATURES
IF Sampling up to 350MHz
IF band select for optimized SINAD and SFDR
On–chip reference and track/hold
Scalable voltage reference
Selectable on-chip dither for improved SFDR & THD
Excellent Linearity:
- **DNL = +/- 0.3 lsb (typ)**
- **INL = +/- 0.6 lsb (typ)**

700 MHz Full Power Analog Bandwidth
SNR = 69dB @ Fin up to Nyquist
SFDR = -90dBc @ Fin up to 250 MHz
THD = -90dBc @ Fin up to 250 MHz
Power dissipation = 900mW typical at 105Msps
Input voltage range of 1Vp-p and 2Vp-p
Two's complement or Straight binary data format
+5.0V and +3.3V Supply Operation
+2.5V to 3.3V TTL/CMOS outputs
Clock Duty Cycle Stablizer.

APPLICATIONS
Wireless and Wired Broadband Communications
- **Wideband carrier frequency systems**

Communications Test Equipment
"IF Sampling" schemes
Radar and Satellite sub-systems



REV 0.1

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AD9433—TARGET SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_{DD} = 3.0V, V_{CC} = 5.0V; external reference; ENCODE = 105 Msps, unless otherwise noted)

Parameter	Temp	Test Level	AD9433BST-105 Min	Typical	Max	Units
RESOLUTION				12		bits
DC ACCURACY						
Differential Nonlinearity	+25°C	I	-0.6	±0.3	+0.6	LSB
	Full	VI				LSB
Integral Nonlinearity	+25°C	I		±0.75		LSB
	Full	VI				LSB
No Missing Codes	Full	VI		Guaranteed		
Gain Error [1]	+25°C	I		±1		% FS
	Full	VI				% FS
Gain Tempco[1]	Full	V		150		ppm/°C
ANALOG INPUT						
Input Voltage Range (with respect to AIN\)	Full	V		±1.0		V p–p
Common Mode Voltage	Full	V		3.0		V
Input Offset Voltage	Full	VI		±0		mV
Input Capacitance	+25°C	V		4		pF
Input Resistance	Full	VI	2	3	3	kΩ
Analog Bandwidth, Full Power	+25°C	V		500		MHz
ANALOG REFERECE						
Reference Voltage	Full	VI	2.4	2.5	2.6	V
Tempco	Full	V		50		ppm/°C
Input Bias Current	Full	VI		15		µA
SWITCHING PERFORMANCE						
Maximum Conversion Rate	Full	VI	105			Msps
Minimum Conversion Rate	Full	IV			10	Msps
Encode Pulse Width High (t_{EH})	+25°C	IV	4.5	5.0		ns
Encode Pulse Width Low (t_{EL})	+25°C	IV	4.5	5.0		ns
Aperture Delay (t_A)	+25°C	V		2.0		ns
Aperture Uncertainty (Jitter)	+25°C	V		0.3		ps rms
Output Valid Time (t_V) [2]	Full	VI		6.0		ns
Output Propagation Delay (t_{PD})[2]	Full	VI	4.5	8.0	9.0	ns
Output Rise Time (t_R) [2]	Full	VI		2.1		ns
Output Fall Time (t_F)	Full	VI		1.9		ns
Output Fall Time (t_F)						
Output Fall Time (t_F)						
DIGITAL INPUTS						
Encode Input Common Mode	Full	V	1.2	1.6	2.0	V
Differential Input (Enc,Enc\)	Full	V		750		mV
Single Ended						
Logic "1" Voltage	Full	IV	0			V
Logic "0" Voltage	Full	IV			0.9	V
Input Resistance	Full	VI		5		kΩ
Input Capacitance	+25°C	V		4.5		PF
DIGITAL OUTPUTS						
Logic "1" Voltage (V_{DD} = +3.3V)	Full	VI	V_{DD}-0.05			V
Logic "0" Voltage (V_{DD} = +3.3V)	Full	VI			0.05	V
Output Coding				Two's complement or Binary		
POWER SUPPLY						
Power Dissipation [3]	Full	VI		900		mW
Power Supply Rejection Ratio (PSRR)	+25°C	I		±5		mV/V

Parameter	Temp	Test Level	AD9433BST-105 Min	Typical	Max	Units
DYNAMIC PERFORMANCE[4]						
Signal–to–Noise Ratio (SNR)						
(Without Harmonics)						
f_{IN} = 10 MHz	+25°C	I		69		dB
f_{IN} = 49 MHz	+25°C	I		69		dB
f_{IN} = 70 MHz	+25°C	I		69		dB
f_{IN} = 150 MHz	+25°C	I		68.8		dB
f_{IN} = 250 MHz	+25°C	I		68.8		dB
Signal–to–Noise Ratio (SINAD)						
(With Harmonics)						
f_{IN} = 10 MHz	+25°C	I		68		dB
f_{IN} = 49 MHz	+25°C	I		68		dB
f_{IN} = 70 MHz	+25°C	I		68		dB
f_{IN} = 150 MHz	+25°C	I		67.8		dB
f_{IN} = 250 MHz	+25°C	I		67.8		dB
Effective Number of Bits						
f_{IN} = 10 MHz	+25°C	I		11.2		bits
f_{IN} = 49 MHz	+25°C	I		11.2		bits
f_{IN} = 70 MHz	+25°C	I		11.2		bits
f_{IN} = 150 MHz	+25°C	I		11.0		bits
f_{IN} = 250 MHz	+25°C	I		11.0		bits
2^{nd} & 3^{rd} Harmonic Distortion						
f_{IN} = 10 MHz	+25°C	I		-90		dBc
f_{IN} = 49 MHz	+25°C	I		-90		dBc
f_{IN} = 70 MHz	+25°C	I		-90		dBc
f_{IN} = 150 MHz	+25°C	I		-90		dBc
f_{IN} = 250 MHz	+25°C	I		-90		dBc
4^{th} or higher Harmonic Distortion						
f_{IN} = 10 MHz	+25°C	I		-87		dBc
f_{IN} = 49 MHz	+25°C	I		-87		dBc
f_{IN} = 70 MHz	+25°C	I		-85		dBc
f_{IN} = 150 MHz	+25°C	I		-85		dBc
f_{IN} = 250 MHz	+25°C	I		-85		dBc
Two–Tone Intermod Distortion (IMD)						
f_{IN} = 10 MHz	+25°C	V		Tbf		dBc
f_{IN} = 20 MHz	+25°C	V		Tbf		dBc
f_{IN} = 47 MHz	+25°C	V		Tbf		dBc

NOTES
1. Gain error and gain temperature coefficients are based on the ADC only (with a fixed 2.5V external reference and 2Vp-p differential input.).
2. t_V and t_{PD} are measured from a 1.5V level of the ENCODE input to the 50%/50% levels of the digital outputs swing. The digital output load during test is not to exceed an ac load of 10pF or a dc current of +/-40 µA.
3. Power dissipation measured with encode at rated speed and a dc analog input.
4. SNR/harmonics based on an analog input voltage of –0.5dBFS referenced to a 2V full-scale input range.