ANALOG DEVICES

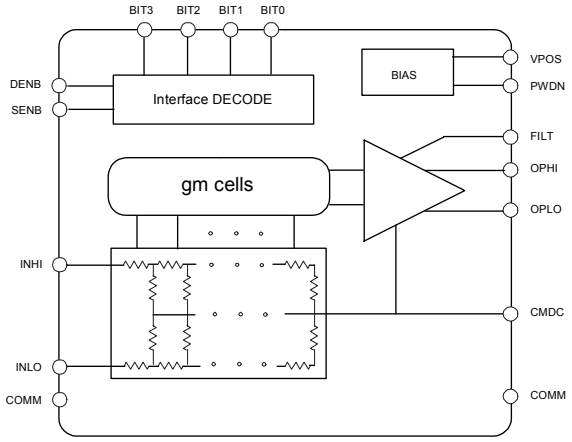
45-dB Digital VGA LF to 500MHz

PRELIMINARY TECHNICAL DATA

AD8369

FEATURES

- **Very Flat AC Response to 400MHz, ±.5dB**
- **Digital Variable Gain, from -5dB to +40dB (R_L=1kΩ)**
- **3dB Step Size**
- **Parallel or Serial 4-bit Interface**
- **Differential Input and Output**
  - **200Ω Differential Input**
  - **200Ω Differential Output**
- **High-Efficiency Output Stage**
- **Operation from Supply Voltages from 3.0 - 5.5 V**
- **Rapid Power-Down to less than 300 μA max**



APPLICATIONS

- **IF Sampling Receivers**
- **Cellular/PCS Base Stations**

PRODUCT DESCRIPTION

The AD8369 is a high-performance digitally controlled variable gain amplifier for use from very low frequencies to 550MHz, with a -3dB frequency of 700MHz at full gain (40dB, Rload=1k) and essentially constant response at all gains. The AD8369 delivers excellent distortion performance, two-tone intermodulation distortion is 63dBc at 150MHz for 10MHz spacing. Digital control of the AD8369 is achieved using a 4-bit serial or parallel interface. The mode of digital control is selected by connecting a single pin to ground or the positive supply.

Variable gain is achieved via two methods. Six dB gain steps are implemented using the X-AMP approach, where the input signal is scaled by a differential R-2R ladder network. The ladder also sets the input impedance at 200 ohms differential. Three dB steps are implemented at the output of the amp via a signal subtraction method. The output impedance is set via on chip resistors across the differential output pins. Consequently the load that is presented to the part will affect the overall gain of the amplifier.

Standard CMOS levels can drive the digital interface. Control pins (SENB and DENB) when left open are pulled to levels that put the part in the parallel transparent mode. The Data pins are pulled low if left unconnected. In serial mode, Bit0 is the serial data input and Bit1 is clock. The DENB has the same function in both the serial and parallel modes. Data is latched while the DENB pin is low and transparent when DENB is high. The AD8369 may be powered on or off by a voltage applied to the ENBL pin. When this voltage is at logic LO, the total dissipation drops to the microwatt range. For a logic HI, the chip powers-up rapidly to its nominal quiescent current of 34mA at 25º C.

The AD8369 is fabricated on Analog Devices proprietary, high performance 25GHz silicon Bipolar IC process. The AD8369 is available in a 16pin TSSOP package for the industrial temperature range of –40°C to +85°C. A device populated evaluation board is available.

Patents Pending

Preliminary Rev. A 8/10/01

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AD8369-SPECIFICATIONS (V_S=5V, T=25°C, Z_O = 200Ω, Frequency = 70MHz unless otherwise noted)

Parameters	Conditions	Min	Typ	Max	Units
OVERALL FUNCTION					
Frequency Range	V_S=5V, T=25°C, Z_O = 200Ω	Note 1		550	MHz
INPUT STAGE					
Maximum Input	Maximum Peak Input Voltage			TBD	Vp-p
Input Resistance// Capacitance	From INHI to INLO, Freq = 70 MHz		200		Ω//pF
Input Noise Spectral Density	At max gain		TBD		nV/√Hz
GAIN CONTROL INTERFACE					
Gain Range			45		dB
Maximum Gain	Gain Code F (1 1 1 1)		40		dB
Minimum Gain	Gain Code 0 (0 0 0 0)		-5		dB
Gain Step Size			3		dB
Gain Step Accuracy			TBD		dB
Gain Step Response	Gain Code 0 (0000) to Gain Code 1 (0001)		TBD		µs
OUTPUT STAGE					
Maximum Output Voltage	R_L ≥ 1kΩ		TBD		Vpp
Output Resistance// Capacitance	From OPHI to OPLO		200		Ω//pF
f = 70 MHz					
Gain	Gain Code F (1 1 1 1)		35		dB
Noise Figure	At Max Gain		6.8		dB
Output IP3	f1 = 69.5 MHz, f2 = 70.5MHz, At Max Gain		22		dBm
Output 1dB Compression Point	At Max Gain		-1		dBm
f = 140 MHz					
Gain	All bits high (1 1 1 1)		35		dB
Noise Figure	At Max Gain		6.8		dB
Output IP3	f1 = 139.5 MHz, f2 = 140.5MHz, At Max Gain		18		dBm
Output 1dB Compression Point	At Max Gain		TBD		dBm
f = 190 MHz					
Gain	All bits high (1 1 1 1)		35		dB
Noise Figure	At Max Gain		6.9		dB
Output IP3	f1 = 189.5 MHz, f2 = 190.5MHz, At Max Gain		17		dBm
Output 1dB Compression Point	At Max Gain		TBD		dBm
f = 240 MHz					
Gain	All bits high (1 1 1 1)		35		dB
Noise Figure	At Max Gain		6.9		dB
Output IP3	f1 = 239.5MHz, f2 = 240.5MHz, At Max Gain		15		dBm
Output 1dB Compression Point	At Max Gain		TBD		dBm

AD8369-SPECIFICATIONS (V_S=5V, T=25°C, Z_O = 200Ω, Frequency = 70MHz unless otherwise noted)

POWER INTERFACE				
Supply Voltage		3.0	5.5	V
Quiescent Current	PWDN high		34	mA
vs. Temperature	-30°C ≤ T_A ≤ 85°C			mA
Disable Current	PWDN low		750	µA
vs. Temperature	-30°C ≤ T_A ≤ 85°C			uA
MODE CONTROL INTERFACE				
Mode LO Threshold	Device in parallel mode of operation		V_S / 2	V
Mode HI Threshold	Device in serial mode of operation		V_S / 2	V
POWER DOWN INTERFACE				
Threshold			1.7	V
Response Time	Time delay following LO to HI transition until device meets full specifications.		TBD	µs
Input Bias Current	PWDN = 5 V		170	µA

Notes

1) The lowest frequency of operation is determined by the capacitor on pin FILT.
2) See applications section for reactive matching networks

TIMING REQUIREMENTS (V_S=5V, T=25°C, F_{CLK} = 8MHz unless otherwise noted)

Parameter	Min	Typ	Max	Units
Clock Pulse Width (T_{PW})	TBD			ns
Clock Period (T_{CK})	TBD			ns
Setup Time Data vs. Clock (T_{DS})	TBD			ns
Setup Time Data Enable vs. Clock (T_{ES})	TBD			ns
Hold Time Data Enable vs. Clock (T_{EH})	TBD			ns

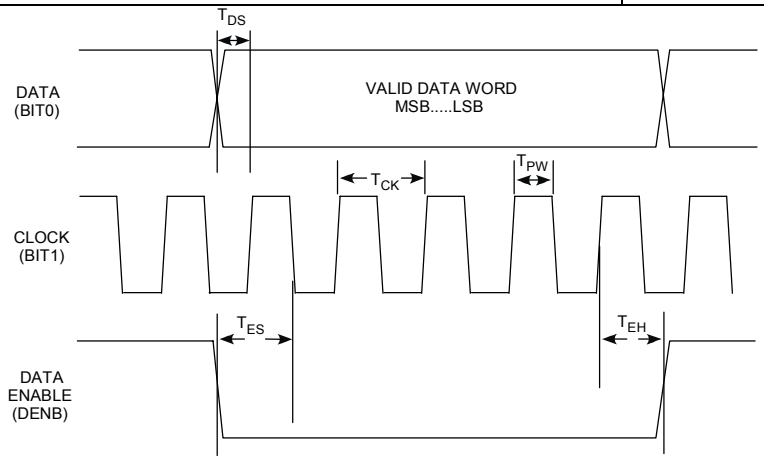


Figure 1. Serial Interface Timing Diagram

Desired Gain (dB)	Equivalent Gain (V_{OUT}/V_{IN})	BIT3 (MSB)	BIT2	BIT1	BIT0 (LSB)
-5	0.562341	0	0	0	0
-2	0.794328	0	0	0	1
+1	1.122018	0	0	1	0
+4	1.584893	0	0	1	1
+7	2.238721	0	1	0	0
+10	3.162278	0	1	0	1
+13	4.466836	0	1	1	0
+16	6.309573	0	1	1	1
+19	8.912509	1	0	0	0
+22	12.58925	1	0	0	1
+25	17.78279	1	0	1	0
+28	25.11886	1	0	1	1
+31	35.48134	1	1	0	0
+34	50.11872	1	1	0	1
+37	70.79458	1	1	1	0
+40	100	1	1	1	1

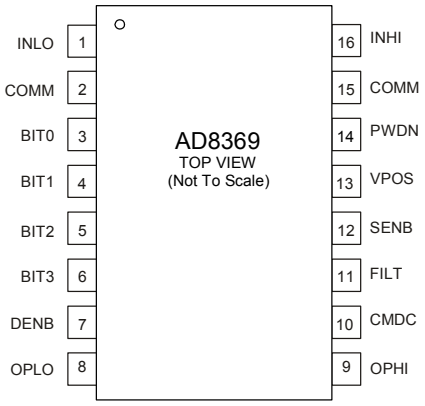
Table 1. Gain for Multiple Values of Gain Code for 1kΩ Load.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage VPOS ……...…….5.5V
PWDN Voltage ……..... V_S + xV
SENB Select Voltage …… V_S + xV
Input Volage, INHI - INLO…….xV
Internal Power Dissipation ….……...TBD
θ_{JA} ……..……150 °C/W
Maximum Junction Temperature ……..…+125° C
Operating Temperature Range …..-40° C to +85° C
Storage Temperature Range …….-65° C to +150° C
Lead Temperature Range (Soldering 60 sec)..+300° C

***Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.**

PIN CONFIGURATION



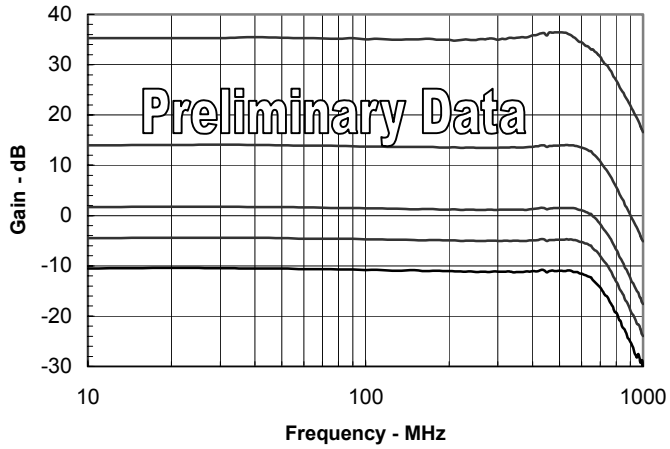
PIN FUNCTION DESCRIPTIONS

Pin	Name	Function
1	INLO	Balanced Differential Input. Internally biased, should be AC coupled.
2	COMM	Device Common. Connect to low impedance ground.
3	BIT0	Gain Selection Least Significant Bit. Used as DATA input signal when in serial mode of operation.
4	BIT1	Gain Selection Control Bit. Used as CLOCK input pin when in serial mode of operation.
5	BIT2	Gain Selection Control Bit. Inactive when in serial mode of operation.
6	BIT3	Gain Selection Most Significant Bit. Inactive when in serial mode of operation.
7	DENB	Data Enable Pin**.** Data writes to register when low. Data is latched during low to high transition. See Figure 1 for timing diagram.
8	OPLO	Balanced Differential Output. Biased to mid supply, should be AC coupled
9	OPHI	Balanced Differential Output. Biased to mid supply, should be AC coupled
10	CMDC	Common Mode Decoupling Pin. Connect bypass capacitor to ground for additional common mode supply decoupling.
11	FILT	High Pass Filter Connection. Used to set high pass corner frequency .
12	SENB	Serial or Parallel Interface Select. Connect SENB to VPOS for serial operation. Connect SENB to COMM for parallel operation.
13	VPOS	Positive Supply Voltage, V_S .+ 3V to +5.5V.
14	PWDN	Power Down Pin. Device is active when high, pull pin low to disable device.
15	COMM	Device Common. Connect to low impedance ground.
16	INHI	Balanced Differential Input. Internally biased, should be AC coupled.

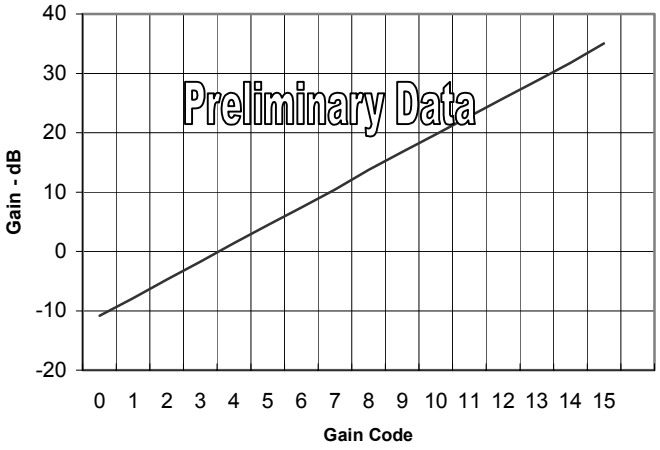
CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8369 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy [>250 V HBM] electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

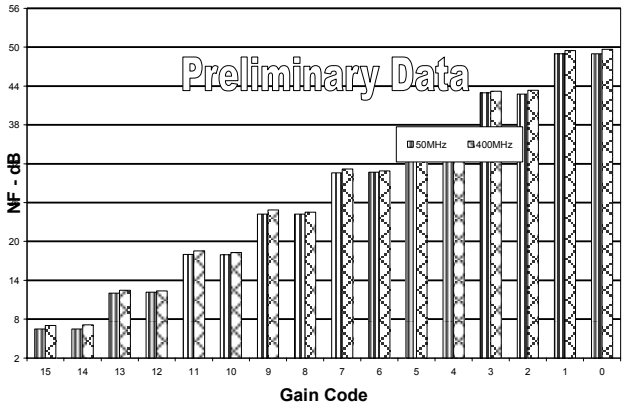
Model	Temp. Range	Package Description	Package Option
AD8369ARU	-40 °C to +85 °C	Tube, 16-Lead TSSOP	RU-16
AD8369ARU-REEL7		7" Tape and Reel	
AD8369-EVAL		Evaluation Board	



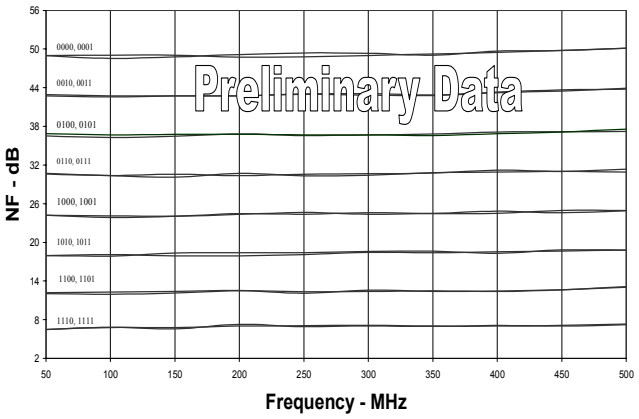
TPC 1. Frequency Response versus Gain Code (ref 200Ω load)



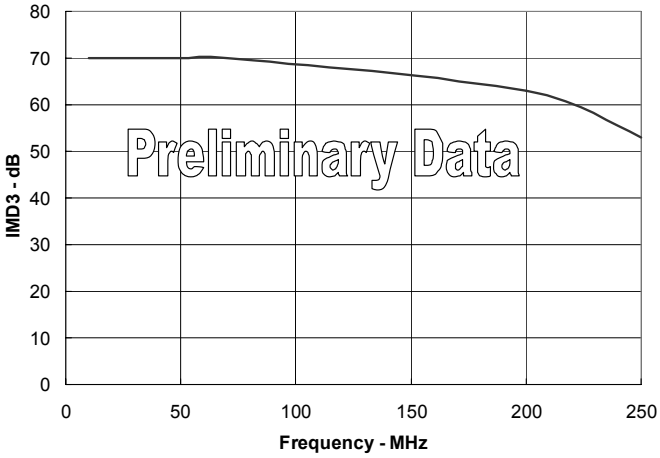
TPC 2. Gain verus Gain Cod e (ref 200Ω load)



TPC 3. NoiseFigurversus Gain Code (ref 200Ω load)



TPC 4. Noise Figure versus Frequency (ref 200Ω load)



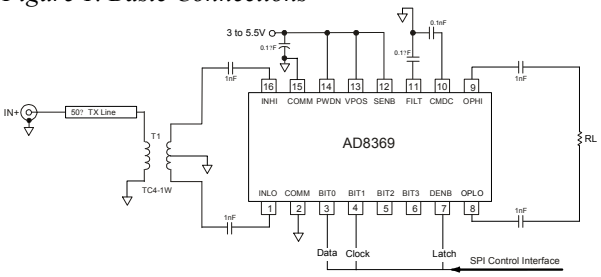
TPC 5. IMD3 versus Frequency at Maximum Gain V_{out}=1Vpp Composite, Rload=1 kΩ

Rev. A 8/10/2001

Basic Connections

The AD8369 is a digitally controlled variable gain amplifier designed to operate in a 200 Ω system. The differential 200 Ω input and output impedances allow for easy impedance matching and gain adjustment in typical high performance intermediate frequency (IF) signal chain designs.

Figure 1. Basic Connections



The AD8369 is typically used as an IF VGA in the receive and transmit portions of the signal chain. Figure 1 shows the basic connections for operating the AD8369 and Figure 2 shows a block diagram of a typical application.

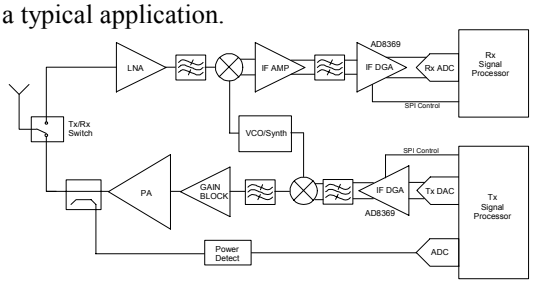


Figure 2. Typical Signal Chain Example

A supply voltage of +3.0 V to +5.5 V is required for the AD8369. The supply to the VPOS pin should be decoupled with a low inductance 0.1µF surface mount ceramic capacitors, close to the device. Additional supply decoupling may be attained using a small series resistance followed by a shunt capacitor to ground, this should help to ensure clean supply voltage to the AD8369.

The input to the AD8369 is a 200 Ω differential resistive ladder network. A broadband 50Ω input match can be achieved by using an impedance transformer as shown in figure 1. The impedance transformer not only transforms a 50 Ω input to a 200 Ω value, but can also be used to convert a single ended input signal to a balanced differential output. Most applications will only require operation over a narrow band of frequencies. For narrow band applications it may be more efficient to use a reactive matching network as in the example of figure 3. In this example the input signal from the SAW filter is transformed to match the 200 Ω input impedance of the AD8369 using a step up matching network. Network selection is highly dependent upon the frequency of operation and driving impedance of the preceding stage. For example, if the SAW filter presents a 50Ω output impedance at 70MHz, LS = 100 nH and CP = 18 pF will transform the 50Ω output to match the 200Ω input of the AD8369.

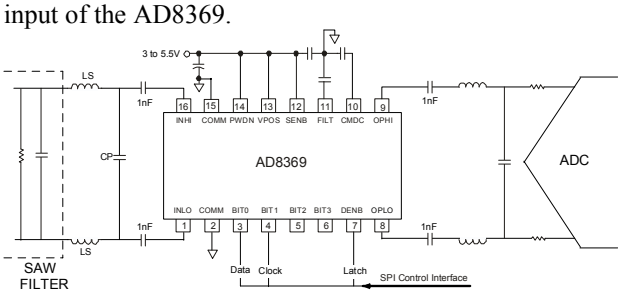


Figure 3. IF Sampling Receiver Example

Evaluation Board

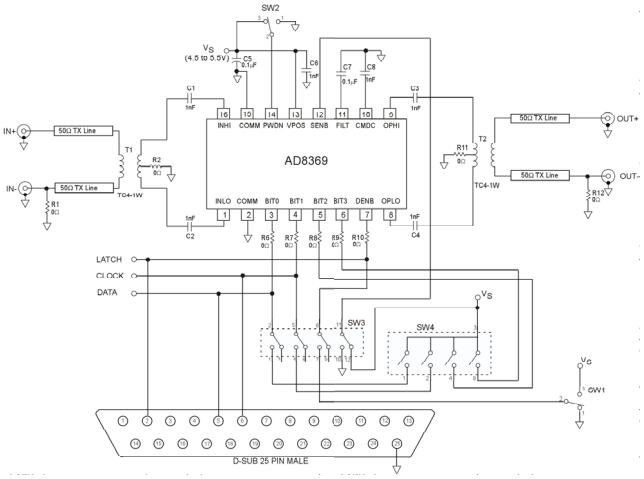


Figure 4. Evaluation Board Schematic

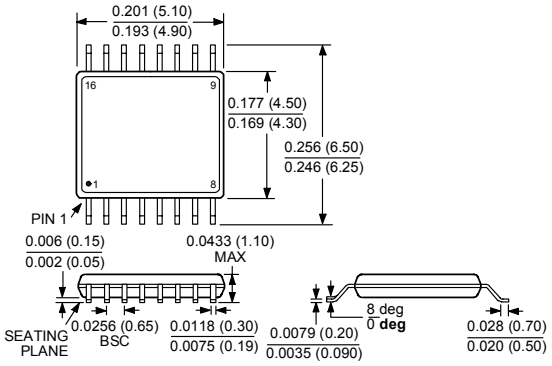
The evaluation board allows for quick testing of the AD8369 using standard 50Ω test equipment. Transforms T1 and T2 are used to transform 50Ω source and load terminations to the desired 200 Ω reference impedance. This allows for broadband operation of the device without a need to pay particular attention to impedance matching.

The evaluation board comes with the AD8369 control software which allows for serial gain control from most computers. By simply adjusting the slider bar in the control software, the gain code is automatically updated to the AD8369. It is necessary to set SW3 to 'SER' for the control software to function normally.

Table II Evaluation Board Configuration Options

Component	Function	Default Condition
VPOS, GND	**Supply and Ground Vector Pins**	Not Applicable
SW1	**Data Enable:** Set to position A for pass through mode of operation. Ser to position B to latch the gain setting.	Not Applicable
SW2	**Device Enable:** When in the PWDN position, the PWDN pin will be connected to ground and the AD8369 will be disabled. The device is enabled when the switch is in the PWUP position, connecting PWDN pin to VPOS.	Not Applicable
SW3, R5	**Serial/Parallel Selection :** The device will respond to serial control inputs from connector P1 when the switch is in the SER position. Parallel operation is achieved when in PAR position. Device can be hardwired for parallel mode of operation by placing 0Ω resistor in position R5.	Not Applicable R5 = open (Size 0603)
SW4	**Parallel Interface Control:** Used to hardwire BIT0 through BIT3 to desired gain code when in parallel mode of operation. The switch functions as a hexadecimal to binary encoder (Gain Code 0 = 0000, Gain Code F = 1111).	Not Applicable
C1, C2, C3, C4	**AC Coupling Capacitors:** Provides AC coupling of the input and output signals.	C1 = C2 = 1nF (Size 0603) C3 = C4 = 1nF (Size 0603)
T1, T2	**Impedance Transformers:** Used to transform the 200Ω input and output impedance to 50Ω.	T1 = T2 = TC4-1W (MiniCircuits)
R1, R2, R11, R12	**Single Ended or Differential:** R2 and R11 are used to ground the center tap of the secondary windings on transformers T1 and T2. R1 and R12 should be used to ground J2 and J7 when used in single ended applications.	R1 = R2 = 0Ω (Size 0603) R11 = R12 =0Ω (Size 0603)
R6, R7, R8, R9, R10	**Control Interface Resistors:** Simple series resistors for each control interface signal. May be replaced with jumpers for interface debug.	R6 = R7 = 0Ω (Size 0603) R8 = R9 =0Ω (Size 0603) R10 = 0Ω (Size 0603)
C5, C6, C8	**Power Supply Decoupling:** Nominal supply decoupling consists of a 0.1µF capacitor followed by a 1nF capacitor to ground as close to the device as possible. C8 provides additional decoupling of the output common mode voltage.	C5 = 0.1µF (Size 0603) C6 = C8 = 1nF (Size 0603)
C7	**High Pass Filter Capacitor:** Used to set high pass corner frequency of output. See applications section for equations.	C7 = 1nF (Size 0603)
C9	**Clock Filter Capacitor:** May be required with some printer ports to minimize overshoot. The clock waveform may be smoothed using a simple filter network established by R7 and C9. Some experimentation may be necessary to determine optimum values.	C9 = open (Size 0603)

OUTLINE DIMENSIONS
16 Lead TSSOP
(RU-16)



Dimensions shown in inches and (mm)