ANALOG DEVICES

500MHz, Linear-in-dB VGA With AGC Detector

Preliminary Technical Data — AD8367

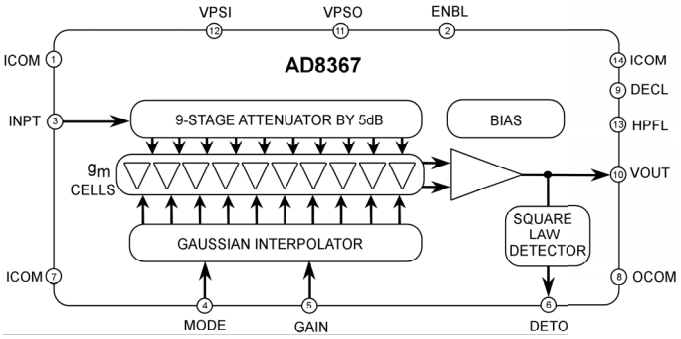
FEATURES

Broad Range Analog Variable Gain
–2.5dB to +42.5dB
Flat AC Response to 500MHz
Linear-in-dB, Scaled 22mV/dB
Resistive Ground Referenced Input
Nominal Zin=200Ω
Maximum Input 300mVrms
High Efficiency Output Stage
1Vrms max O/P
On Chip Square Law Detector
Single Supply Operation: 2.7 V to 5.5 V
Rapid Power-Down to less than 1μA

APPLICATIONS

Power Amplifier Control Loops
Linear IF AGC Amplifiers
PID Control Circuitry
High Speed Data I/O

FUNCTIONAL BLOCK DIAGRAM



14 PIN TSSOP Package

PRODUCT DESCRIPTION

The AD8367 is a high-performance variable gain amplifier for use from arbitrarily low frequencies up to about 500MHz, with a –3dB frequency of 1GHz at full gain (42.5dB) and essentially constant response at all gains. The excellent accuracy of the ac and time domain response is achieved using a new X-AMP™ architecture, the most recent in a series of powerful proprietary concepts for variable gain applications, which far surpasses what can be achieved using the standard solutions based on translinear techniques.

The input is applied to a resistive ladder network, having nine sections each of 5dB, and an input resistance of nominally 200Ω. At maximum gain, the first tap is selected; at progressively lower gains the tap moves smoothly and continuously toward higher attenuation values. The AD8367 is a feedback amplifier – essentially an op-amp with a gain bandwidth product of 100GHz – and is very linear, even at high frequencies. The output third-order intercept is at +20dBV at 100MHz (+27dBm relative to a 200Ω reference), measured at an output level (with Vpos=5V) of 1V pk-pk. The full-scale rise-time of the output is ~2ns.

The analog gain-control interface is very simple to use. It is scaled at 22.2mV/dB, and the control voltage V_G runs from –2.5dB at 0V to 42.5dB at 1V. In the inverse mode of operation, selected by a simple pin strap, it decreases from 42.5dB at V_G =0V to –2.5dB at V_G =1V. This second mode is used in AGC applications, aided by the integrated square-law detector, whose set point is chosen such that the output is leveled to 500mVrms, whatever the waveshape. A single external capacitor sets up the loop averaging time.

The AD8367 may be powered on or off by a voltage applied to the ENBL pin. When this voltage is at a logic LO, the total power dissipation drops to the microwatt range. For a logic HI, the chip powers-up rapidly to its normal quiescent current of 20mA at 25°C. The AD8367 is available in a 14 pin TSSOP package for the industrial temperature range of -40°C to +85°C.

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AD8367-SPECIFICATIONS (V_S=5V, T=25°C, Zo = 200Ω unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
OVERALL FUNCTION					
Frequency Range	To meet all specifications	1		500	MHz
INPUT STAGE					
Maximum Input	Maximum Peak Input Voltage		300		mVrms
Input Resistance	From INPT to ICOM	175	200	225	Ω
GAIN CONTROL INTERFACE (GAIN)					
GAIN Range			45		dB
Maximum Gain	V_{GAIN} = 1V, MODE = 5V	42.5			dB
Minimum Gain	V_{GAIN} = 1V, MODE = 0V			-2.5	dB
Voltage Range	V_{GAIN} Range	0		1	V
Step Response			TBD	TBD	µs
OUTPUT STAGE					
Output Voltage Swing	$R_L \geq 1k\Omega$		4		Vp-p
Output Source Resistance	Series Resistance of Output Buffer	TBD	25	TBD	Ω
f = 10 MHz					
Gain	V_{GAIN} = 1V, MODE = 5V		42.5		dB
Noise Figure	V_{GAIN} = 1V, MODE = 5V		7		dB
	Using Broadband Matching Network, R_L = 50Ω				
Output IP3	f1 = 10 MHz, f2 = 11MHz, V_{GAIN} =0.5V, MODE = 5V		28		dBm
	Using Reactive Matching Network[1], R_L = 50Ω				
Output 1dB Compression Point	V_{GAIN} = 0.5V, MODE = 5V		14		dBm
	Using Broadband Matching Network, R_L = 50Ω				
f = 70 MHz					
Gain	V_{GAIN} = 1V, MODE = 5V		42.5		dB
Noise Figure	V_{GAIN} = 1V, MODE = 5V		7.3		dB
	Using Broadband Matching Network, R_L = 50Ω				
Output IP3	f1 = 70 MHz, f2 = 71MHz, V_{GAIN} = 0.5V, MODE =5V		29		dBm
	Using Reactive Matching Network[1], R_L = 50Ω				
Output 1dB Compression Point	V_{GAIN} = 1V, MODE = 5V		13.4		dBm
	Using Broadband Matching Network, R_L = 50Ω				

AD8367-SPECIFICATIONS

(V_S=5V, T=25°C, Zo = 200Ω unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
f = 140 MHz					
Gain	V_{GAIN} = 1V, MODE = 5V		42.5		dB
Noise Figure	V_{GAIN} = 1V, MODE = 5V		7.8		dB
	Using Broadband Matching Network, R_L = 50Ω				
Output IP3	f1 = 140 MHz, f2 = 141MHz,V_{GAIN}=0.5V, MODE =5V		31.5		dBm
	Using Reactive Matching Network[1], R_L = 50Ω				
Output 1dB Compression Point	V_{GAIN} = 1V, MODE = 5V		13.2		dBm
	Using Broadband Matching Network, R_L = 50Ω				
f = 380 MHz					
Gain	V_{GAIN} = 1V, MODE = 5V		42.5		dB
Noise Figure	V_{GAIN} = 1V, MODE = 5V		9.8		dB
	Using Broadband Matching Network, R_L = 50Ω				
Output IP3	f1 = 380MHz, f2 =381MHz, V_{GAIN} = 0.5V, MODE= 5V		21.5		dBm
	Using Reactive Matching Network[1], R_L = 50Ω				
Output 1dB Compression Point	V_{GAIN} = 1V, MODE = 5V		12.8		dBm
	Using Broadband Matching Network, R_L = 50Ω				
POWER INTERFACE					
Supply Voltage		2.7		5.5	V
Quiescent Current	ENBL high		20		mA
vs. Temperature	-30°C ≤ T_A ≤ 85°C			TBD	mA
Total Supply Current	ENBL high, V_{GAIN} = 1V, MODE = 5V, R_L= 200 Ω (includes load current)		23		mA
Disable Current	ENBL low		1.0		mA
vs. Temperature	-30°C ≤ T_A ≤ 85°C	0.5		2.0	uA
MODE CONTROL INTERFACE (MODE)					
Mode LO Threshold	Device in negative slope mode of operation	0.75			V
Mode HI Threshold	Device in positive slope mode of operation			1.5	V
ENABLE INTERFACE (ENBL)					
Enable Threshold			2		V
Enable Response Time	Time delay following HI to LO transition until device meets full specifications.		TBD		µs
Enable Input Bias Current	ENBL = 5 V		20		µA
	ENBL = 0 V		20		nA

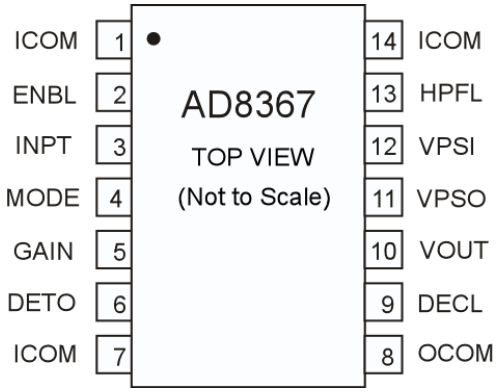
Notes
1) See applications section for reactive matching networks

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage VPSO, VPSI ……..…..……5.5V
ENBL Voltage ……..……VPS + .x V
MODE Select Voltage ……VPS + .x V
V_{GAIN} Control Voltage ……..……VPS + .x V
Input Power at Maximum Gain……..……..+8 dBm
Equivalent Voltage ……1.6 V
Internal Power Dissipation ….……..TBD
θ_{JA} ……..……150°C/W
Maximum Junction Temperature ……..…+125° C
Operating Temperature Range ……-40° C to +85° C
Storage Temperature Range …….-65° C to +150° C
Lead Temperature Range (Soldering 60 sec)..+300° C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



Pin Function Descriptions

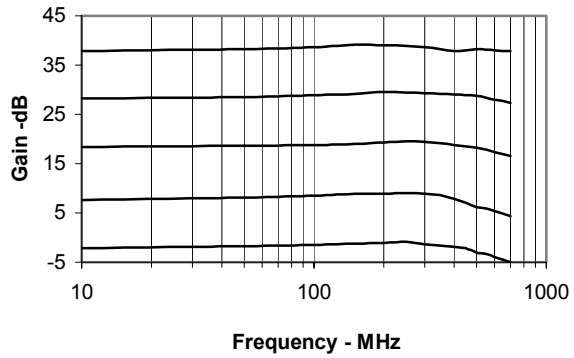
Pin	Name	Function
1,7,14	ICOM	Device Common. Connect to low impedance ground.
2	ENBL	Apply a positive voltage (≤VPS) to activate device.
3	INPT	Device Input.
4	MODE	Slope Control. Pull HI for Positive VGA Slope. Pull LO for Negative VGA Slope.
5	GAIN	Gain Control Voltage Input.
6	DETO	Detector Output. Provides output voltage for RSSI function and AGC control.
8	OCOM	Device Common. Connect to low impedance ground.
9	DECL	De-coupling Pin. Used as an external connection for mid-supply de-coupling capacitor.
10	VOUT	Single–Ended Output. Must be AC coupled.
11	VPSO	Positive Supply Voltage. +2.7 V to +5.5 V. VPSI and VPSO are tied together internally with back to back PN junctions. They should be tied together externally and properly bypassed.
12	VPSI	Positive Supply Voltage. +2.7 V to +5.5 V. VPSI and VPSO are tied together internally with back to back PN junctions. They should be tied together externally and properly bypassed.
13	HPFL	High Pass Filter Connection. Used to set the high pass corner frequency.

ORDERING GUIDE

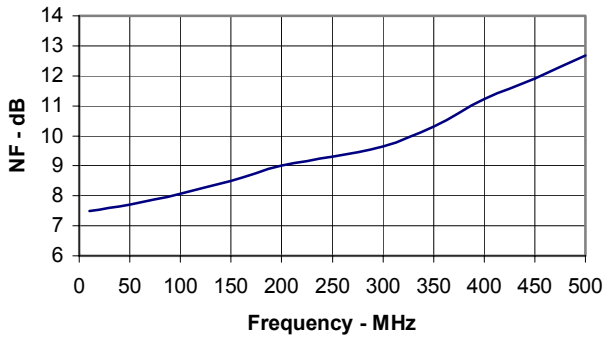
Model	Temp. Range	Package Description	Package Option
AD8367ARU	-40 °C to +85 °C	Tube, 14-Lead TSSOP	
AD8367ARU-REEL		13" Tape and Reel	
AD8367ARU-REEL7		7" Tape and Reel	
AD8367-EVAL		Evaluation Board	

CAUTION

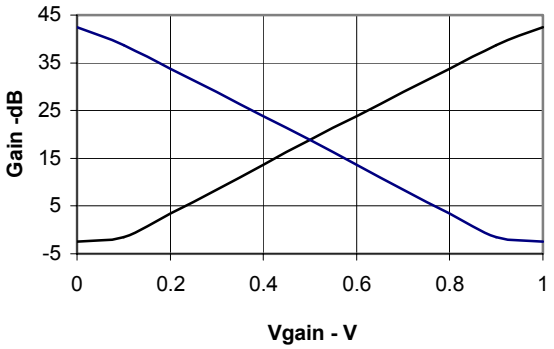
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8367 feetures proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy [>250 V HBM] electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality



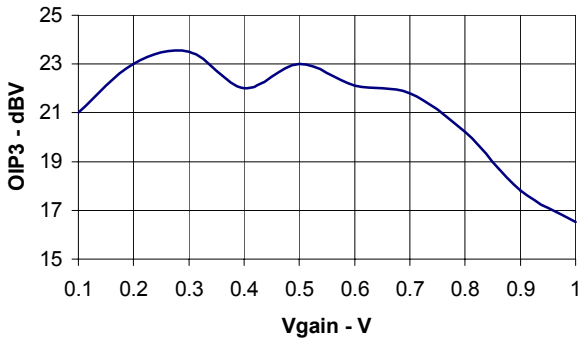
TPC 1. Gain versus Frequency for Values of V_{GAIN}



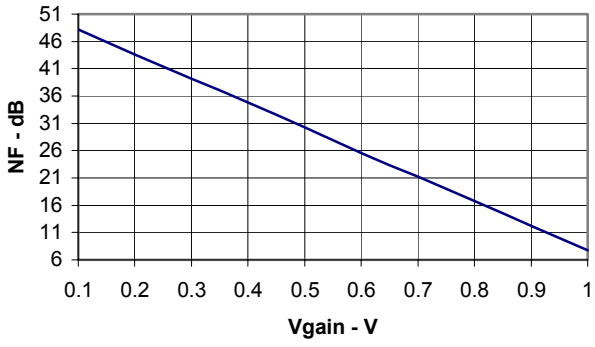
TPC 4. NF versus Frequency (Using Broadband Matching Network)



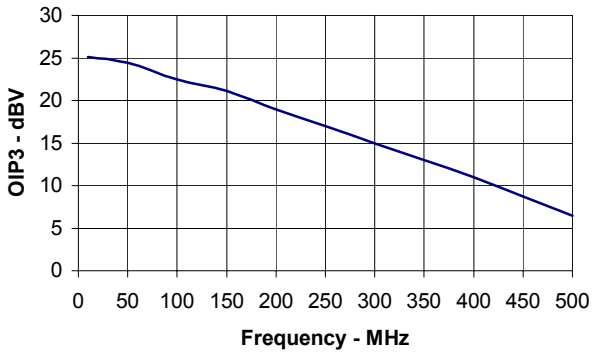
TPC 2. Gain versus Vgain (Mode LOW and Mode HI)



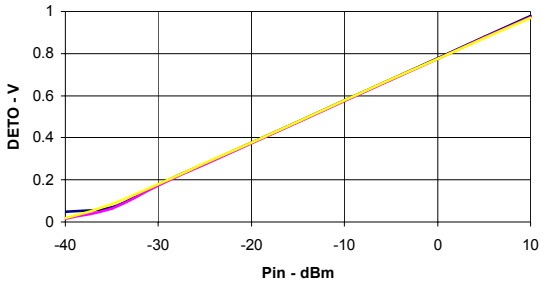
TPC 5. OIP3 versus Vgain (Ref 200Ω)



TPC 3. NF versus Vgain (Using Broadband Matching Network)



TPC 6. OIP3 versus Frequency (Ref 200Ω, Using Broadband Matching Network)



TPC 7. DETO versus Input Power@ 10,70,140 and 380MHz

BASIC CONNECTIONS

The AD8367 is a variable gain single-ended IF amplifier with accurate 45dB of gain control and a 3dB bandwidth of 500MHz. It can be configured as a traditional VGA whose gain is controlled externally through the GAIN pin or as an AGC amplifier where the output is forced to a specific level by virtue of a built-in RMS detector.

The AD8367 is typically used as an IF VGA in the receive and transmit portions of the signal chain. Figure 1 shows the basic connections for operating the AD8367 and Figure 2 shows a block diagram of a typical application.

A supply voltage of +2.7 V to +5.5 V is required for the AD8367. The supply to the VPSO and VPSI pins should be decoupled with a low inductance 0.1µF surface mount ceramic capacitors, close to the device. Additional supply decoupling may be attained using a small series resistance and a capacitor should be used to ensure clean supply voltage to the AD8367.

The input to the AD8367 is ground referenced at an impedance of 200Ω. A broadband 50Ω input match can be achieved by connecting a 66.5 Ω resistor between INPT and ground. This resistance combines with the internal input impedance to give an overall broadband input resistance of approximately 50Ω.

The AD8367 is designed to drive a 200Ω load. The output of the AD8367 has an internal source impedance of 50Ω. The output voltage swing will be reduced to 2Vp-p when using the configuration in figure 1 with a 50Ω load. By using reactive matching techniques the maximum power can be delivered to the load over a narrow bandwidth (see applications section for Reactive Matching).

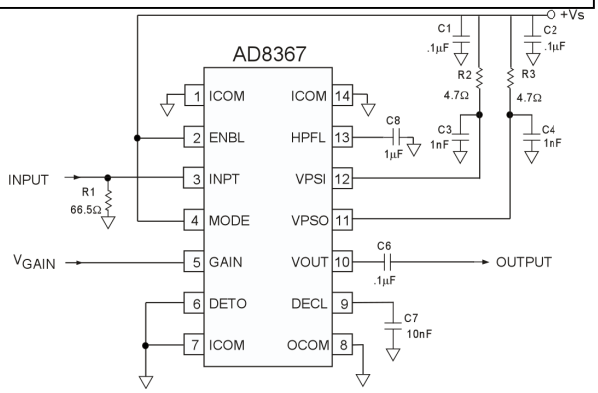


Figure 1. Basic Connections for VGA Mode

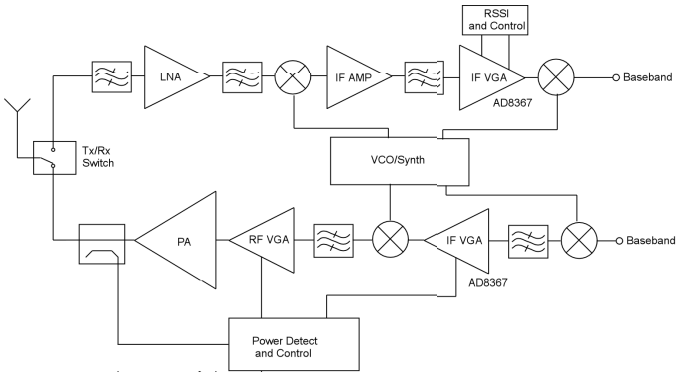


Figure 2. Typical Application

In typical applications the AD8367 will be employed as an IF VGA where the gain control voltage, V_{GAIN}, is generated elsewhere in the signal chain. Usually, the gain control voltage is derived from some measurement system. The Gain of the device can be defined as:

$$Gain = V_{GAIN} \times 45dB / V - 2.5dB$$

where

V_{GAIN} is the control voltage applied to the GAIN input pin.

The block diagram in figure 2 shows the transmit and receive sections of a half duplex super-heterodyne architecture. In this example, a directional coupler is used to feed a portion of the transmitted RF signal to a power measurement device. The measurement device drives the gain control voltage to the VGA to maintain a constant radiated RF output.
The AD8367 is used as an IF AGC in the receiver

to maintain a desired signal level prior to the final downconversion to baseband. In this application the DETO pin is used for RSSI, and to drive the gain control voltage to yield a closed loop AGC. Figure 3 shows the basic connections for operating the AD8367 as an IF AGC.

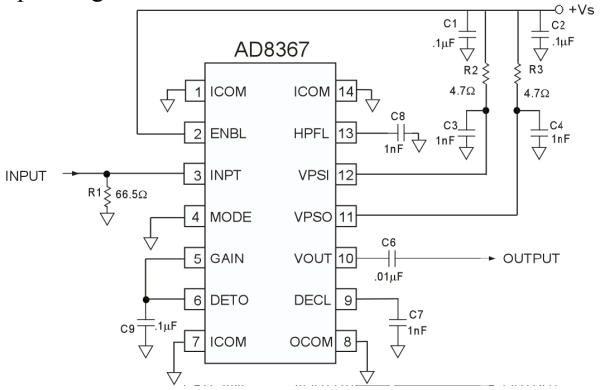


Figure 3. Basic Connections for AGC Mode

Slope Control

The slope of the gain transfer function can be inverted using the MODE pin. By simply connecting the MODE pin to ground the gain will decrease with increasing gain control voltage. This is the recommended mode of operation for AGC applications.

AGC Operation

A closed loop AGC can be implemented by connecting the DETO to the GAIN pin. As the DETO output voltage increases with input signal strength the gain is reduced. The resultant output will be driven to a 500mVrms level for a 200Ω load.

When operating the AD8367 in AGC mode, the DETO voltage can be used as a received signal strength indicator, RSSI. The RSSI voltage at the DETO pin is a function of the input power and can be expressed numerically as:

$$V_{DETO} = P_{IN}(dBm) \times C_{GAIN} + INTC$$

where

V_{DETO} is the voltage at the DETO output

P_{IN} is the input power to the device in units of dBm

C_{GAIN} is the conversion gain of the onboard detector. C_{GAIN} is typically 20mV/dBm.

INTC is the detector intercept. INTC is typically 0.78V.

Capacitive Loading

Capacitive loads on the output of the AD8367 exceeding ~15pF may result in noise floor shaping and possibly even oscillations. Special care should be taken to minimize capacitive loading on the output of the device. It may be necessary to add a small series resistor on the output trace of the device when attempting to drive capacitive loads.

Reactive Matching

In many applications, the AD8367 will most likely be matched using reactive matching components as shown in figure 4. The AD8367 is designed to operate in a 200Ω system, this may require transforming the source or load impedance through the use of a step up or step down network. Table I outlines common matching networks for using the AD8367 in a 50Ω system.

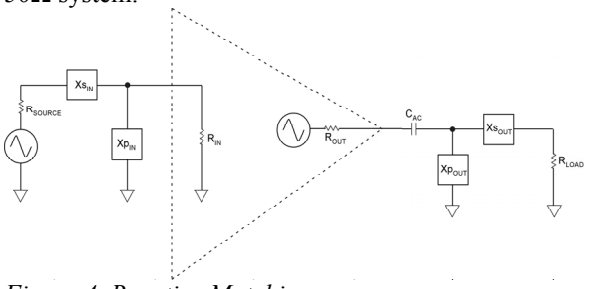


Figure 4. Reactive Matching

Table I. Reactive Matching Components for a 50Ω System, R_S=50Ω, R_{LOAD}=50Ω.

Frequency	Xs_{IN}	Xp_{IN}	Xs_{OUT}	Xp_{OUT}
10MHz	0Ω	66.5Ω	0Ω	open
70MHz	200nH	20pF	200nH	20pF
140MHz	100nH	10pF	100nH	10pF
380MHz	39nH	4pF	39nH	4pF

Evaluation Board

Figure 5 shows the schematic of the AD8367 evaluation board. The board is powered by a single supply in the range, +2.7 to +5.5V. Table II details the various configuration options of the evaluation board.

Figure 5. Evaluation Board Schematic

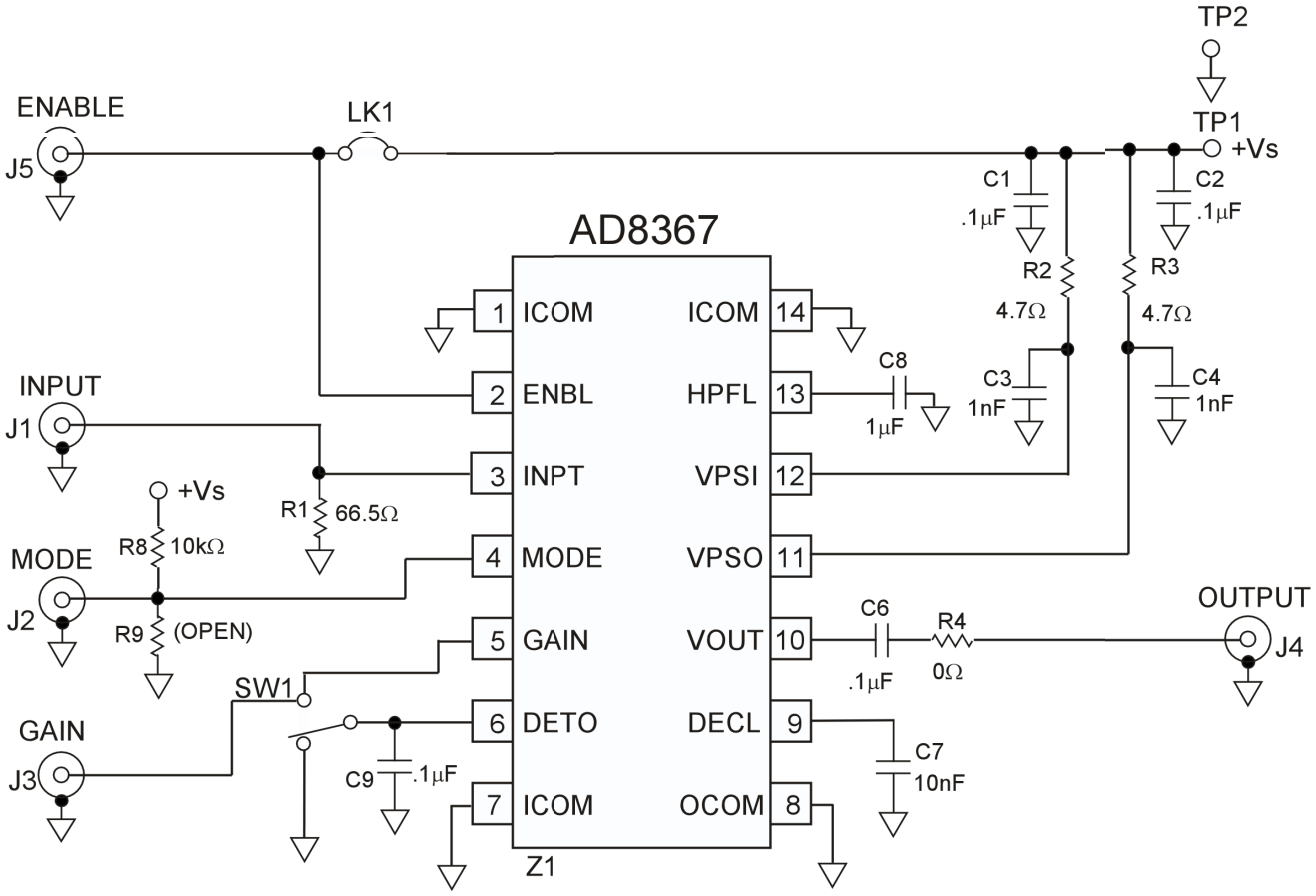


Table II Evaluation Board Configuration Options

Component	Function	Default Condition
TP1, TP2	**Supply and Ground Vector Pins**	Not Applicable
LK1	Device Enable: When LK1 is installed, the ENBL pin is connected to the positive supply and the AD8367 is in operating mode. LK1 should be removed when using a remote device to enable the AD8367 through J5.	LK1 = Installed
R1	**Input Interface:** The 66.5 Ω resistor in position R1 combines with the AD8367's internal input impedance to give a broadband input impedance of around 50 Ω.	R1= 66.5 Ω (Size 0603)
R4, C6	**Output Interface:** The AC coupling capacitor, C6, can be increased to obtain a lower high pass corner frequency.	R4 = 0Ω (Size 0603) C6 = .1uF (Size 0603)
C1, C2, C3, C4, R2, R3	**Power Supply Decoupling:** The nominal supply decoupling consists of a 0.1uF capacitor to ground, a 4.7Ω series resistor, and a 1nF capacitor to ground. The same de-coupling network should be used on both VPSI and VPSO supply lines.	C1 = C2 = 0.1uF (Size 0603) R2 = R3 = 4.7Ω (Size 0805) C3= C4 = 1nF (Size 0603)
C7	**Internal Supply Decoupling:** Capacitor C7 provides mid-supply decoupling.	C7 = 1nF (Size 0603)
C8	**Filter Capacitor:** HPFL capacitor, sets the high pass corner frequency.	C8 = 1uF (Size 0805)
R8, R9	**Gain Mode:** Allows for pin strapping of the desired gain mode. The evaluation board uses a 10kΩ pull-up resistor to set the default mode of operation to a positive VGA slope.	R8 =10kΩ (Size 0805) R9 = open (Size 0805)
SW1	**VGA/AGC Select:** Used to select VGA or AGC mode of operation.	SW1 = ON