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50–1000 MHz Quadrature Demodulator

Advanced Datasheet **AD8348**

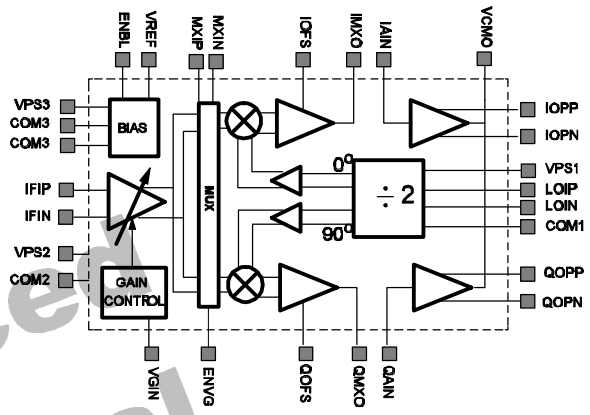
Features

Integrated I/Q demodulator with IF VGA Amplifier
Operating Frequency 50–1000Mhz
Demodulation Bandwidth 40MHz
Linear-in-dB AGC Range 45dB
Third Order Intercept
IIP3 +25 dBm @ min gain
IIP3 -11 dBm @ max gain
Quadrature Demodulation Accuracy
Phase Accuracy 0.6° RMS
Amplitude Balance 0.3 dB
Noise Figure 10dB @ max gain
LO Input -10 dBm
Single Supply 2.7-5.5V
Power down mode
Compact 28-pin TSSOP package

Applications

QAM/QPSK Demodulator
W-CDMA/CDMA/GSM/NADC
Wireless Local Loop
LMDS/MMDS

Functional Block Diagram



General Description

The AD8348 is a broadband quadrature demodulator with an integrated IF VGA & baseband amplifiers. It is suitable for use in communications receivers, performing quadrature demodulation from the intermediate frequency (IF) directly to baseband frequencies. The baseband amplifiers have been designed to directly interface with a dual channel A-to-D converter such as the AD9201 & AD9283 for digitizing and post-processing.

The IF input signal goes through an X-AMP variable-gain amplifier into two Gilbert-cell mixers. The IF variable gain amplifier provides 45dB of gain control. A precision gain-control circuit sets a linear-in-dB gain characteristic for the VGA and provides temperature compensation. The LO quadrature phase splitter employs a divide-by-two frequency divider to achieve high quadrature accuracy and amplitude balance over the entire operating frequency range. I & Q-channel baseband amplifiers follow the baseband outputs of the mixers. Connecting a bypass capacitor at each offset input (IOFS & QOFS) nulls DC offsets. Offset control can also be overridden by applying an external voltage at the offset inputs.

The IF variable-gain amplifier can be optionally disabled and the IF signal can be applied directly to the quadrature mixer inputs via pins MXIP and MXIN. The mixers' outputs are brought off-chip for filtering before final amplification. Inserting a channel selection filter before each baseband amplifier increases the demodulator's signal handling range by reducing the amplitude of high-level, out-of-channel interferers before further amplification. The signals from the external filters are further amplified to drive A-to-D converters differentially. The DC common-mode level at the baseband outputs is set by the voltage applied to the VCMO pin, which can be tied to the internal VREF voltage or provided externally. This flexibility allows the user to maximize the input dynamic range to the A-to-D converter.

REV. B
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AD8348-SPECIFICATIONS (V_S = 5V; T_A=25 °C; F_{LO}=900MHz; F_{IF}=900MHz; Plo=-10dBm, Rs(LO)= 50 Ω, Rs(IF)=200Ω, unless otherwise noted)

Parameter	Condition	Min	Typ	Max	Units
GENERAL					
LO Frequency Range	External input must be 2x LO frequency	50		1000	MHz
IF Frequency Range		50		1000	MHz
Baseband bandwidth		0		20	MHz
LO Input Level	50 ohm source	-10		-6	dBm
VGIN Input Level		0.2		1.2	V
IF FRONT-END WITH VGA	IFIP/IFIN to IMXO/VREF, QMXO/ VREF ENVG=5V				
Zin		150Ω ||1pF	190Ω ||1pF	230Ω ||1pF	Ω ||pF
Variable Gain Range		42.3	44	45	dB
Linear-in-dB error			-0.7/+0.9		dB
Maximum Conversion Gain	VGIN=0.2V (max gain)	25.3	25.6	26.3	dB
Minimum Conversion Gain	VGIN=1.2V (min gain)	-19.6	-18.3	-16.4	dB
IF Gain Flatness	FIF=50MHz-1GHz		3.5		dB p-p
2nd Order Input Intercept(IIP2)	IF1=905MHz, IF2=906MHz -22 dBm each tone from 200 ohm source VGIN=1.2V (min gain)		40		dBm
3rd Order Input Intercept(IIP3)	IF1=900MHz, IF2=950MHz -22 dBm each tone from 200 ohm source VGIN=1.2V (min gain)	26.8	26.6	31.8	dBm
2nd Order Input Intercept(IIP2)	IF1=905MHz, IF2=906MHz -42 dBm each tone from 200 ohm source VGIN=0V (max gain)		30		dBm
3rd Order Input Intercept(IIP3)	IF1=55MHz, IF2=56MHz -42 dBm each tone from 200 source VGIN=0V (max gain) (see figure 2)	-13	-11	-7.6	dBm
1dB Input compression point	VGIN=0V (max gain)				dBm
Noise Figure	VGIN=0V (max gain) From 200 ohm source	9.5	10.0	11.4	dB
Input LO Leakage	Measured at IFIP,IFIN		-125		dBm
Output LO Leakage	Measured at IMXO/QMXO (LO=50MHz)		10		mVp-p
Demodulation Bandwidth	Full-power bandwidth (IIP3 drops 3dB)		20		MHz
	Small-signal 3dB bandwidth	40	40	100	MHz
Quadrature Phase Error	LO=1GHz (LOIP/LOIN 2GHz, single- ended) (see figure 1)		0.55	0.74	deg RMS
I/Q Amplitude Imbalance			0.3?		dB
Peak output current			2.5		mA
IF FRONT-END WITHOUT VGA	from MXIP,MXIN to IMXO/QMXO ENVG=0V				
Zin	Measured differentially across MXIP/ MXIN	150Ω ||0.5pF	200Ω || 0.5pF	240Ω ||0.5pF	Ω ||Pf
Conversion Gain		11.7	12.2	12.3	DB
IF Gain Flatness	FIF=50MHz-1GHz		1?		dB p-p

Parameter	Condition	Min	Typ	Max	Units
2nd Order Input Intercept(IIP2)	IF1=905MHz, IF2=906MHz -32 dBm each tone from 200 ohm source	40	48.6	51.9	dBm
3rd Order Input Intercept(IIP3)	IF1=905MHz, IF2=906MHz -32 dBm each tone from 200 ohm source (See figure 2)	8.9	10.8	13.7	dBm
1dB Input compression point	VGIN=0V (max gain)				dBm
Noise Figure	VGIN=0V (max gain) From 200 ohm source	14.6	16.3	16.5	dB
Input LO Leakage	Measured at MXIP/MXIN		-120		dBm
Output LO Leakage	Measured at IMXO/QMXO		10		mVp-p
Demodulation Bandwidth	Full-power bandwidth (IIP3 drops 3dB)		20		MHz
	Small-signal 3dB bandwidth, 10pF load	40	40	100	MHz
Quadrature Phase Error	LO=1GHz (LOIP/LOIN 2GHz, single- ended input) (See figure 1)		0.62	0.84	deg RMS
I/Q Amplitude Imbalance			0.3?		dB
Capacitive load	shunt from IMXO,QMXO to VCMO	0		10	pF
Resistive load	shunt from IMXO,QMXO to VCMO	2k			Ω
Peak output current			2.5		mA
BASEBAND AMPLIFIER	from IAIN to IOPP/IOPN & QAIN to QOPP/QOPN				
Gain		18.9	19.1	19.5	dB
Input referred Noise Voltage		6.5	8	9.5	nV/rtHz
Bandwidth	10pF differential load	38	38	61	MHz
Output DC differential offset	Corrected using 500pF capacitor on IOFS,QOFS		10	15	mV
Output Common-mode offset			10		mV
Group Delay Flatness	0.1-30MHz	0.1	0.3	0.3	ns pp
3rd Order Intermod. Distortion	Fin1=5MHz Fin2=6MHz Vin1=Vin2=50mVp-p	-94.8	-83	-78	dBc
Capacitive load	Differential across IOPP/IOPN, QOPP/QOPN	0	10	10	pF
Resistive load	Differential across IOPP/IOPN, QOPP/QOPN	2k			ohm
Peak output current			1		mA
REFERENCE VOLTAGE					
V_{REF}			1		V
POWER SUPPLIES					
Voltage		2.7		5.5	V
Current Active	ENBL=5V		43	62	mA
Current Standby	ENBL=0		20		uA

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage VPS1, VPS2, VPS3……..…….5.5V
LO & RF Input Power ……..……..…TBD dBm
Internal Power Dissipation ….…..……..…..…..TBD
θ_{JA} ……TBD C/W
Maximum Junction Temperature ……..…+TBD° C
Operating Temperature Range ….-40° C to +85° C
Storage Temperature Range …...-65° C to +150° C
Lead Temperature (Soldering 60 sec)..….+TBD° C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

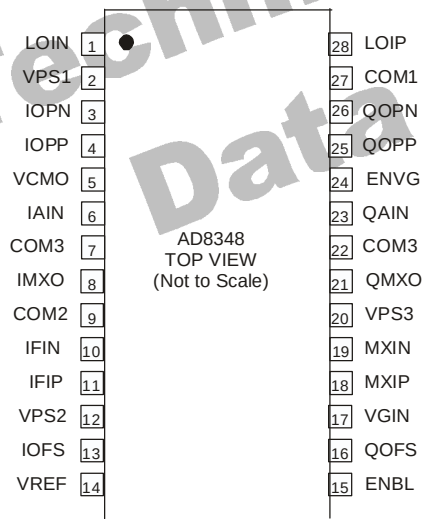
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8366 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy [>250 V HBM] electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temp. Range	Package Description	Package Option
AD8348XXX	-34 °C to +85 °C	28-Lead TSSOP Thin Shrink Small Outline Package	RU-28

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin	Name	Description	Equiv. Cir.
1,28	LOIN,LOIP	LO Input. For optimum performance, these inputs should be driven differentially. Typical input drive level is equal to –10 dBm. To obtain a broadband 50 Ω input impedance, connect a 60 Ω shunt resistor between LOIP and LOIN.	
2	VPS1	Positive Supply for LO section. This pin should be decoupled with 0.1 uF and 100 pF capacitors.	
3,4	IOPN,IOPP	I-channel differential baseband output. Typical output swing is equal to 1Vpp differential. The common mode level on these pins is programmed by the voltage on VCMO	
5	VCMO	Baseband Amplifier Common-mode Voltage. The voltage applied to this pin sets the output common mode level of the baseband amplifiers and mixer outputs. This pin can either be connected to VREF or to a reference voltage from another device (typically an ADC)	
6	IAIN	I-ch Baseband Amplifier Input. This pin should have a bias level of approximately 1 V. If IAIN is DC coupled to IMXO, biasing will be provided by IMXO. If an ac-coupled filter is placed between IMXO and IAIN, this pin can be biased from VREF through a 1 kΩ resistor. The gain from IAIN to the differential outputs IOPN/IOPP is 20 dB.	
7,22	COM3	Ground for Biasing and Baseband sections	
8	IMXO	I-ch Baseband Output. This is a low impedance output whose bias level is equal to 1V. This pin is typically connected to IAIN, either directly or through a filter.	
9	COM2	IF Section Ground	
10,11	IFIN,IFIP	IF Input. RFIN should be ac-coupled to ground. The single-ended IF input signal should be ac-coupled into RFIP. For a broadband 50 Ω input impedance, connect a 65 Ω resistor from the signal side of RFIP's coupling capacitor, to ground.	
12	VPS2	Positive Supply for IF Section. This pin should be decoupled with 0.1 uF and 100 pF capacitors.	
13	IOFS	I-ch Offset Nulling Input. To null the dc-offset on the I-channel VGA output (IMXO), connect a 0.1 uF capacitor from this pin to ground. Optionally this can be driven with a fixed voltage (typically a DAC calibrated such that the offset at IOPP/IOPN is nulled) to extended operating frequency range down to DC.	
14	VREF	Reference Voltage Output. This output voltage (1V) is the main bias level for the device and can be used to externally bias the inputs and outputs of the baseband amplifiers.	
15	ENBL	Chip Enable Input. Active high. Threshold is equal to +Vs/2.	
16	QOFS	Q-ch Offset Nulling Input. To null the dc-offset on the Q-channel VGA output (QMXO), connect a 0.1 uF capacitor from this pin to ground. Optionally this can be driven with a fixed voltage (typically a DAC calibrated such that the offset at IOPP/IOPN is nulled) to extended operating frequency range down to DC.	
17	VGIN	Gain Control Input. The voltage on this pin controls the gain on the RF and baseband VGAs. The gain control is applied in parallel to all VGAs. The gain control voltage range is from 0.2 V to 1.2 V and corresponds to a conversion gain range from +25 dB to –18 dB. This is the gain to the output of the mixers (i.e. QMXO and IMXO). There is an additional 20 dB of gain in the baseband amplifiers. Note that the gain control function has a negative sense (i.e. increasing voltage decreases gain).	
18,19	MXIP, MXIN	Auxiliary mixer inputs. If ENVG is low then the IFIP, IFIN inputs are disabled and MXIP, MXIN is enabled, allowing the VGA to be bypassed. This is a fully differential input which should be AC coupled to the signal source. If a broadband 50 ohm match is desired, a 65 ohm resistor should be placed across MXIP, MXIN.	
20	VPS3	Positive Supply for Biasing and Baseband sections. This pin should be decoupled with 0.1 uF and 100 pF capacitors.	
21	QMXO	Q-ch Baseband VGA Output. This is a low impedance output whose bias level is equal to 1V. This pin is typically connected to QAIN, either directly or through a filter.	
22	COM3	Ground for baseband and biasing sections	
23	QAIN	Q-ch Baseband Amplifier Input. This pin should have a bias level of approximately 1 V. If QAIN is connected directly to QMXO, biasing will be provided by QMXO. If an ac-coupled filter is placed between QMXO and QAIN, this pin can be biased from VREF through a 1 kΩ resistor. The gain from QAIN to the differential outputs QOPN/QOPP is 20 dB.	
24	ENVG	VGA enable. Active high. If high, IFIP, IFIN inputs are enabled and MXIP, MXIN inputs are disabled.	
25,26	QOPP,QOPN	Q-channel differential baseband output. Typical output swing is equal to 1Vpp differential. The common mode level on these pins is programmed by the voltage on VCMO	
27	COM1	LO Section Ground	

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead TSSOP
(RU-28)