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0.8 GHz - 2.7 GHz Direct Conversion Quadrature Demodulator

Preliminary Technical Data AD8347

FEATURES

Integrated RF and Baseband AGC amplifiers
Base band Level Control circuit
Quadrature Phase Accuracy 3 deg
I/Q Amplitude Balance 0.3dB
Third Order Intercept (IIP3) +12dB (min. gain)
Noise Figure 11dB @ max. gain
Linear-in-dB AGC Range 65dB
Low LO Drive –10dBm
ADC Compatible I/Q outputs
Single Supply 2.7-5.5V
Power down mode
Package 28-pin TSSOP

Applications

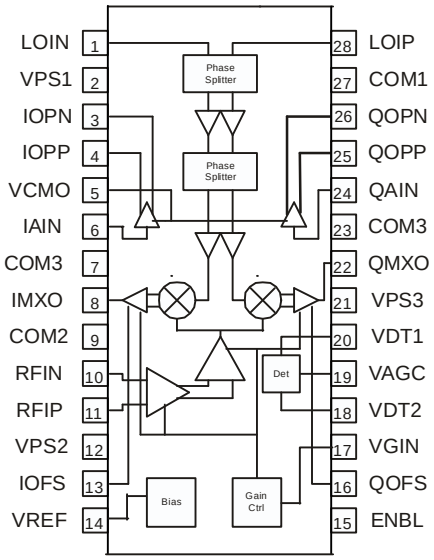
Cellular Basestations
Radio Links
Wireless Local Loop
IF Broadband Demodulator
RF Instrumentation
Satellite Modems

General Description

The AD8347 is a broadband Direct Quadrature Demodulator with RF & Baseband Automatic Gain Control (AGC) Amplifier. It is suitable for use in many communications receivers, performing Quadrature demodulation directly to baseband frequencies. The input operating frequency is up to 2.7GHz. The outputs can be connected directly to popular A-to-D converters such as the AD9201 & AD9283.

The RF input signal goes through two stages of variable gain amplifiers prior to two Gilbert-cell Mixers. The LO quadrature phase splitter employs polyphase filters to achieve high quadrature accuracy and amplitude balance over the entire operating frequency range. Separate I & Q channel, variable-gain preamplifiers follow the baseband outputs of the mixers. The RF & baseband amplifiers together provide 65dB of gain control.

Functional Block Diagram



Baseband level detectors are included for use in an AGC loop to maintain the output level. The demodulator DC offsets are minimized by connecting a bypass capacitors to each offset null pin (IOFS & QOFS).

The offset control can also be overridden by applying an external voltage at the offset inputs. The precision control circuit sets the Linear-in-dB RF gain response to the gain control voltage and provides temperature compensation.

The baseband preamplifier outputs are brought off-chip for filtering before final amplification. Inserting a channel selection filter before the output amplifier to eliminate high-level out-of-channel interferers. Additional internal circuitry allows the user to set the DC common-mode level at the baseband outputs.

U.S. Patents Issued and Pending

REV. PrK 5/15/01

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AD8347

AD8347-SPECIFICATIONS

(Vs=+5V; T_A=25°C; F_{LO}=1.9GHz; F_{RF}=1.905GHz; Plo=-8dBm, Rload=10KΩ, dBm with respect to 50 ohm, unless otherwise noted)

Parameter	Condition	Min	Typ	Max	Units
Operating Conditions					
LO/RF Freq. Range		0.8		2.7	GHz
LO Input Level		-10		0	dBm
VGIN Input Level		0.2		1.2	V
V_{SUPPLY} (V_S)		2.7		5.5	V
Temperature Range		-40		85	°C
RF Amplifier/Demodulator	from RFIP/RFIN to IMXO & QMXO				
AGC Gain Range			65		dB
Conversion Gain (max.)	Vgin=0.2V (max. gain)		40		dB
Conversion Gain (min.)	Vgin=1.2V (min. gain)		-25		dB
Gain Accuracy	F_{RF}=1.9GHz		+/-2		dB
Gain Flatness	F_{LO}=0.8-2.7GHz, F_{BB}=1MHz		0.6		dB p-p
3rd Order Input Intercept(IIP3)	F_{RF1}=1.905GHz, F_{RF2}=1.906GHz, -10dBm each tone, (min. gain)		+10		dBm
2nd Order Input Intercept(IIP2)	RF1=1.905GHz, RF2=1.906GHz, -10dBm each tone, (min. gain)		+31		dBm
LO Leakage (RF)	at RFIP		-50		dBm
LO Leakage (MXO)	at IMXO/QMXO		-60		dBm
Demodulation Bandwidth	-3dB		65		MHz
Quadrature Phase Error	F_{RF1}=1.9GHz		3		deg.
I/Q Amplitude Imbalance	F_{RF1}=1.9GHz		0.3		dB
Noise Figure	max. gain		11		dB
Mixer Output Level	RF=-70dBm, max. gain		15		mVpp
Baseband DC Offset	at IMXO/QMXO, max. gain (corrected, ref to VREF)		2.5		mV
Baseband Output Amplifier	from IAIN to IOPP/IOPN & QAIN to QOPP/QOPN				
Gain			30		dB
Bandwidth	-3dB		50		MHz
Output DC Offset (diff. out)	|(V(IOPP,IOPN)|		80		mV
Common-mode offset	|(V(IOPP)+V(IOPN))/2-V(VCMO)| etc		See notes		mV
Group Delay Flatness	0-50MHz		1.5		ns pp
3rd Order Intermod. Distortion	Fin1=5MHz Fin2=6MHz Vin1=Vin2=8mVpp		-70		dBc
Input bias current			5		uA
Output Swing Limit (upper)		Vs-1.3			V
Output Swing Limit (lower)				0.4	V

Parameter	Condition	Min	Typ	Max	Units
Control Input/Output					
Gain Control Input bias current	VGIN		30		nA
Offset Input overriding current	IOFS, QOFS		10		uA
VREF Output	Rload=10K ohm		1		V
Detector					
DC Input threshold[1]	|V(VDET)-V(VREF)| VDT2 connected to VDET		5		mV
LO/RF Input					
LOIP Input VSWR	w/ext. res.; LOIN w/100pF to GND		1.4:1		
RFIP Input VSWR	w/ext. res.; RFIN w/100pF to GND		1.4:1		
Power Supplies	VPS1,VPS2,VPS3				
Power-up Control	Low=Standby	0		0.5	V
Power-up Control	High=Enabled	2.0		+Vs	V
Current (Enabled)	@ 2.7V		55		mA
Current (Standby)	@2.7V		30		uA

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage VPS1, VPS2, VPS3…...…….5.5V
LO & RF Input Power ……..…..……..TBD dBm
Internal Power Dissipation ……..…..……..TBD
θ_{JA} ……...……TBD C/W
Maximum Junction Temperature ……..…+TBD° C
Operating Temperature Range …...-40° C to +85° C
Storage Temperature Range …….-65° C to +150° C
Lead Temperature (Soldering 60 sec)...…..+TBD° C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8366 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy [>250 V HBM] electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temp. Range	Package Description	Package Option
AD8347ARU	-34 °C to +85 °C	28-Lead TSSOP Thin Shrink Small Outline Package	RU-28
AD8347-EVAL		Evaluation Board	

PIN CONFIGURATION

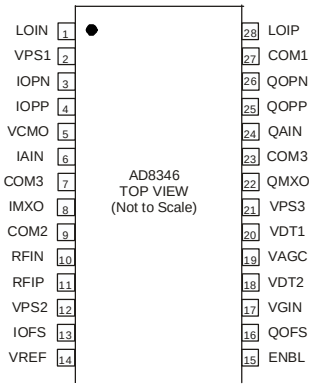

Table I PIN FUNCTION DESCRIPTIONS

Pin	Name	Description	Equiv. Cir.
1,28	LOIN,LOIP	LO Input. For optimum performance, these inputs should be driven differentially. Typical input drive level is equal to –8 dBm. To obtain a broadband 50 Ω input impedance, connect a 200 Ω shunt resistor between LOIP and LOIN.	
2	VPS1	Positive Supply for LO section. This pin should be decoupled with 0.1 uF and 100 pF capacitors.	
3,4	IOPN,IOPP	I-channel differential baseband output. Typical output swing is equal to 1Vpp differential. The common mode level on these pins is programmed by the voltage on VCMO	
5	VCMO	Baseband Amplifier Common-mode Voltage. The voltage applied to this pin sets the output common mode level of the baseband amplifiers. This pin can either be connected to VREF (pin 14) or to a reference voltage from another device (typically an ADC)	
6	IAIN	I-ch Baseband Amplifier Input. This pin should have a bias level of approximately 1 V. If IAIN is connected directly to IMXO, biasing will be provided by IMXO. If an ac-coupled filter is placed between IMXO and IAIN, this pin can be biased from VREF through a 1 kΩ resistor. The gain from IAIN to the differential outputs IOPN/IOPP is 30 dB.	
7,23	COM3	Ground for Biasing and Baseband sections	
8	IMXO	I-ch Baseband VGA Output. This is a low impedance output whose bias level is equal to 1V. This pin is typically connected to IAIN, either directly or through a filter.	
9	COM2	RF Section Ground	
10,11	RFIN,RFIP	RF Input. RFIN should be ac-coupled to ground. The RF input signal should be ac-coupled into RFIP. For a broadband 50 Ω input impedance, connect a 200 Ω resistor from the signal side of RFIP's coupling capacitor, to ground.	
12	VPS2	Positive Supply for RF Section. This pin should be decoupled with 0.1 uF and 100 pF capacitors.	
13	IOFS	I-ch Offset Nulling Input. To null the dc-offset on the I-channel VGA output (IMXO), connect a 0.1 uF capacitor from this pin to ground.	
14	VREF	Reference Voltage Output. This output voltage (1V) is the main bias level for the device and can be used to externally bias the inputs and outputs of the baseband amplifiers.	
15	ENBL	Chip Enable Input. Active high. Threshold is equal to +Vs/2.	
16	QOFS	Q-ch Offset Nulling Input. To null the dc-offset on the Q-channel VGA output (QMXO), connect a 0.1 uF capacitor from this pin to ground.	
17	VGIN	Gain Control Input. The voltage on this pin controls the gain on the RF and baseband VGAs. The gain control is applied in parallel to all VGAs. The gain control voltage range is from 0.2 V to 1.2 V and corresponds to a gain range from +40 dB to –25 dB. This is the gain to the output of the baseband VGAs (i.e. QMXO and IMXO). There is an additional 30 dB of gain in the baseband amplifiers. Note that the gain control function has a negative sense (i.e. increasing voltage decreases gain). In AGC mode, this pin is connected directly to VAGC.	
18	VDT2	Detector Input. This pin is one of the inputs to the on-board detector. This pin, which has a high input impedance, is normally connected to IMXO.	
19	VAGC	AGC Output. This pin provides the output voltage from the on-board detector. In AGC mode, this pin is connected directly to VGIN.	
20	VDT1	Detector Input. This pin is one of the inputs to the on-board detector. This pin, which has a high input impedance, is normally connected to QMXO.	
21	VPS3	Positive Supply for Biasing and Baseband sections. This pin should be decoupled with 0.1 uF and 100 pF capacitors.	
22	QMXO	Q-ch Baseband VGA Output. This is a low impedance output whose bias level is equal to 1V. This pin is typically connected to QAIN, either directly or through a filter.	
24	QAIN	Q-ch Baseband Amplifier Input. This pin should have a bias level of approximately 1 V. If QAIN is connected directly to QMXO, biasing will be provided by QMXO. If an ac-coupled filter is placed between QMXO and QAIN, this pin can be biased from VREF through a 1 kΩ resistor. The gain from QAIN to the differential outputs QOPN/QOPP is 30 dB.	
25,26	QOPP,QOPN	Q-channel differential baseband output. Typical output swing is equal to 1Vpp differential. The common mode level on these pins is programmed by the voltage on VCMO	
27	COM1	LO Section Ground	

CIRCUIT DESCRIPTION

OVERVIEW

The AD8347 is a direct I/Q demodulator usable in digital wireless communication systems including Cellular, PCS and Digital Video receivers. RF signal in the frequency range of 800-2500 MHz is directly downconverted to the I & Q components at baseband using an Local Oscillator (LO) signals at the same frequency as the RF signal.

The RF input signal goes through two stages of variable gain amplifiers before splitting up to reach two Gilbert-cell Mixers. The mixers are driven by two pairs of Local Oscillator (LO) signals which are in quadrature (90 deg. of phase difference) with each other. The output of the mixers are applied to baseband I & Q channel variable-gain preamplifiers. The outputs from the baseband preamplifiers are brought out differentially to pins for external filtering. An amplifier at each channel gains up the output from the external filters to a level compatible with most A-to-D Converters. A sum-of-squares detector is available for use in an Automatic Gain Control (AGC) loop to fix the output level. The RF & baseband amplifiers provide 65dB of gain control range. Additional on chip circuits allow the setting of the DC level at the I & Q channel baseband outputs, as well as nulling the DC offset at each channel.

RF Variable Gain Amplifiers

These amplifiers use the patented X-AMP™ approach with NPN-differential pairs separated by sections of resistive attenuator. The gain control is achieved through a gaussian interpolator where the control voltage steers a tail current to be supplied to the different differential pairs according to the gain desired. In the first amplifier the combined output currents from the GM cells go through a cascode stage to resistive loads with inductive peaking. In the second amplifier the differential current are split and fed the two Gilbert-cell mixers through separate cascode stages.

Mixers

Two double balanced Gilbert-cell mixers, one for each channel perform the In-phase (I) and Quadrature (Q) downconversion. Each mixer has four cross-connected transistor pairs which are terminated in resistive loads and feed the differential baseband preamplifiers for each channel. The bases of the mixer transistors are driven by the quadrature LO signals.

Baseband Preamplifiers

The baseband preamplifiers also use the X-AMP approach with NPN-differential pairs separated by sections of resistive attenuators. The same interpolator controlling the RF amplifiers controls the tail currents, of the differential pairs. The differential outputs of these preamplifiers are provided off chip for external filtering. The offset nulling minimises the DC offsets at both I and Q channels. The common-mode output voltage is set to be the same as the reference voltage (1.0V) generated in the Bias section, and made available at VREF output.

Output Amplifiers

The output amplifier gains up the signal coming back from the external filters to a level compatible with most high speed A-to-D converters (up to 1Vpp) or antialiasing filters. This amplifiers are based on an Active-feedback design (like AD830) to achieve the high gain-bandwidth and low distortion.

LO & Phase-splitters

The incoming LO signal is applied to a polyphase phase-splitter to generate the LO signals for the I-ch and Q-ch mixers. The polyphase phase-splitters are RC networks connected in a cyclical manner to achieve gain balance and phase quadrature. The wide operating frequency range of these phase-splitters is achieved by cascading multiple sections of these networks with staggered RC constants. Each branch goes through a buffer to make up for the loss and high frequency roll-off. The output from the buffers then go into another polyphase phase-splitter to enhance the accuracy of phase quadrature. Each LO signal gets buffered again to drive the mixers.

Output Level Detector

Two signals proportional to the square of each output channel are summed together and compared to a built-in threshold to create an AGC voltage (VAGC). The inputs to the detectors are referenced to VREF.

Bias

A bandgap reference generates the reference currents used by the different sections. The bandgap reference is controlled by an external power-up (ENBL) logic signal which, when set low, puts the whole chip into a sleep mode requiring less than 20uA of supply current. The reference voltage (VREF) of 1.0V which serves as the common-mode reference for the baseband circuits is made available for external use.

Evaluation Board

Figure 1. shows the schematic of the AD8347 evaluation board. Note that un-installed components are indicated with the “open” designation. The board is powered by a single supply in the range, +2.7 to +5.5V.Table II details the various configuration options of the evaluation board.

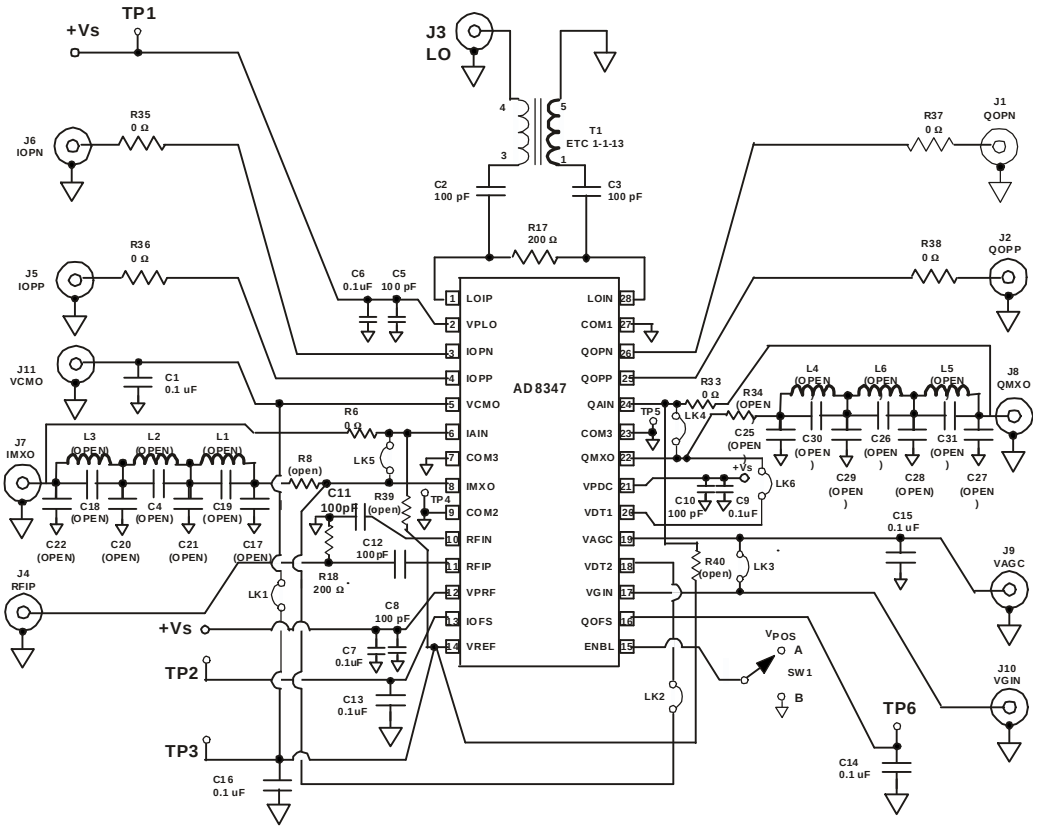

Figure 1. Evaluation Board Schematic

SILKSCREEN TOP
08-006922-03
REV A

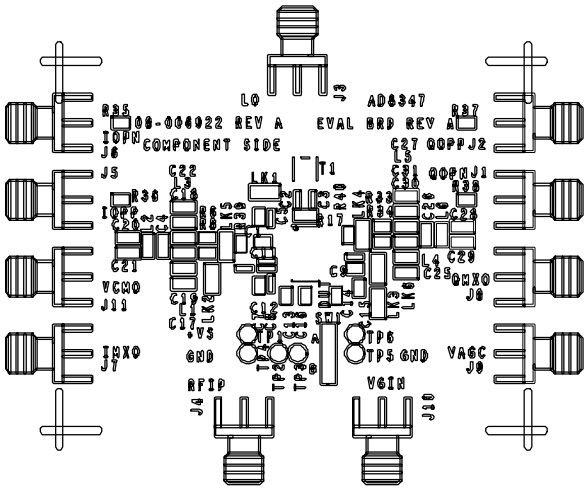

Figure 2. Silkscreen of Component Side

COMPONENT SIDE
08-006922-01
REV A

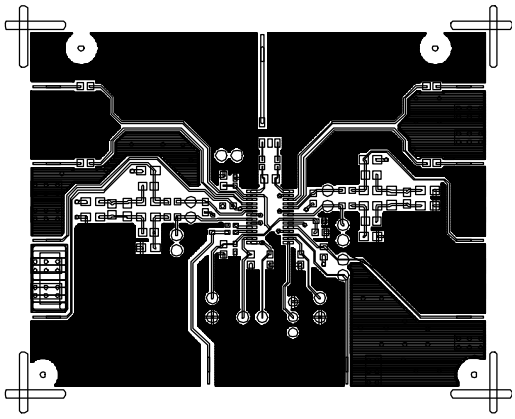

Figure 3. Layout of Component Side

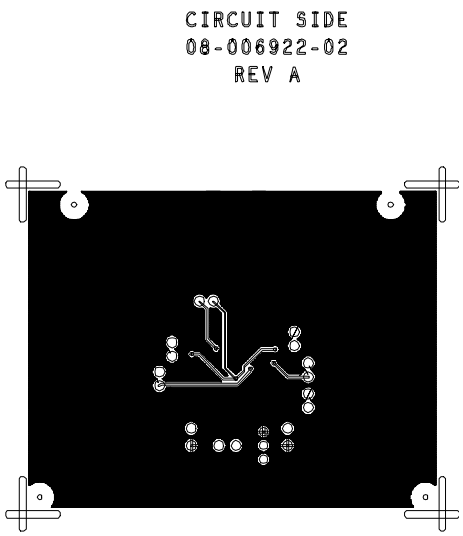

Figure 4. Layout of Circuit Side

Table II Evaluation Board Configuration Options

Component	Function	Default Condition
TP1, TP4, TP5	**Power Supply and Ground Vector Pins**	Not Applicable
TP2, TP6	**IOFS and QOFS probe points**	Not Applicable
TP3	**V_{REF} probe point**	Not Applicable
LK1, J11	**Baseband Amplifier Output Bias**: Installing this link connects VREF to VCMO. This sets the bias level on the baseband amplifiers to V_{REF} which is equal to approximately 1V. Alternatively, the bias level of the baseband amplifiers can be set by applying an external voltage to SMA connector J11	LK1 Installed
LK2, LK6, LK3, J9, J10	**AGC Mode:** Installing LK2 and LK6 connects the mixer outputs IMXO and QMXO to the detector inputs VDT2 and VDT1. By installing LK3 which connects VGIN to VAGC, the AGC mode is activated. The AGC voltage can be observed on SMA connector J9. With LK3 removed, the gain control signal for the internal variable gain amplifiers should by applied to SMA connector J10	LK2, LK6, LK3 Installed
LK4, LK5 R6, R33, L1-L5 C4, C17-C22, C25-C31 R8, R34, R39, R40	**Baseband Filtering**: Installing LK4 and LK5, connects the mixer outputs IMXO and QMXO directly to the baseband amplifier inputs IAIN and QAIN. With R6 and R33 installed (0 Ohms), IAIN and QAIN can be observed on SMA connectors J7 and J8. By removing LK4 and LK5 and installing R8 and R34, LC filters can be inserted between the mixer outputs and the baseband amplifier inputs. R8 and R34 can be used to increase the effective output impedance of IMXO and QMXO (these outputs have low output impedances). R39 and R40 can be used to provide terminations for the filter at IAIN and QAIN (IAIN and QAIN are high impedance inputs). R39 and R40 are terminated to V_{REF}.	LK4, LK5 Installed R6=R33= 0 Ohms (size 0603) L1-L5 = Open (size 0805) C4, C17-C22, C25-C31 = Open (size 0805) R8=R34= Open (0603) R39=R40= Open (0603)
R35, R36, R37, R38	Baseband Amplifier Output Series Resistors:	R35=R36=R37=R38= 0 Ohms (size 0603)
SW1	**Device Enable:** When in position A, the ENBL pin is connected to $+V_S$ and the AD8347 is in operating mode. In position B, the ENBL pin is grounded, putting the device in power down mode.	SW1=A

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead TSSOP
(RU-28)