



0.1 GHz–2.5 GHz, 70 dB Logarithmic Detector/Controller

AD8313

FEATURES

Wide Bandwidth: 0.1 GHz to 2.5 GHz Min
High Dynamic Range: 70 dB to ± 3.0 dB
High Accuracy: ± 1.0 dB over 65 dB Range (@ 1.9 GHz)
Fast Response: 40 ns Full-Scale Typical
Controller Mode with Error Output
Scaling Stable Over Supply and Temperature
Wide Supply Range: +2.7 V to +5.5 V
Low Power: 40 mW at 3 V
Power-Down Feature: 60 μ W at 3 V
Complete and Easy to Use

APPLICATIONS

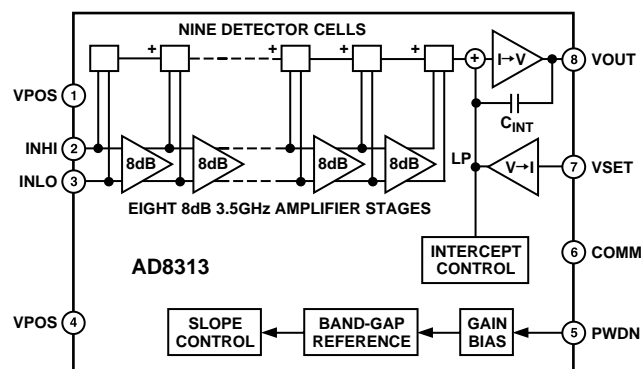
RF Transmitter Power Amplifier Setpoint
Control and Level Monitoring
Logarithmic Amplifier for RSSI Measurement
Cellular Base Stations, Radio Link, Radar

PRODUCT DESCRIPTION

The AD8313 is a complete multistage demodulating logarithmic amplifier, capable of accurately converting an RF signal at its differential input to an equivalent decibel-scaled value at its dc output. The AD8313 maintains a high degree of log conformance for signal frequencies from 0.1 GHz to 2.5 GHz and is useful over the range of 10 MHz to 3.5 GHz. The nominal input dynamic range is -65 dBm to 0 dBm (re: 50 Ω), and the sensitivity can be increased by 6 dB or more with a narrow band input impedance matching network or balun. Application is straightforward, requiring only a single supply of 2.7 V–5.5 V and the addition of a suitable input and supply decoupling. Operating on a 3 V supply, its 13.7 mA consumption (for $T_A = +25^\circ\text{C}$) amounts to only 41 mW. A power-down feature is provided; the input is taken high to initiate a low current (20 μ A) sleep mode, with a threshold at half the supply voltage.

The AD8313 uses a cascade of eight amplifier/limiter cells, each having a nominal gain of 8 dB and a -3 dB bandwidth of 3.5 GHz, for a total midband gain of 64 dB. At each amplifier output, a detector (rectifier) cell is used to convert the RF signal to baseband form; a ninth detector cell is placed directly at the input of the AD8313. The current-mode outputs of these cells are summed to generate a piecewise linear approximation to the logarithmic function, and converted to a low impedance voltage-mode output by a transresistance stage, which also acts as a low-pass filter.

FUNCTIONAL BLOCK DIAGRAM



When used as a log amp, the scaling is determined by a separate feedback interface (a transconductance stage) that sets the slope to approximately 18 mV/dB; used as a controller, this stage accepts the setpoint input. The logarithmic intercept is positioned to nearly -100 dBm, and the output runs from about 0.45 V dc at -73 dBm input to 1.75 V dc at 0 dBm input. The scale and intercept are supply and temperature stable.

The AD8313 is fabricated on Analog Devices' advanced 25 GHz silicon bipolar IC process and is available in a 8-lead μ SOIC package. The operating temperature range is -40°C to $+85^\circ\text{C}$. An evaluation board is available.

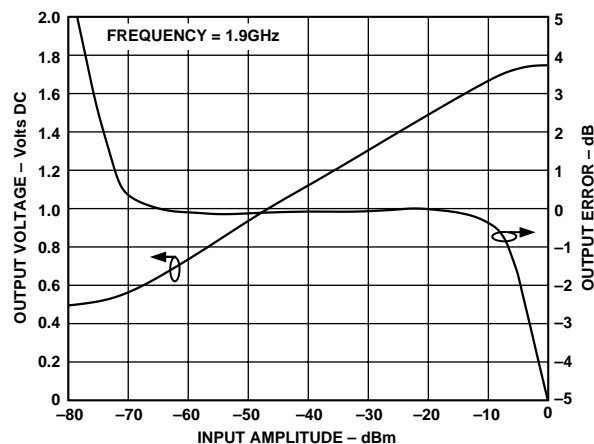


Figure 1. Typical Logarithmic Response and Error vs. Input Amplitude

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: <http://www.analog.com>
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AD8313—SPECIFICATIONS (@ T_A = +25°C, V_S = +5.0 V¹, R_L ≥ 10 kΩ unless otherwise noted)

Parameter	Conditions	Min ²	Typ	Max ²	Units
SIGNAL INPUT INTERFACE					
Specified Frequency Range		0.1		2.5	GHz
DC Common-Mode Voltage			V _{POS} – 0.75		V
Input Bias Currents			10		μA
Input Impedance	f _{RF} < 100 MHz ³		900 1.1		Ω pF ⁴
LOG (RSSI) MODE	Sinusoidal, input termination configuration shown in Figure 27.				
100 MHz ⁵	Nominal Conditions				
±3 dB Dynamic Range ⁶		53.5	65		dB
Range Center			–31.5		dBm
±1 dB Dynamic Range			56		dB
Slope		17	19	21	mV/dB
Intercept		–96	–88	–80	dBm
	+2.7 V ≤ V _S ≤ +5.5 V, –40°C ≤ T ≤ +85°C				
±3 dB Dynamic Range		51	64		dB
Range Center			–31		dBm
±1 dB Dynamic Range			55		dB
Slope		16	19	22	mV/dB
Intercept		–99	–89	–75	dBm
Temperature Sensitivity	P _{IN} = –10 dBm		–0.022		dB/°C
900 MHz ⁵	Nominal Conditions				
±3 dB Dynamic Range		60	69		dB
Range Center			–32.5		dBm
±1 dB Dynamic Range			62		dB
Slope		15.5	18	20.5	mV/dB
Intercept		–105	–93	–81	dBm
	+2.7 V ≤ V _S ≤ +5.5 V, –40°C ≤ T ≤ +85°C				
±3 dB Dynamic Range		55.5	68.5		dB
Range Center			–32.75		dBm
±1 dB Dynamic Range			61		dB
Slope		15	18	21	mV/dB
Intercept		–110	–95	–80	dBm
Temperature Sensitivity	P _{IN} = –10 dBm		–0.019		dB/°C
1.9 GHz ⁷	Nominal Conditions				
±3 dB Dynamic Range		52	73		dB
Range Center			–36.5		dBm
±1 dB Dynamic Range			62		dB
Slope		15	17.5	20.5	mV/dB
Intercept		–115	–100	–85	dBm
	+2.7 V ≤ V _S ≤ +5.5 V, –40°C ≤ T ≤ +85°C				
±3 dB Dynamic Range		50	73		dB
Range Center			36.5		dBm
±1 dB Dynamic Range			60		dB
Slope		14	17.5	21.5	mV/dB
Intercept		–125	–101	–78	dBm
Temperature Sensitivity	P _{IN} = –10 dBm		–0.019		dB/°C
2.5 GHz ⁷	Nominal Conditions				
±3 dB Dynamic Range		48	66		dB
Range Center			–34		dBm
±1 dB Dynamic Range			46		dB
Slope		16	20	25	mV/dB
Intercept		–111	–92	–72	dBm
	+2.7 V ≤ V _S ≤ +5.5 V, –40°C ≤ T ≤ +85°C				
±3 dB Dynamic Range		47	68		dB
Range Center			–34.5		dBm
±1 dB Dynamic Range			46		dB
Slope		14.5	20	25	mV/dB
Intercept		–128	–92	–56	dBm
Temperature Sensitivity	P _{IN} = –10 dBm		–0.040		dB/°C

Parameter	Conditions	Min ²	Typ	Max ²	Units
3.5 GHz ⁵					
±3 dB Dynamic Range			43		dB
±1 dB Dynamic Range			35		dB
Slope			24		mV/dB
Intercept			−65		dBm
CONTROL MODE					
Controller Sensitivity	f = 900 MHz		23		V/dB
Low Frequency Gain	VSET to VOUT ⁸		84		dB
Open-Loop Corner Frequency	VSET to VOUT ⁸		700		Hz
Open-Loop Slew Rate	f = 900 MHz		2.5		V/μs
VSET Delay Time			150		ns
VOUT INTERFACE					
Current Drive Capability					
Source Current			400		μA
Sink Current			10		mA
Minimum Output Voltage	Open Loop		50		mV
Maximum Output Voltage	Open Loop		V _{POS} − 0.1		V
Output Noise Spectral Density	P _{IN} = −60 dBm, f _{SPOT} = 100 Hz		2.0		μV/√Hz
	P _{IN} = −60 dBm, f _{SPOT} = 10 MHz		1.3		μV/√Hz
Small Signal Response Time	P _{IN} = −60 dBm to −57 dBm, 10% to 90%		40	60	ns
Large Signal Response Time	P _{IN} = No Signal to 0 dBm, Settled to 0.5 dB		110	160	ns
VSET INTERFACE					
Input Voltage Range		0		V _{POS}	V
Input Impedance			18k 1		Ω pF
POWER-DOWN INTERFACE					
PWDN Threshold			V _{POS} /2		V
Power-Up Response Time	Time delay following HI to LO transition until device meets full specifications.		1.8		μs
PWDN Input Bias Current	PWDN = 0 V		5		μA
	PWDN = V _S		<1		μA
POWER SUPPLY					
Operating Range		+2.7		+5.5	V
Powered Up Current			13.7	15.5	mA
	+4.5 V ≤ V _S ≤ +5.5 V, −40°C ≤ T ≤ +85°C			18.5	mA
	+2.7 V ≤ V _S ≤ +3.3 V, −40°C ≤ T ≤ +85°C			18.5	mA
Powered Down Current	+4.5 V ≤ V _S ≤ +5.5 V, −40°C ≤ T ≤ +85°C		50	150	μA
	+2.7 V ≤ V _S ≤ +3.3 V, −40°C ≤ T ≤ +85°C		20	50	μA

NOTES

¹Except where otherwise noted, performance at V_S = +3.0 V is equivalent to +5.0 V operation.

²Minimum and maximum specified limits on parameters that are guaranteed but not tested are six sigma values.

³Input impedance shown over frequency range in Figure 24.

⁴Double slashes (||) denote “in parallel with.”

⁵Linear regression calculation for error curve taken from −40 dBm to −10 dBm for all parameters.

⁶Dynamic range refers to range over which the linearity error remains within the stated bound.

⁷Linear regression calculation for error curve taken from −60 dBm to −5 dBm for 3 dB dynamic range. All other regressions taken from −40 dBm to −10 dBm.

⁸AC response shown in Figure 10.

Specifications subject to change without notice.

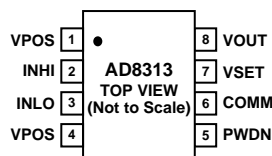
AD8313

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage V_S 5.5 V
 VOUT, VSET, PWDN 0 V, VPOS
 Input Power Differential (re: 50 Ω , 5.5 V) +25 dBm
 Input Power Single-Ended (re: 50 Ω , 5.5 V) +19 dBm
 Internal Power Dissipation 200 mW
 θ_{JA} 200°C/W
 Maximum Junction Temperature +125°C
 Operating Temperature Range -40°C to +85°C
 Storage Temperature Range -65°C to +150°C
 Lead Temperature Range (Soldering 60 sec) +300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin	Name	Description
1, 4	VPOS	Positive supply voltage (VPOS), +2.7 V to +5.5 V.
2	INHI	Noninverting Input. This input should be ac coupled.
3	INLO	Inverting Input. This input should be ac coupled.
5	PWDN	Connect pin to ground for normal operating mode. Connect pin to supply for power-down mode.
6	COMM	Device Common.
7	VSET	Setpoint input for operation in controller mode. To operate in RSSI mode, short VSET and VOUT.
8	VOUT	Logarithmic/Error Output.

ORDERING GUIDE

Model	Temperature Range	Package Descriptions	Package Option	Brand Code
AD8313ARM	-40°C to +85°C	8-Lead μ SOIC	RM-08	J1A
AD8313ARM-REEL	-40°C to +85°C	13" Tape and Reel	RM-08	J1A
AD8313ARM-REEL7	-40°C to +85°C	7" Tape and Reel	RM-08	J1A
AD8313-EVAL		Evaluation Board		

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8313 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy [>250 V HBM] electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Typical Performance Characteristics–AD8313

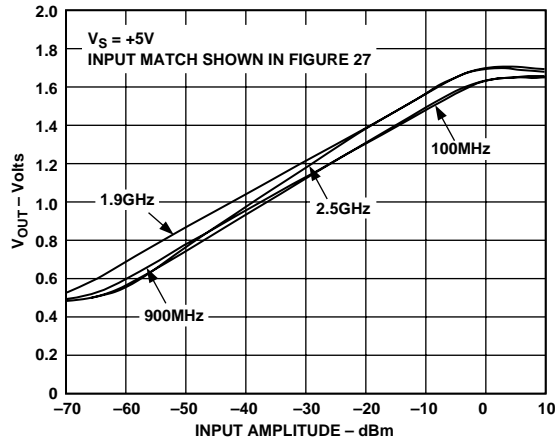


Figure 2. V_{OUT} vs. Input Amplitude

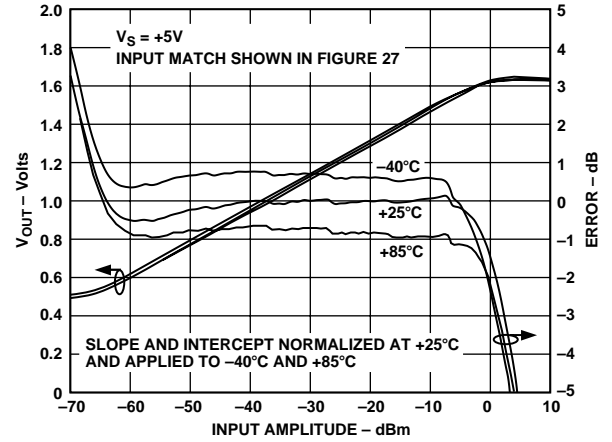


Figure 5. V_{OUT} and Log Conformance vs. Input Amplitude at 900 MHz; -40°C , $+25^{\circ}\text{C}$ and $+85^{\circ}\text{C}$

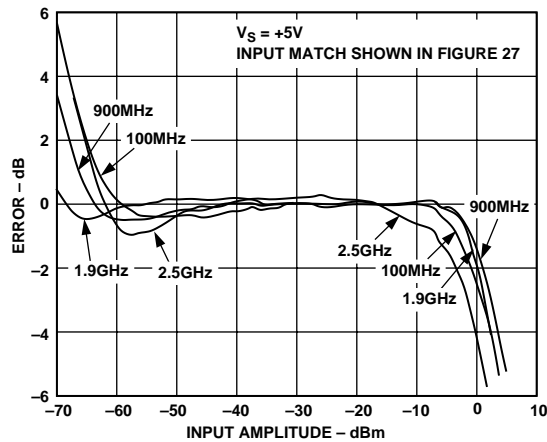


Figure 3. Log Conformance vs. Input Amplitude

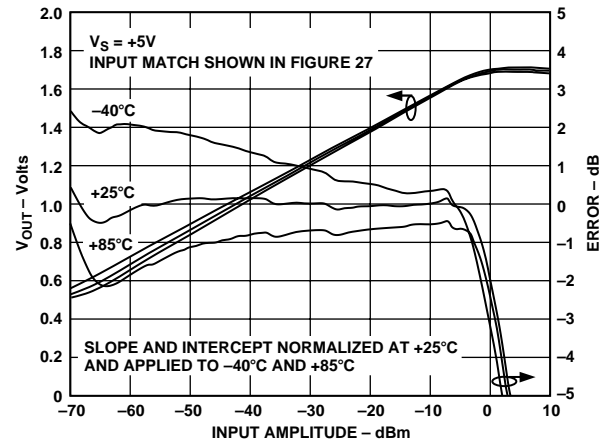


Figure 6. V_{OUT} and Log Conformance vs. Input Amplitude at 1.9 GHz; -40°C , $+25^{\circ}\text{C}$ and $+85^{\circ}\text{C}$

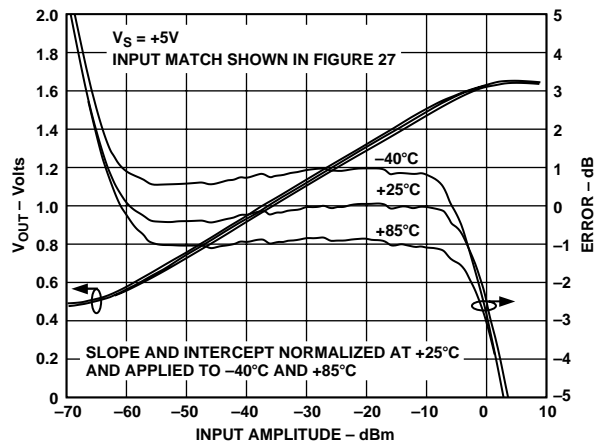


Figure 4. V_{OUT} and Log Conformance vs. Input Amplitude at 100 MHz; -40°C , $+25^{\circ}\text{C}$ and $+85^{\circ}\text{C}$

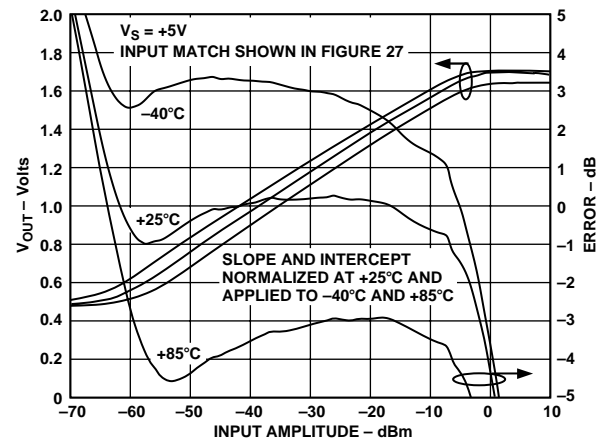


Figure 7. V_{OUT} and Log Conformance vs. Input Amplitude at 2.5 GHz; -40°C , $+25^{\circ}\text{C}$ and $+85^{\circ}\text{C}$

AD8313

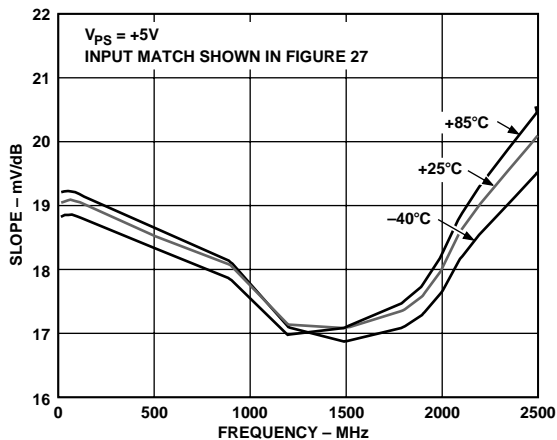


Figure 8. V_{OUT} Slope vs. Frequency; -40°C , $+25^{\circ}\text{C}$ and $+85^{\circ}\text{C}$

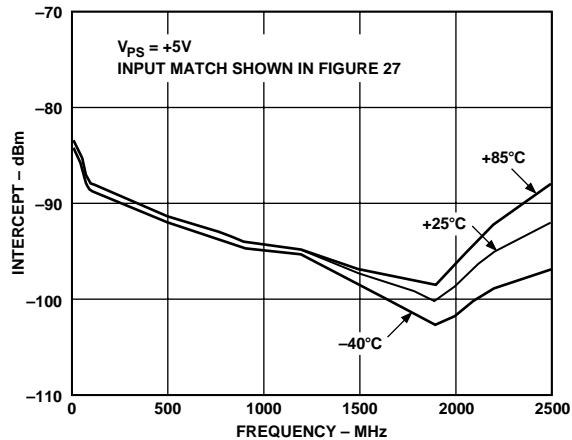


Figure 11. V_{OUT} Intercept vs. Frequency; -40°C , $+25^{\circ}\text{C}$ and $+85^{\circ}\text{C}$

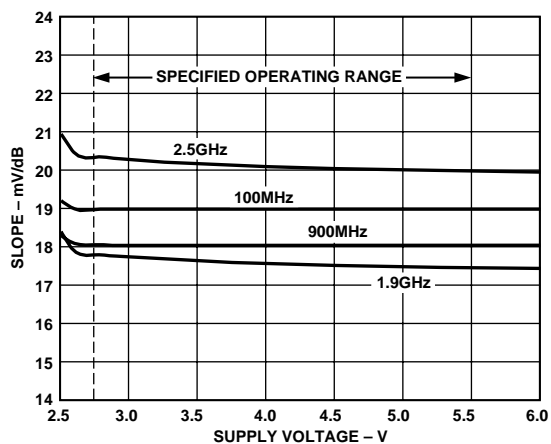


Figure 9. V_{OUT} Slope vs. Supply Voltage

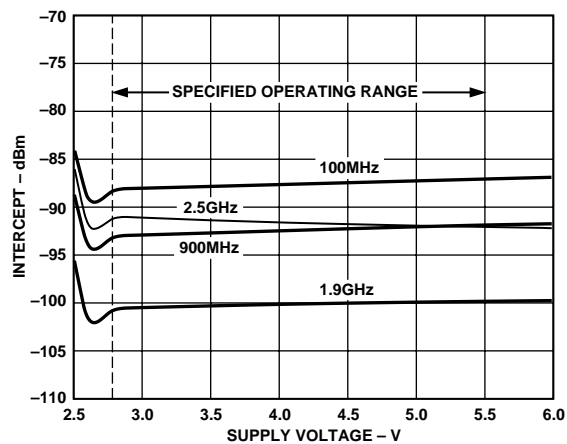


Figure 12. V_{OUT} Intercept vs. Supply Voltage

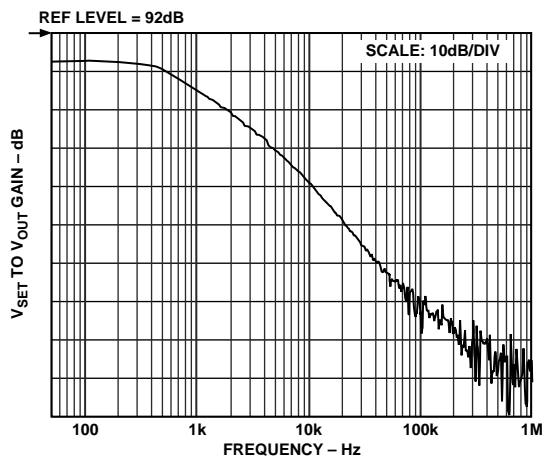


Figure 10. AC Response from V_{SET} to V_{OUT}

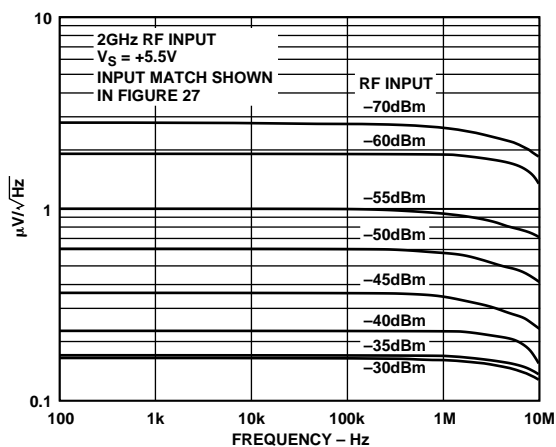


Figure 13. V_{OUT} Noise Spectral Density

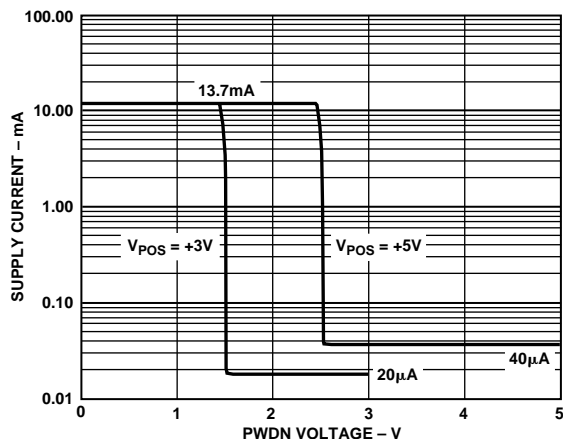


Figure 14. Typical Supply Current vs. PWDN Voltage

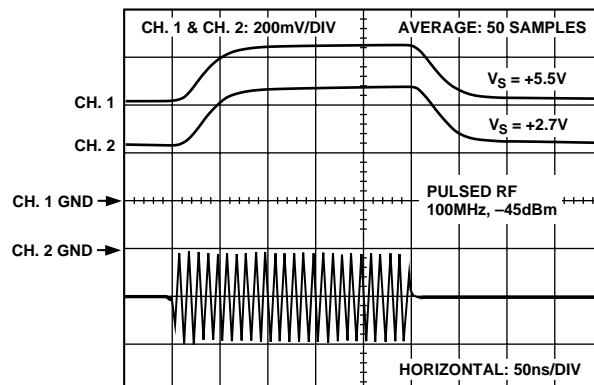


Figure 17. Response Time, No Signal to -45 dBm

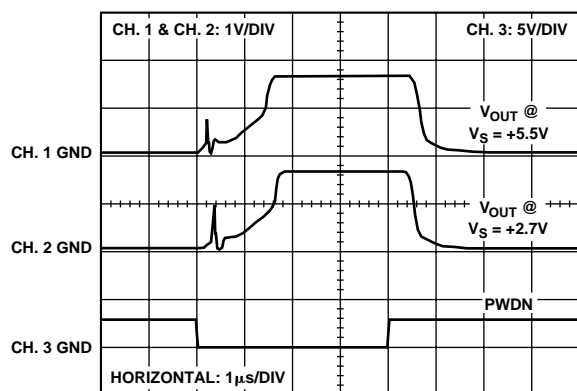


Figure 15. PWDN Response Time

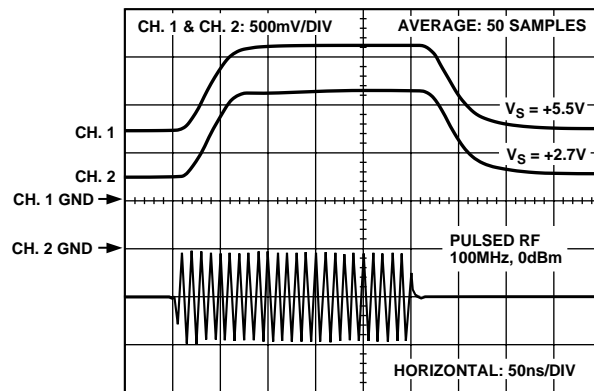


Figure 18. Response Time, No Signal to +0 dBm

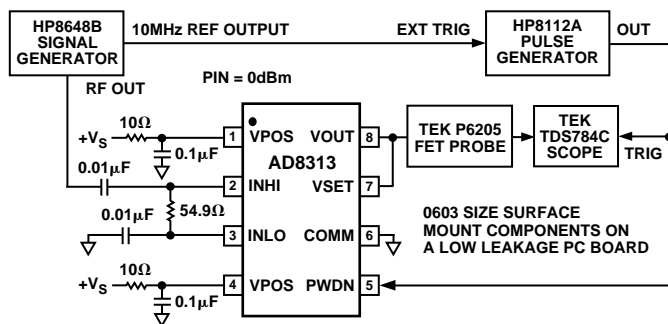


Figure 16. Test Setup for PWDN Response Time

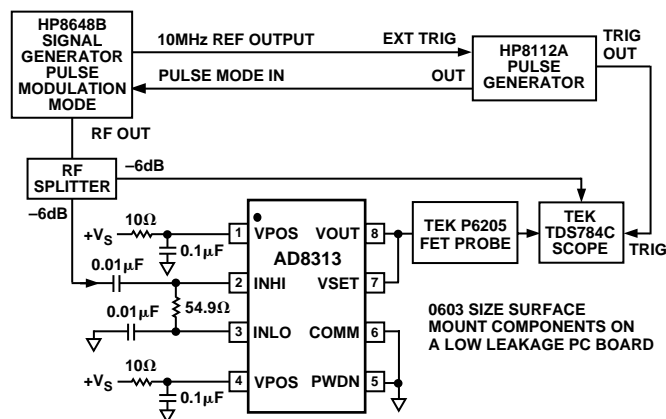


Figure 19. Test Setup for RSSI-Mode Pulse Response

AD8313

CIRCUIT DESCRIPTION

The AD8313 is essentially an 8-stage logarithmic amplifier, specifically designed for use in RF measurement and power amplifier control applications at frequencies up to 2.5 GHz. A block diagram is shown in Figure 20. (For a full treatment of log-amp theory and design principles, consult the AD8307 data sheet).

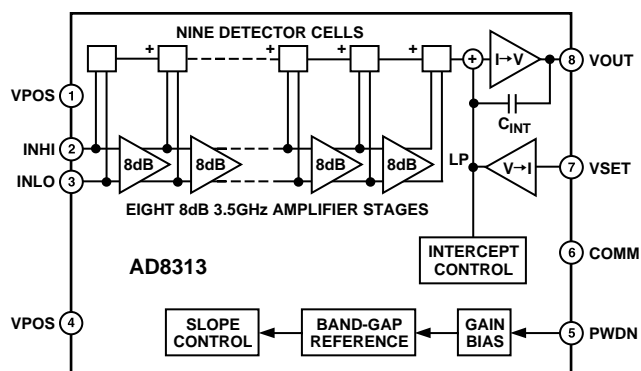


Figure 20. Block Diagram

A fully-differential design is used, and the inputs INHI and INLO (Pins 2 and 3) are internally biased to approximately 0.75 V below the supply voltage, and present a low frequency impedance of nominally 900 Ω in parallel with 1.1 pF. The noise spectral density referred to the input is 0.6 nV/√Hz, equivalent to a voltage of 35 μV rms in a 3.5 GHz bandwidth, or a noise power of -76 dBm re: 50 Ω. This sets the lower limit to the dynamic range; the Applications section shows how to increase the sensitivity by the use of a matching network or input transformer. However, the low end accuracy of the AD8313 is enhanced by specially shaping the demodulation transfer characteristic to partially compensate for errors due to internal noise.

Each of the eight cascaded stages has a nominal voltage gain of 8 dB and a bandwidth of 3.5 GHz, and is supported by precision biasing cells which determine this gain and stabilize it against supply and temperature variations. Since these stages are direct-coupled and the dc gain is high, an offset-compensation loop is included. The first four of these stages, and the biasing system, are powered from Pin 4, while the later stages and the output interfaces are powered from Pin 1. The biasing is controlled by a logic interface PWDN (Pin 5); this is grounded for normal operation, but may be taken high (to VS) to disable the chip. The threshold is at VPOS/2 and the biasing functions are enabled and disabled within 1.8 μs.

Each amplifier stage has a detector cell associated with its output. These nonlinear cells essentially perform an absolute-value (full-wave rectification) function on the differential voltages along this backbone, in a transconductance fashion; their outputs are in current-mode form and are thus easily summed. A ninth detector cell is added at the input of the AD8313. Since the mid-range response of each of these nine detector stages is separated by 8 dB, the overall dynamic range is about 72 dB (Figure 21). The upper end of this range is determined by the capacity of the first detector cell, and occurs at approximately 0 dBm. The practical dynamic range is over 70 dB, to the ±3 dB error points. However, some erosion of this range will occur at temperature and frequency extremes. Useful operation to over 3 GHz is possible, and the AD8313 remains serviceable at 10 MHz (see Typical Performance Characteristics), needing only a small amount of additional ripple filtering.

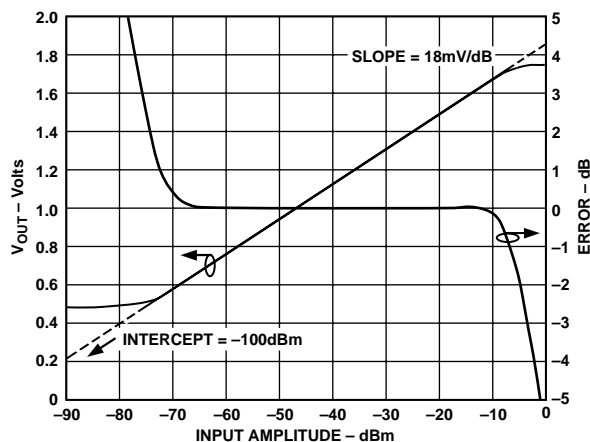


Figure 21. Typical RSSI Response and Error vs. Input Power at 1.9 GHz

The fluctuating current output generated by the detector cells, with a fundamental component at twice the signal frequency, is filtered first by a low-pass section inside each cell, and also by the output stage. The output stage converts these currents to a voltage, VOUT, at pin VOUT (Pin 8), which can swing “rail-to-rail.” The filter exhibits a two-pole response with a corner at approximately 12 MHz and full-scale rise time (10%–90%) of 40 ns. The residual output ripple at an input frequency of 100 MHz has an amplitude of under 1 mV. The output can drive a small resistive load: it can source currents of up to 400 μA, and sink up to 10 mA. The output is stable with any capacitive load, though settling time may be impaired. The low frequency incremental output impedance is approximately 0.2 Ω.

In addition to its use as an RF power measurement device (that is, as a logarithmic amplifier) the AD8313 may also be used in controller applications, by breaking the feedback path from VOUT to the VSET (Pin 7), which determines the slope of the output (nominally 18 mV/dB). This pin becomes the setpoint input in controller modes. In this mode, the voltage VOUT remains close to ground (typically under 50 mV) until the decibel equivalent of the voltage VSET is reached at the input, when VOUT makes a rapid transition to a voltage close to VPOS (see controller mode). The logarithmic intercept is nominally positioned at -100 dBm (re: 50 Ω) and this is effective in both the log amp mode and the controller mode.

Thus, with Pins 7 and 8 connected (log amp mode) we have:

$$V_{OUT} = V_{SLOPE} (P_{IN} + 100 \text{ dBm})$$

where P_{IN} is the input power, stated in dBm when the source is directly terminated in 50 Ω. However, the input impedance of the AD8313 is much higher than 50 Ω and the sensitivity of this device may be increased by about 12 dB by using some type of matching network (see below), which adds a voltage gain and lowers the intercept by the same amount. This dependence on the choice of reference impedance can be avoided by restating the expression as:

$$V_{OUT} = 20 \times V_{SLOPE} \times \log (V_{IN}/2.2 \mu V)$$

where V_{IN} is the rms value of a sinusoidal input appearing across Pins 2 and 3; here, 2.2 μV corresponds to the intercept, expressed in voltage terms. (For a more thorough treatment of the effect of signal waveform and metrics on the intercept positioning for a log amp, see the AD8307 data sheet).

With Pins 7 and 8 disconnected (controller mode), the output may be stated as

$$V_{OUT} \rightarrow V_S \quad \text{when} \quad V_{SLOPE} (P_{IN} + 100) > V_{SET}$$

$$V_{OUT} \rightarrow 0 \quad \text{when} \quad V_{SLOPE} (P_{IN} + 100) < V_{SET}$$

when the input is stated in terms of the power of a sinusoidal signal across a net termination impedance of 50 Ω. The transition zone between high and low states is very narrow, since the output stage behaves essentially as a fast integrator. The above equations may be restated as

$$V_{OUT} \rightarrow V_S \quad \text{when} \quad V_{SLOPE} \log (V_{IN}/2.2 \mu V) > V_{SET}$$

$$V_{OUT} \rightarrow 0 \quad \text{when} \quad V_{SLOPE} \log (V_{IN}/2.2 \mu V) < V_{SET}$$

A further use of the separate VOUT and VSET pins is in raising the load-driving current capability by the inclusion of an external NPN emitter follower. More complete information about usage in these various modes is provided in the Applications section.

INTERFACES

This section describes the signal and control interfaces and their behavior. On-chip resistances and capacitances exhibit variations of up to ±20%. These resistances are sometimes temperature dependent and the capacitances may be voltage dependent.

Power-Down Interface, PWDN

The power-down threshold is accurately centered at the midpoint of the supply as shown in Figure 22. If Pin 5 is left unconnected or tied to the supply voltage (recommended) the bias enable current is shut off, and the current drawn from the supply is predominately through a nominal 300 kΩ chain (20 μA at 3 V). When grounded, the bias system is turned on. The threshold level is accurately at V_{POS}/2. The input bias current at the PWDN pin when operating in the device "ON" state is approximately 5 μA for V_{POS} = 3 V.

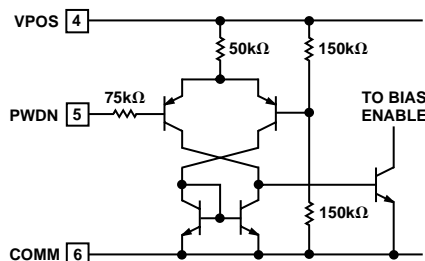


Figure 22. Power-Down Threshold Circuitry

Signal Inputs, INHI, INLO

The simplest low frequency ac model for this interface consists of just a 900 Ω resistance R_{IN} in shunt with a 1.1 pF input capacitance, C_{IN} connected across INHI and INLO. Figure 23 shows these distributed in the context of a more complete schematic. The input bias voltage shown is for the enabled chip; when disabled, it will rise by a few hundred millivolts. If the input is coupled via capacitors, this change may cause a low-level signal transient to be introduced, having a time-constant formed by these capacitors and R_{IN}. For this reason, large-valued coupling capacitors should be well matched; this is not necessary when using the small capacitors found in many impedance transforming networks used at high frequencies.

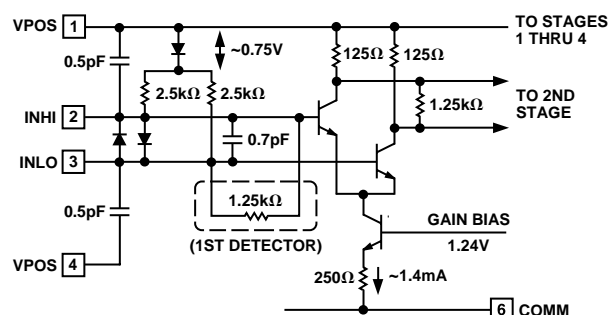


Figure 23. Input Interface Simplified Schematic

For high frequency use, Figure 24 shows the input impedance plotted on a Smith chart. This measured result of a typical device includes a 191 mil 50 Ω trace and a 680 pF capacitor to ground from the INLO pin.

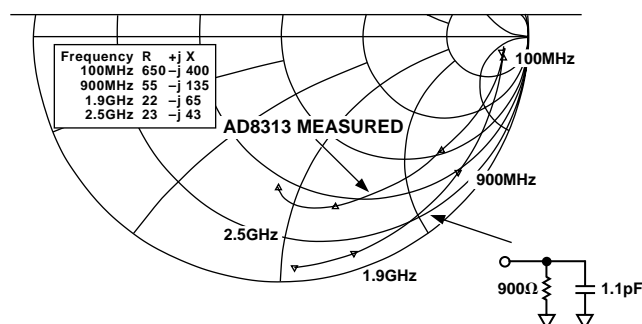


Figure 24. Typical Input Impedance

Logarithmic/Error Output, VOUT

The rail-to-rail output interface is shown in Figure 25. V_{OUT} can run from within about 50 mV of ground, to within about 100 mV of the supply voltage, and is short-circuit safe to either supply. However, the sourcing load current I_{SOURCE} is limited by that provided by the PNP transistor, to typically 400 μA. Larger load currents can be provided by adding an external NPN transistor (see Applications). The dc open-loop gain of this amplifier is high, and it may be regarded essentially as an integrator having a capacitance of 2 pF (C_{INT}) driven by the current-mode signals generated by the summed outputs of the nine detector stages, which is scaled approximately 4.0 μA/dB.

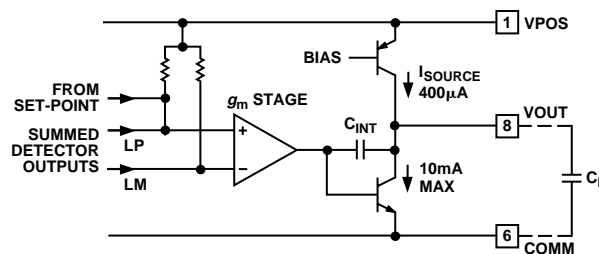


Figure 25. Output Interface Circuitry

Thus, for a midscale RF input of about 3 mV, which is some 40 dB above the minimum detector output, this current is 160 μA and the output changes by 8 V/μs. When VOUT is connected to VSET, the rise and fall times are approximately 40 ns (for R_L ≥ 10 kΩ). The nominal slew rate is ±2.5 V/μs. The HF compensation technique results in stable operation with a large capacitive load, C_L, though the positive-going slew rate will then be limited by I_{SOURCE}/C_L to 1 V/μs for C_L = 400 pF.

AD8313

Setpoint Interface, VSET

The setpoint interface is shown in Figure 26. The voltage V_{SET} is divided by a factor of three in a resistive attenuator of total resistance 18 k Ω . The signal is converted to a current by the action of the op amp and the resistor R3 (1.5 k Ω), which balances the current generated by the summed output of the nine detector cells at the input to the previous cell. The logarithmic slope is nominally $3 \times 4.0 \mu\text{A/dB} \times 1.5 \text{ k}\Omega \approx 18 \text{ mV/dB}$.

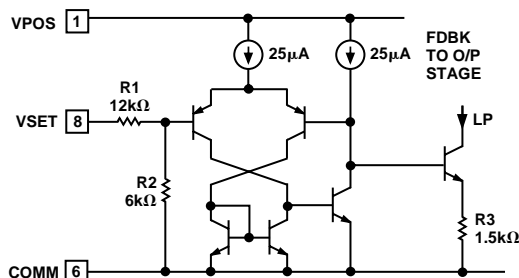


Figure 26. Setpoint Interface Circuitry

APPLICATIONS

Basic Connections for Log (RSSI) Mode

Figure 27 shows the AD8313 connected in its basic measurement mode. A power supply of +2.7 V to +5.5 V is required. The power supply to each of the VPOS pins should be decoupled with a 0.1 μF , surface mount ceramic capacitor and a series resistor of 10 Ω .

The PWDN pin is shown as grounded. The AD8313 may be disabled by a logic “HI” at this pin. When disabled, the chip current is reduced to about 20 μA from its normal value of 13.7 mA. The logic threshold is at $V_{POS}/2$ and the enable function occurs in about 1.8 μs ; note, however, that further settling time is generally needed at low input levels. While the input in this case is terminated with a simple 50 Ω broadband resistive match, there are a wide variety of ways in which the input termination can be accomplished. These are discussed in the Input Coupling section.

VSET is connected to VOUT to establish a feedback path that controls the overall scaling of the logarithmic amplifier. The load resistance, R_L , should not be lower than 5 k Ω in order that the full-scale output of 1.75 V can be generated with the limited available current of 400 μA max.

As stated in the Absolute Maximum Ratings, an externally applied overvoltage on the VOUT pin that is outside the range 0 V to V_{POS} is sufficient to cause permanent damage to the device. If overvoltages are expected on the VOUT pin, a series resistor (R_{PROT}) should be included as shown. A 500 Ω resistor is sufficient to protect against overvoltage up to $\pm 5 \text{ V}$; 1000 Ω should be used if an overvoltage of up to $\pm 15 \text{ V}$ is expected. Since the output stage is meant to drive loads of no more than 400 μA , this resistor will not impact device performance for more high impedance drive applications (higher output current applications are discussed in the Increasing Output Current section).

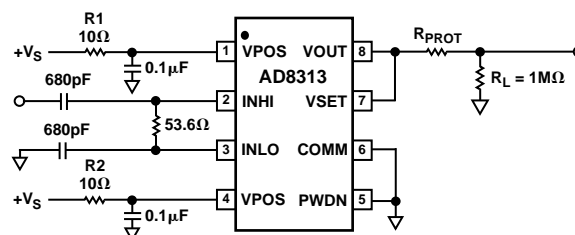


Figure 27. Basic Connections for Log (RSSI) Mode

Operating in the Controller Mode

Figure 28 shows the basic connections for operation in controller mode. The link between VOUT and VSET is broken and a “setpoint” is applied to VSET. Any difference between V_{SET} and the equivalent input power to the AD8313, will drive V_{OUT} either to the supply rail or close to ground. If V_{SET} is greater than the equivalent input power, V_{OUT} will be driven towards ground and vice versa.

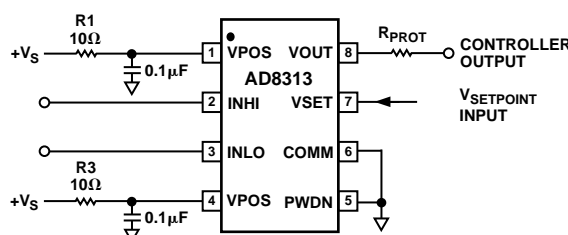


Figure 28. Basic Connections for Operation in the Controller Mode

This mode of operation is useful in applications where the output power of an RF power amplifier (PA) is to be controlled by an analog AGC loop (Figure 29). In this mode, a setpoint voltage, proportional in dB to the desired output power, is applied to the VSET pin. A sample of the output power from the PA, via a directional coupler or other means, is fed to the input of the AD8313.

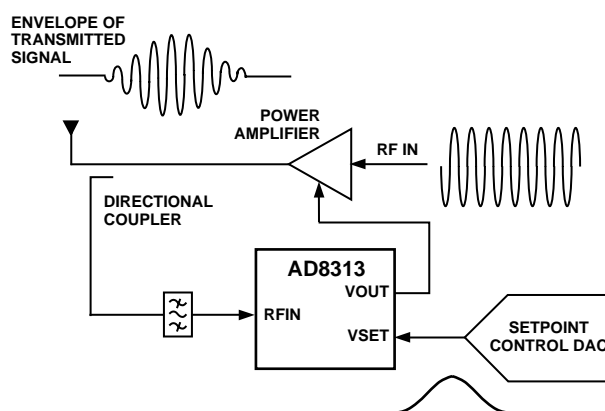


Figure 29. Setpoint Controller Operation

V_{OUT} is applied to the gain control terminal of the power amplifier. The gain control transfer function of the power amplifier should be an inverse relationship, i.e., increasing voltage decreases gain.

A positive input step on V_{SET} (indicating a demand for increased power from the PA) will drive V_{OUT} towards ground. This should be arranged to increase the gain of the PA. The loop will settle when V_{OUT} settles to a voltage that sets the input power to the AD8313 to the dB equivalent of V_{SET} .

Input Coupling

The signal may be coupled to the AD8313 in a variety of ways. In all cases, there must not be a dc path from the input pins to ground. Some of the possibilities include: dual input coupling capacitors, a flux-linked transformer, a printed-circuit balun, direct drive from a directional coupler, or a narrow-band impedance matching network.

Figure 30 shows a simple broadband resistive match. A termination resistor of $53.6\ \Omega$ combines with the internal input impedance of the AD8313 to give an overall resistive input impedance of approximately $50\ \Omega$. The termination resistor should preferably be placed directly across the input pins, INHI to INLO, where it serves to lower the possible deleterious effects of dc offset voltages on the low end of the dynamic range. At low frequencies, this may not be quite as attractive, since it necessitates the use of larger coupling capacitors. The two $680\ \text{pF}$ input coupling capacitors set the high-pass corner frequency of the network at $9.4\ \text{MHz}$.

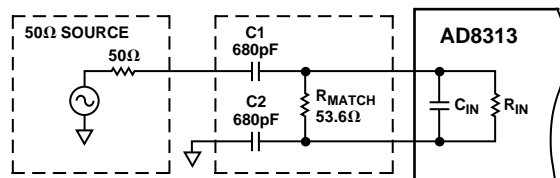


Figure 30. A Simple Broadband Resistive Input Termination

The high pass corner frequency can be set higher according to the equation:

$$f_{3dB} = \frac{1}{2 \times \pi \times C \times 50}$$

where: $C = \frac{C1 \times C2}{C1 + C2}$

In high frequency applications, the use of a transformer, balun or matching network is advantageous. The impedance matching characteristics of these networks provide what is essentially a gain stage before the AD8313 that increases the device sensitivity. This gain effect is further explored in the following matching example.

Figures 31 and 32 show device performance under these three input conditions at $900\ \text{MHz}$ and $1900\ \text{MHz}$.

While the $900\ \text{MHz}$ case clearly shows the effect of input matching by realigning the intercept as expected, little improvement is seen at $1.9\ \text{GHz}$. Clearly, if no improvement in sensitivity is required, a simple $50\ \Omega$ termination may be the best choice for a given design based on ease of use and cost of components.

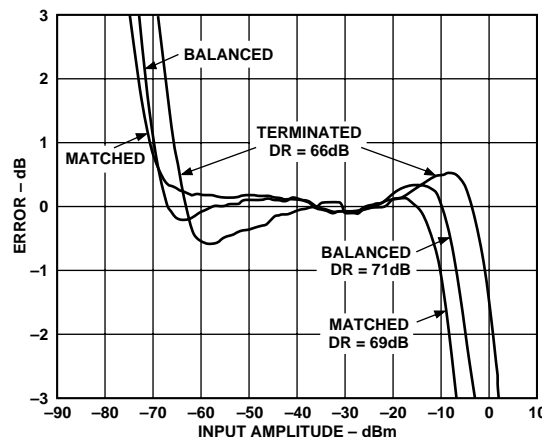


Figure 31. Comparison of Terminated, Matched and Balanced Input Drive at $900\ \text{MHz}$

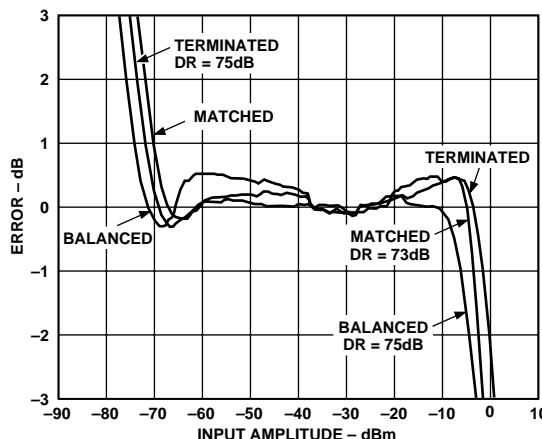


Figure 32. Comparison of Terminated, Matched and Balanced Input Drive at $1900\ \text{MHz}$

A Narrow-Band LC Matching Example at $100\ \text{MHz}$

While numerous software programs are available that allow the values of matching components to be easily calculated, a clear understanding of the calculations involved is valuable. A low frequency ($100\ \text{MHz}$) value has been used for this exercise because of the deleterious board effects at higher frequencies. RF layout simulation software is useful when board design at higher frequencies is required.

A narrow-band LC match can be implemented either as a series-inductance/shunt-capacitance or as a series-capacitance/shunt-inductance. However, the concurrent requirement that the AD8313 inputs, INHI and INLO, be ac-coupled, makes a series-capacitance/shunt-inductance type match more appropriate (see Figure 33).

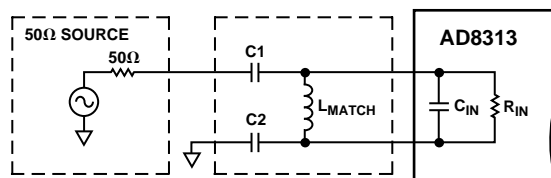


Figure 33. Narrow-Band Reactive Match

AD8313

Typically, the AD8313 will need to be matched to 50 Ω. The input impedance of the AD8313 at 100 MHz can be read from the Smith Chart (Figure 24) and corresponds to a resistive input impedance of 900 Ω in parallel with a capacitance of 1.1 pF.

To make the matching process simpler, the input capacitance of the AD8313, C_{IN} , can be temporarily removed from the calculation by adding a virtual shunt inductor (L_2), which will resonate away C_{IN} (Figure 34). This inductor will be factored back into the calculation later. This allows the main calculation to be based on a simple resistive-to-resistive match (i.e., 50 Ω to 900 Ω).

The resonant frequency is defined by the equation

$$\omega = \frac{1}{\sqrt{L_2 C_{IN}}}$$

therefore: $L_2 = \frac{1}{\omega^2 C_{IN}} = 2.3 \mu H$

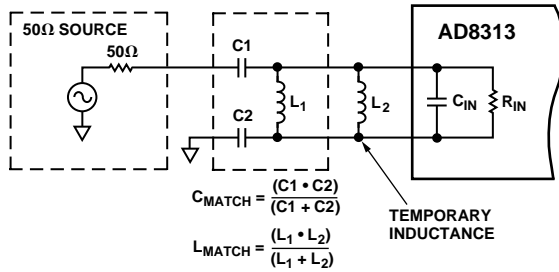


Figure 34. Input Matching Example

With C_{IN} and L_2 temporarily out of the picture, the focus is now on matching a 50 Ω source resistance to a (purely resistive) load of 900 Ω and calculating values for C_{MATCH} and L_1 .

When $R_S R_{IN} = \frac{L_1}{C_{MATCH}}$

the input will look purely resistive at a frequency given by

$$f_o = \frac{1}{2\pi\sqrt{L_1 C_{MATCH}}} = 100 \text{ MHz}$$

Solving for C_{MATCH} gives

$$C_{MATCH} = \frac{1}{\sqrt{R_S R_{IN}}} \frac{1}{2\pi f_o} = 7.5 \text{ pF}$$

Solving for L_1 gives

$$L_1 = \frac{\sqrt{R_S R_{IN}}}{2\pi f_o} = 337.6 \text{ nH}$$

Because L_1 and L_2 are in parallel, they can be combined to give the final value for L_{MATCH} (i.e.)

$$L_{MATCH} = \frac{L_1 L_2}{L_1 + L_2} = 294 \text{ nH}$$

$C1$ and $C2$ can be chosen in a number of ways. First $C2$ can be set to a large value such as 1000 pF, so that it appears as an RF short. $C1$ would then be set equal to the calculated value of C_{MATCH} . Alternatively, $C1$ and $C2$ can each be set to twice C_{MATCH} so that the total series capacitance is equal to C_{MATCH} . By making $C1$ and $C2$ slightly unequal (i.e., select $C2$ to be about 10% less than $C1$) but keeping their series value the same, the amplitude of the signals on INHI and INLO can be equalized so that the AD8313 is driven in a more balanced manner. Any one of the three options detailed above can be used as long as the combined series value of $C1$ and $C2$ (i.e., $C1 \times C2 / (C1 + C2)$) is equal to C_{MATCH} .

In all cases, the values of C_{MATCH} and L_{MATCH} must be chosen from standard values. At this point, these values need now be installed on the board and measured for performance at 100 MHz. Because of board and layout parasitics, the component values from the above example had to be tuned to the final values of $C_{MATCH} = 8.9 \text{ pF}$ and $L_{MATCH} = 270 \text{ nH}$ shown in Table I.

Assuming a lossless matching network and noting conservation of power, the impedance transformation from R_S to R_{IN} (50 Ω to 900 Ω) has an associated voltage gain given by

$$Gain_{dB} = 20 \times \log \sqrt{\frac{R_{IN}}{R_S}} = 12.6 \text{ dB}$$

Because the AD8313 input responds to *voltage* and not true power, the voltage gain of the matching network will increase the effective input low-end power sensitivity by this amount. Thus, in this case, the dynamic range will be shifted downwards, that is, the 12.6 dB voltage gain will shift the 0 dBm to -65 dBm input range downwards to -12.6 dBm to -77.6 dBm. However, because of network losses this gain will not be fully realized in practice. Reference Figures 31 and 32 for an example of practical attainable voltage gains.

Table I shows recommended values for the inductor and capacitors in Figure 32 for some selected RF frequencies along with the associated theoretical voltage gain. These values for a reactive match are optimal for the board layout detailed as Figure 45. As previously discussed, a modification of the board layout will produce networks that may not perform as specified. At 2.5 GHz, a shunt inductor is sufficient to achieve match. Consequently, $C1$ and $C2$ are set sufficiently high that they appear as RF shorts.

Table I. Recommended Values for $C1$, $C2$ and L_{MATCH} in Figure 33

Freq. (MHz)	C_{MATCH} (pF)	$C1$ (pF)	$C2$ (pF)	L_{MATCH} (nH)	Voltage Gain (dB)
100	8.9	22	15	270	12.6
		9	1000	270	
900	1.5	3	3	8.2	9.0
		1.5	1000	8.2	
1900	1.5	3	3	2.2	6.2
		1.5	1000	2.2	
2500	Large	390	390	2.2	3.2

Figure 35 shows the voltage response of the 100 MHz matching network; note the high attenuation at lower frequencies typical of a high-pass network.

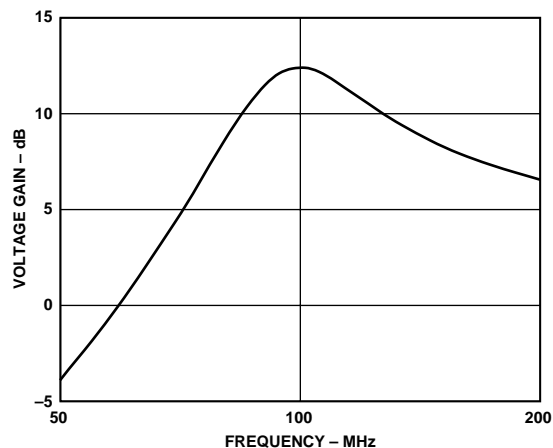


Figure 35. Voltage Response of 100 MHz Narrow-Band Matching Network

Adjusting the Log Slope

Figure 36 shows how the log slope may be adjusted to an exact value. The idea is simple: the output at pin VOUT is attenuated by the variable resistor R2 working against the internal 18 kΩ of input resistance at the VSET pin. When R2 is zero, the attenuation it introduces is zero, and thus the slope is the basic 18 mV/dB (note that this value varies with frequency, see Figure 8). When R2 is set to its maximum value of 10 kΩ, the attenuation from VOUT to VSET is the ratio 18/(18+10), and the slope is raised to $(28/18) \times 18$ mV, or 28 mV/dB. At about the midpoint, the nominal scale will be 23 mV/dB. Thus, a 70 dB input range will change the output by 70×23 mV, or 1.6 V.

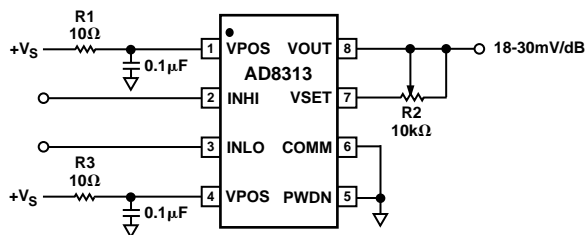


Figure 36. Adjusting the Log Slope

As already stated, the unadjusted log slope varies with frequency from 17 mV/dB to 20 mV/dB, as shown in Figure 8. By placing a resistor between VOUT and VSET, the slope can be adjusted to a convenient 20 mV/dB as shown in Figure 37. Table II shows the recommended values for this resistor R_{EXT} . Also shown are values for R_{EXT} that increase the slope to approximately 50 mV/dB. The corresponding voltage swings for a -65 dBm to 0 dBm input range are also shown in Table II.

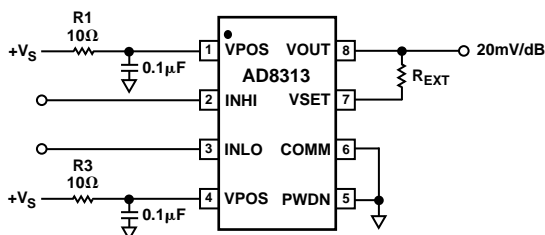


Figure 37. Adjusting the Log Slope to a Fixed Value

Table II. Values for R_{EXT} in Figure 37

Frequency MHz	R_{EXT} kΩ	Slope mV/dB	V_{OUT} Swing for Pin -65 dBm to 0 dBm - V
100	0.953	20	0.44 to 1.74
900	2.00	20	0.58 to 1.88
1900	2.55	20	0.70 to 2.00
2500	0	20	0.54 to 1.84
100	29.4	50	1.10 to 4.35
900	32.4	50.4	1.46 to 4.74
1900	33.2	49.8	1.74 to 4.98
2500	26.7	49.7	1.34 to 4.57

The value for R_{EXT} is calculated using the equation:

$$R_{EXT} = \frac{(New\ Slope - Original\ Slope)}{Original\ Slope} \times 18\ k\Omega$$

The value for the *Original Slope*, at a particular frequency, can be read from Figure 8. The resulting output swing is calculated by simply inserting the *New Slope* value and the intercept at that frequency (Figures 8 and 11) into the general equation for the AD8313's output voltage:

$$V_{OUT} = Slope (P_{IN} - Intercept)$$

Increasing Output Current

Where it is necessary to drive a more substantial load, one of two methods can be used. In Figure 38, a 1 kΩ pull-up resistor is added at the output which provides the load current necessary to drive a 1 kΩ load to +1.7 V for $V_S = 2.7$ V. The pull-up resistor will slightly lower the intercept and the slope. As a result, the transfer function of the AD8313 will be shifted upwards (intercept shifts downward).

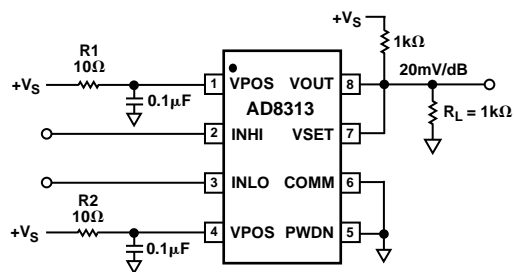


Figure 38. Increasing AD8313 Output Current Capability

In Figure 39, an emitter-follower is used to provide current gain, when a 100 Ω load can readily be driven to full-scale output. While a high β transistor such as the BC848BLT1 (min $\beta = 200$) is recommended, a 2 kΩ pull-up resistor between VOUT and +Vs can provide additional base current to the transistor.

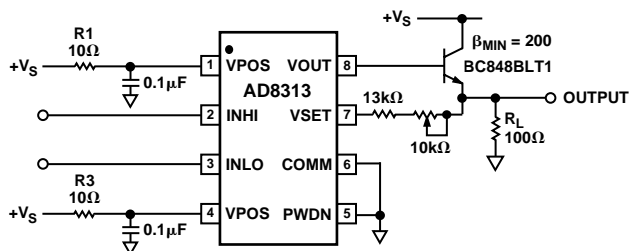


Figure 39. Output Current Drive Boost Connection

AD8313

In addition to providing current gain, the resistor/potentiometer combination between VSET and the emitter of the transistor increases the log slope to as much as 45 mV/dB, at maximum resistance. This will give an output voltage of 4 V for a 0 dBm input. If no increase in the log slope is required, VSET can be connected directly to the emitter of the transistor.

Effect of Waveform Type On Intercept

Although it is specified for input levels in dBm (dB relative to 1 mW), the AD8313 fundamentally responds to voltage and not to power. A direct consequence of this characteristic is that input signals of equal rms power but differing crest factors will produce different results at the log amp's output.

The effect of different signal waveforms is to vary the effective value of the log amp's intercept upwards or downwards. Graphically, this looks like a vertical shift in the log amp's transfer function. The device's logarithmic slope, however, is in principle not affected. For example, consider the case of the AD8313 being alternately fed from a continuous wave and a single CDMA channel of the same rms power. The AD8313's output voltage will differ by the equivalent of 3.55 dB (64 mV) over the complete dynamic range of the device (the output for a CDMA input being lower).

Table III shows the correction factors that should be applied to measure the rms signal strength of a various signal types. A continuous wave input is used as a reference. To measure the rms power of a square-wave, for example, the mV equivalent of the dB value given in the table (18 mV/dB times 3.01 dB) should be subtracted from the output voltage of the AD8313.

Table III. Shift in AD8313 Output for Signals with Differing Crest Factors

Signal Type	Correction Factor (Add to Output Reading)
CW Sine Wave	0 dB
Square Wave or DC	−3.01 dB
Triangular Wave	+0.9 dB
GSM Channel (All Time Slots On)	+0.55 dB
CDMA Channel	+3.55 dB
PDC Channel (All Time Slots On)	+0.58 dB
Gaussian Noise	+2.51 dB

EVALUATION BOARD

Schematic and Layout

Figure 44 shows the schematic of the evaluation board that was used to characterize the AD8313. Note that uninstalled components are drawn in as dashed.

This is a 3-layer board (signal, ground and power), with a Duroid dielectric (RT 5880, $h = 5$ mil, $\epsilon_R = 2.2$). FR4 can also be used, but microstrip dimensions must be recalculated because of the different dielectric constant and board height. The trace layout and silkscreen of the signal and power layers are shown in Figures 40 to 43. A detail of the PCB footprint for the μ SOIC package and the pads for the matching components are shown in Figure 45.

The vacant portions of the signal and power layers are filled out with ground plane for general noise suppression. To ensure a low impedance connection between the planes, there are multiple through-hole connections to the RF ground plane. While the ground planes on the power and signal planes are used as general purpose ground returns, any RF grounds related to the input matching network (e.g., C2) are returned directly to the RF internal ground plane.

General Operation

The board should be powered by a single supply in the range, +2.7 V to +5.5 V. The power supply to each of the VPOS pins is decoupled by a 10 Ω resistor and a 0.1 μ F capacitor.

The two signal inputs are ac-coupled using 680 pF high quality RF capacitors (C1, C2). A 53.6 Ω resistor across the differential signal inputs (INH1, INLO) combines with the internal 900 Ω input impedance to give a broadband input impedance of 50.6 Ω . This termination is not optimal from a noise perspective due to the Johnson noise of the 53.6 Ω resistor. Neither does it take account for the AD8313's reactive input impedance or of the decrease over frequency of the resistive component of the input impedance. However, it does allow evaluation of the AD8313 over its complete frequency range without having to design multiple matching networks.

For optimum performance, a narrowband match can be implemented by replacing the 53.6 Ω resistor (labeled L/R) with an RF inductor and replacing the 680 pF capacitors with appropriate values. The section on Input Matching includes a table of recommended values for selected frequencies and explains the method of calculation.

Switch 1 is used to select between power-up and power-down modes. Connecting the PWDN pin to ground enables normal operation of the AD8313. In the opposite position, the PWDN pin can either be driven externally (SMA connector labeled EXT ENABLE) to either device state or allowed to float to a disabled device state.

The evaluation board ships with the AD8313 configured to operate in RSSI measurement mode, the logarithmic output appearing on the SMA connector labeled VOUT. This mode is set by the 0 Ω resistor (R11), which shorts the VOUT and VSET pins to each other.

Varying the Logarithmic Slope

The slope of the AD8313 can be increased from its nominal value of 18 mV/dB to a maximum of 40 mV/dB by removing R11, the 0 Ω resistor, which shorts VSET to VOUT. VSET and VOUT are now connected through a 20 k Ω potentiometer.

Operating in Controller Mode

To put the AD8313 into controller mode, R7 and R11 should be removed, breaking the link between VOUT and VSET. The VSET pin can then be driven externally via the SMA connector labeled EXT VSET IN ADJ.

Increasing Output Current

To increase the output current of VOUT, set both R3 and R11 to 0 Ω and install potentiometer R4 (1 k Ω to 5 k Ω).

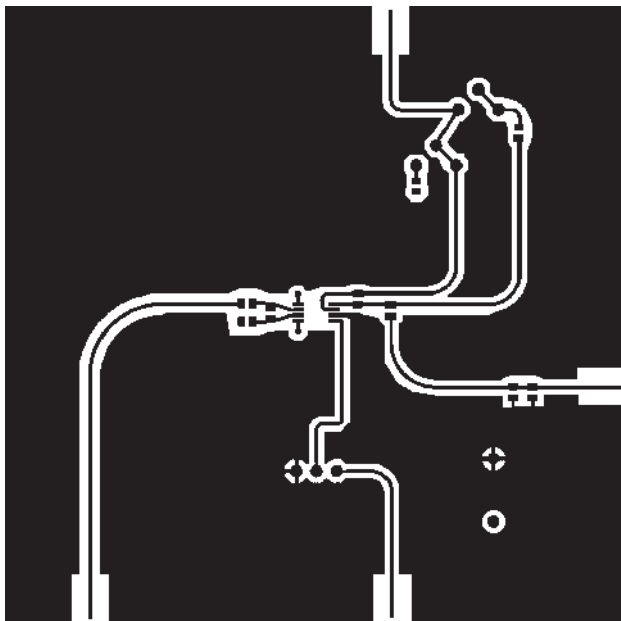


Figure 40. Layout of Signal Layer

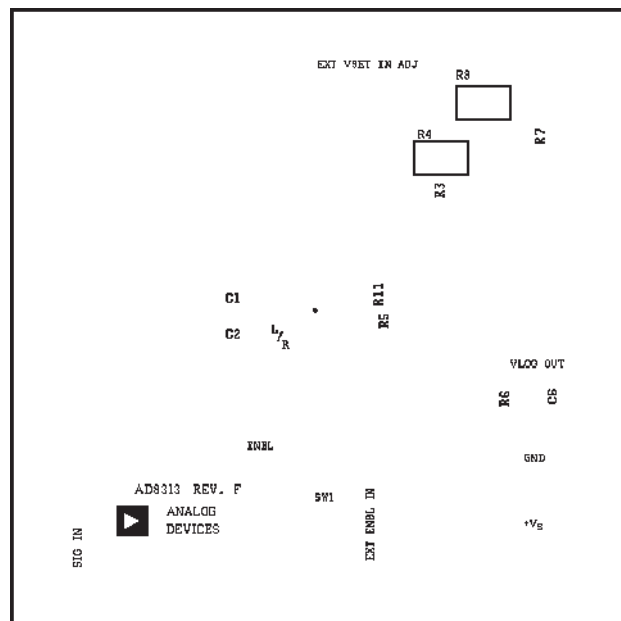


Figure 42. Signal Layer Silkscreen

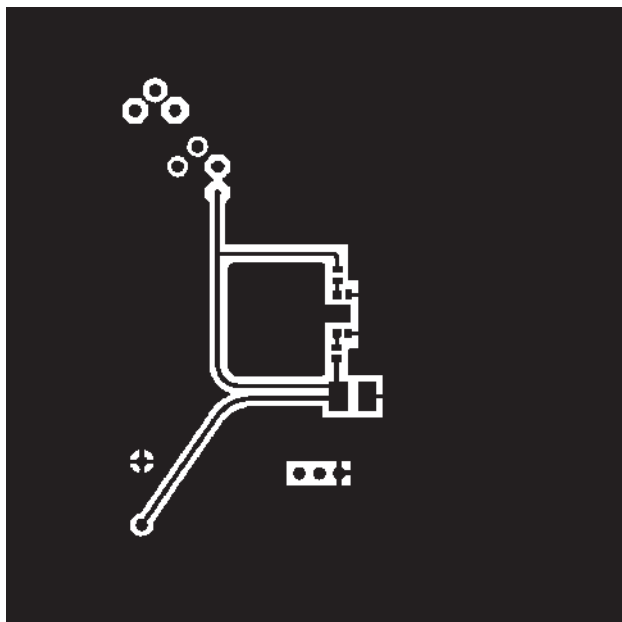


Figure 41. Layout of Power Layer

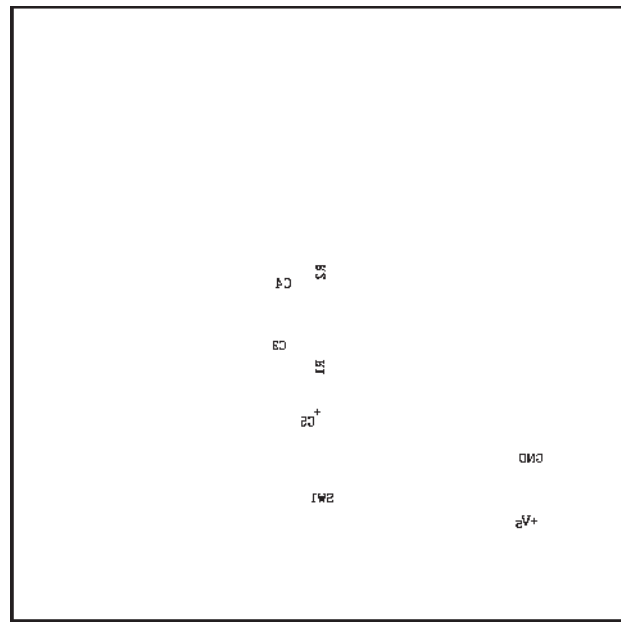


Figure 43. Power Layer Silkscreen

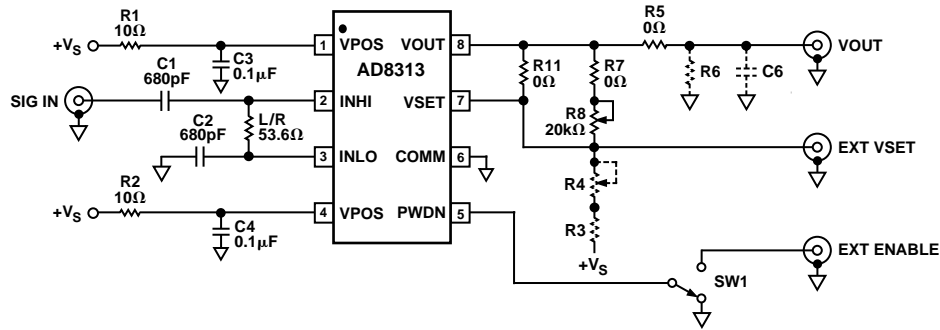


Figure 44. Evaluation Board Schematic

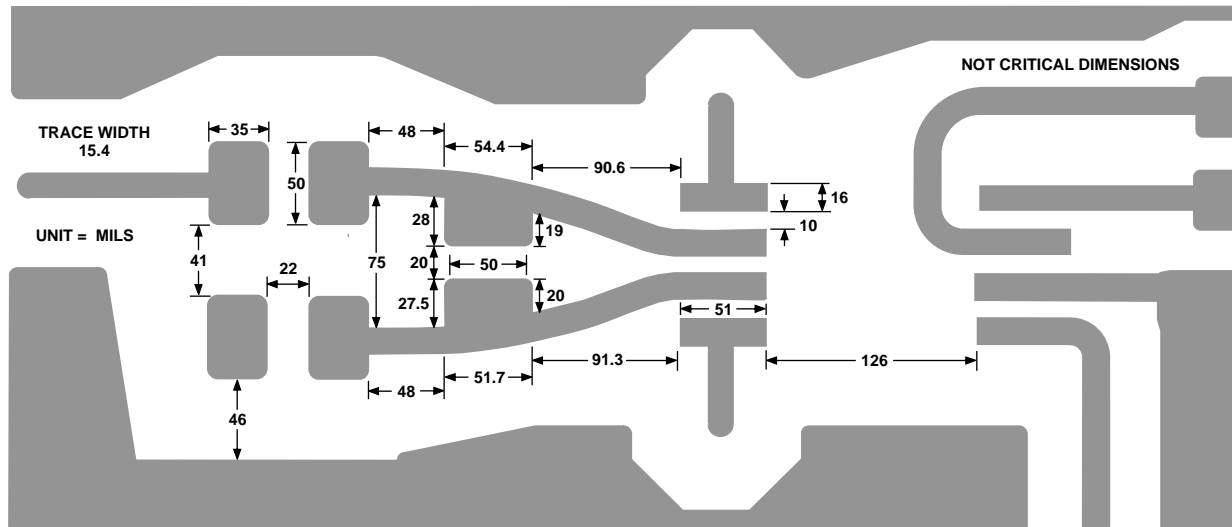


Figure 45. Detail of PCB Footprint for Package and Pads for Matching Network

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead μ SOIC Package (RM-08)

