ANALOG DEVICES

Dual Low-Power 350 MHz Voltage Feedback Amplifier

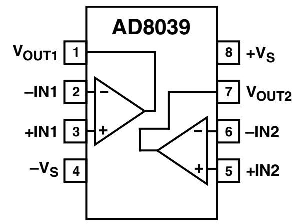
AD8039

FEATURES
Low Power
1.0 mA Supply Current/Amp
High Speed
350 MHz, –3 dB Bandwidth (G = 1)
425 V/μs Slew Rate
Low Cost
Low Noise
8 nV/$\sqrt{Hz}$ @ 100 kHz
600 fA/$\sqrt{Hz}$ @ 100 kHz
Low Input Bias Current: 300 nA Max
Low Distortion
–90 dB SFDR @ 1 MHz
–65 dB SFDR @ 5 MHz
Wide Supply Range: 3 V to 12 V
Small Packaging: SOIC-8, SOT23-8

APPLICATIONS
Battery Powered Instrumentation
Filters
A–D Driver
Level Shifting
Buffering
High-Density PC Boards
Photo Multiplier

CONNECTION DIAGRAM

SOIC-8 (R) and SOT23-8 (RT)*



PRODUCT DESCRIPTION

The AD8039 amplifier is a dual high-speed (350 MHz) voltage feedback amplifier with an exceptionally low quiescent current of 1.0 mA/amplifier typical (1.5 mA max). The AD8038 single amplifier is under development. Despite being low power and low cost the amplifier provides excellent overall performance. Additionally, it offers high slew rate of 425 V/μs and low input offset voltage of 3 mV max.

ADI's proprietary XFCB process allows low noise operation (8 nV/$\sqrt{Hz}$ and 600 fA/$\sqrt{Hz}$) at extremely low quiescent currents. Given wide supply voltage range (3 V to 12 V), wide bandwidth, and small packaging, the AD8039 amplifier is designed to work in a variety of applications where power and space are at a premium.

The AD8039 amplifier has a wide input common-mode range of 1 V from either rail and will swing within 1 V of each rail on the output. This amplifier is optimized for driving capacitive loads up to 15 pF. If driving larger capacitive loads, a small series resistor is needed to avoid excessive peaking or overshoot.

The AD8039 amplifier is the only dual low-power high-speed amplifier available in a tiny SOT23-8 package and the single AD8038 will be available in SC70. These amps are rated to work over the industrial temperature range, –40°C to +85°C.

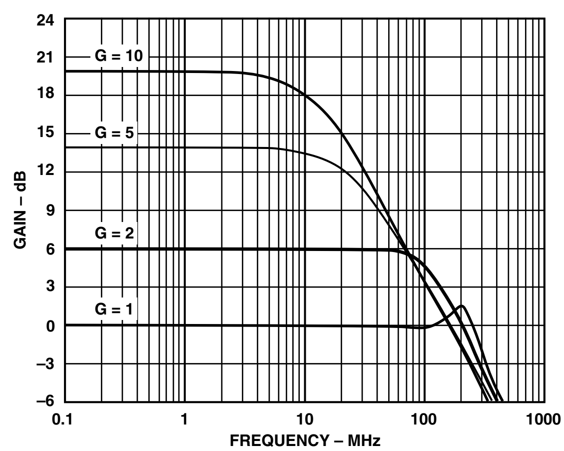


Figure 1. Small Signal Frequency Response for Various Gains, V_{OUT} = 500 mV p-p, V_S = ±5 V

*Not yet released

REV. 0

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AD8039–SPECIFICATIONS (T_A = 25°C, V_S = ±5 V, R_L= 2 kΩ, Gain = +1, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	G = 1, V_O = 0.5 V p-p	300	350		MHz
	G = 2, V_O = 0.5 V p-p		175		MHz
	G = 1, V_O = 2 V p-p		100		MHz
Bandwidth for 0.1 dB Flatness	G = 2, V_O = 0.2 V p-p		45		MHz
Slew Rate	G = 1, V_O = 2 V Step, R_L = 2 kΩ	400	425		V/µs
Overdrive Recovery Time	G = 2, 1 V Overdrive		50		ns
Settling Time to 0.1%	G = 2, V_O = 2 V Step		20		ns
NOISE/HARMONIC PERFORMANCE					
SFDR					
Second Harmonic	f_C = 1 MHz, V_O = 2 V p-p, R_L = 2 kΩ		–90		dBc
Third Harmonic	f_C = 1 MHz, V_O = 2 V p-p, R_L = 2 kΩ		–92		dBc
Second Harmonic	f_C = 5 MHz, V_O = 2 V p-p, R_L = 2 kΩ		–65		dBc
Third Harmonic	f_C = 5 MHz, V_O = 2 V p-p, R_L = 2 kΩ		–70		dBc
Crosstalk, Output-to-Output	f = 5 MHz, G = 2		–70		dB
Input Voltage Noise	f = 100 kHz		8		$nV/\sqrt{Hz}$
Input Current Noise	f = 100 kHz		600		$fA/\sqrt{Hz}$
DC PERFORMANCE					
Input Offset Voltage			0.5	3	mV
Input Offset Voltage Drift			4.5		µV/°C
Input Bias Current			150	300	nA
Input Bias Current Drift			3		nA/°C
Input Offset Current			25		±nA
Open-Loop Gain	V_O = ±2.5 V		70		dB
INPUT CHARACTERISTICS					
Input Resistance			10		MΩ
Input Capacitance			2		pF
Input Common-Mode Voltage Range	R_L = 1 kΩ		±4		V
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V	61	67		dB
OUTPUT CHARACTERISTICS					
DC Output Voltage Swing	R_L = 2 kΩ, Saturated Output		±4		V
Capacitive Load Drive	30% Overshoot, G = +2		20		pF
POWER SUPPLY					
Operating Range		3.0		12	V
Quiescent Current Per Amplifier			1.0	1.5	mA
Power Supply Rejection Ratio	– Supply	–71	–77		dB
	+ Supply	–64	–70		dB

Specifications subject to change without notice.

SPECIFICATIONS (T_A = 25°C, V_S = 5 V, R_L = 2 kΩ to V_S/2, Gain = +1, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	G = 1, V_O = 0.2 V p-p	275	300		MHz
	G = 2, V_O = 0.2 V p-p		150		MHz
	G = 1, V_O = 2 V p-p		30		MHz
Bandwidth for 0.1 dB Flatness	G = 2, V_O = 0.2 V p-p		45		MHz
Slew Rate	G = 1, V_O = 2 V Step, R_L = 2 kΩ	340	365		V/µs
Overdrive Recovery Time	G = 2, 1 V Overdrive		50		ns
Settling Time to 0.1%	G = 2, V_O = 2 V Step		20		ns
NOISE/HARMONIC PERFORMANCE					
SFDR					
Second Harmonic	f_C = 1 MHz, V_O = 2 V p-p, R_L = 2 kΩ		–82		dBc
Third Harmonic	f_C = 1 MHz, V_O = 2 V p-p, R_L = 2 kΩ		–79		dBc
Second Harmonic	f_C = 5 MHz, V_O = 2 V p-p, R_L = 2 kΩ		–60		dBc
Third Harmonic	f_C = 5 MHz, V_O = 2 V p-p, R_L = 2 kΩ		–67		dBc
Crosstalk, Output-to-Output	f = 5 MHz, G = 2		–70		dB
Input Voltage Noise	f = 100 kHz		8		nV/√Hz
Input Current Noise	f = 100 kHz		600		fA/√Hz
DC PERFORMANCE					
Input Offset Voltage			0.8	3	mV
Input Offset Voltage Drift			3		µV/°C
Input Bias Current			150	300	nA
Input Bias Current Drift			3		nA/°C
Input Offset Current			30		±nA
Open-Loop Gain	V_O = ±2.5 V		70		dB
INPUT CHARACTERISTICS					
Input Resistance			10		MΩ
Input Capacitance			2		pF
Input Common-Mode Voltage Range	R_L = 1 kΩ		1.0–4.0		V
Common-Mode Rejection Ratio	V_{CM} = ±1 V	59	65		dB
OUTPUT CHARACTERISTICS					
DC Output Voltage Swing	R_L = 2 kΩ, Saturated Output		0.9–4.1		V
Capacitive Load Drive	30% Overshoot		20		pF
POWER SUPPLY					
Operating Range		3		12	V
Quiescent Current Per Amplifier			0.9	1.5	mA
Power Supply Rejection Ratio		–65	–71		dB

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . 12.6 V
Power Dissipation . . . . See Figure 2
Common-Mode Input Voltage . . . . $\pm V_S$
Differential Input Voltage . . . . ±4 V
Storage Temperature . . . . –65°C to +125°C
Operating Temperature Range . . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the AD8039 package is limited by the associated rise in junction temperature (T_J) on the die. The plastic encapsulating the die will locally reach the junction temperature. At approximately 150°C, which is the glass transition temperature, the plastic will change its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8039. Exceeding a junction temperature of 175°C for an extended period of time can result in changes in the silicon devices, potentially causing failure.

The still-air thermal properties of the package and PCB (θ_{JA}), ambient temperature (T_A), and the total power dissipated in the package (P_D) determine the junction temperature of the die. The junction temperature can be calculated as follows:

$$T_J = T_A + \left(P_D \times \theta_{JA}\right)$$

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) multiplied by the quiescent current (I_S). Assuming the load (R_L) is referenced to midsupply, then the total drive power is $V_S/2 \times I_{OUT,}$ some of which is dissipated in the package and some in the load ($V_{OUT} \times I_{OUT}$). The difference between the total drive power and the load power is the drive power dissipated in the package.

P_D = quiescent power + (total drive power – load power)

$$P_D = \left[V_S \times I_S\right] + \left[\left(V_S/2\right) \times \left(V_{OUT}/R_L\right)\right] - \left[V_{OUT}{}^2/R_L\right]$$

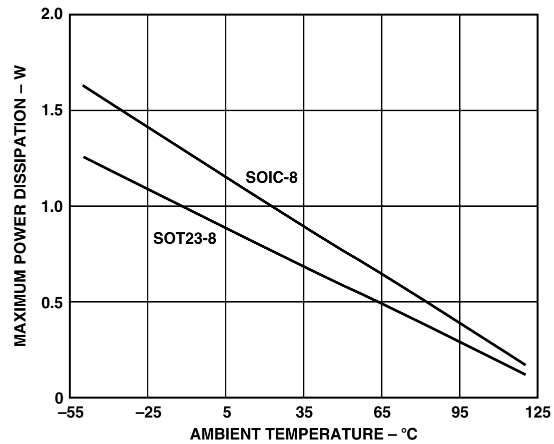


Figure 2. Maximum Power Dissipation vs. Temperature for a Four-Layer Board

RMS output voltages should be considered. If R_L is referenced to V_{S-} as in single-supply operation, then the total drive power is V_S ¥ I_{OUT}.

If the RMS signal levels are indeterminate, then consider the worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply:

$$P_D = \left(V_S \times I_S\right) + \left(V_S/4\right)^2/R_L$$

In single supply operation with R_L referenced to V_{S-}, worst case is $V_{OUT} = V_S/2$.

Airflow will increase heat dissipation effectively reducing θ_{JA}. Also, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes will reduce the θ_{JA}. Care must be taken to minimize parasitic capacitances at the input leads of high-speed op amp as discussed in the board layout section.

Figure 2 shows the maximum safe power dissipation in the package versus ambient temperature for the SO-8 (125°C/W) and SOT23-8 (160°C/W) package on a JEDEC standard four-layer board. θ_{JA} values are approximations.

OUTPUT SHORT CIRCUIT

Shorting the output to ground or drawing excessive current from the AD8039 will likely cause a catastrophic failure.

ORDERING GUIDE

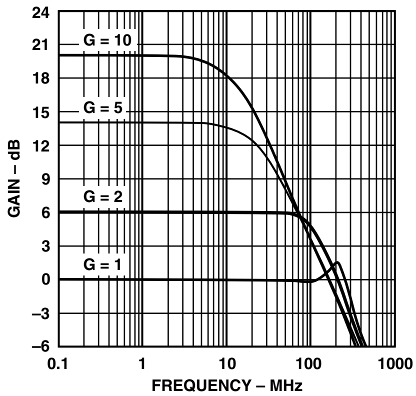
Model	Temperature Range	Package Description	Package Outline	Branding Information
AD8039AR	–40°C to +85°C	8-Lead SOIC	SO-8	
AD8039AR-REEL	–40°C to +85°C	8-Lead SOIC	SO-8	
AD8039AR-REEL7	–40°C to +85°C	8-Lead SOIC	SO-8	
AD8039ART-REEL*	–40°C to +85°C	8-Lead SOT23	RT-8	HYA
AD8039ART-REEL7*	–40°C to +85°C	8-Lead SOT23	RT-8	HYA
AD8038AR*	–40°C to +85°C	8-Lead SOIC	SO-8	
AD8038AKS*	–40°C to +85°C	5-Lead SC70	KS-5	HUA

*Under development

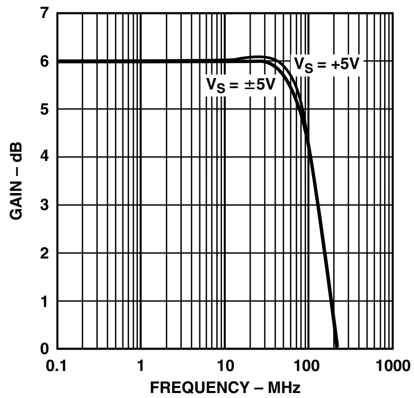
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8039 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

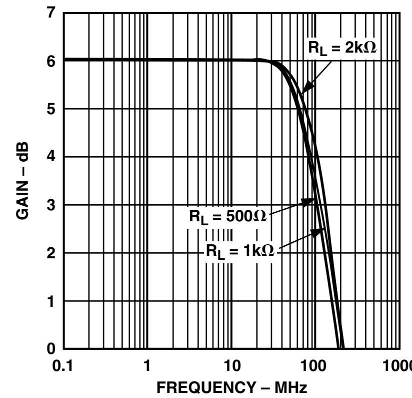
(Default Conditions: ±5 V, C_L = 5 pF, G = 2, R_G = R_F = 1 kΩ, R_L = 2 kΩ, V_O = 2 V p-p, Frequency = 1 MHz, T_A = 25°C.)



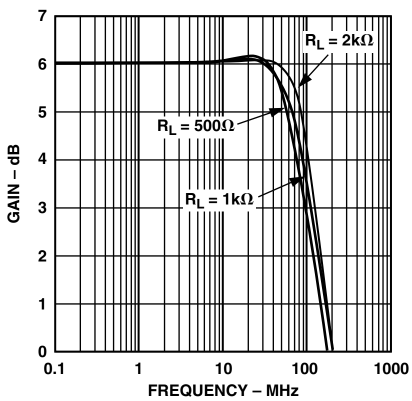
TPC 1. Small Signal Frequency Response for Various Gains, V_{OUT} = 500 mV p-p



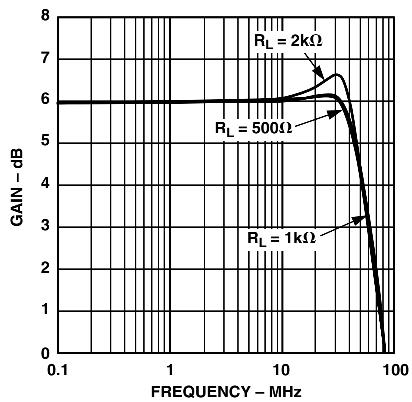
TPC 2. Small Signal Frequency Response for Various Supplies, V_{OUT} = 500 mV p-p



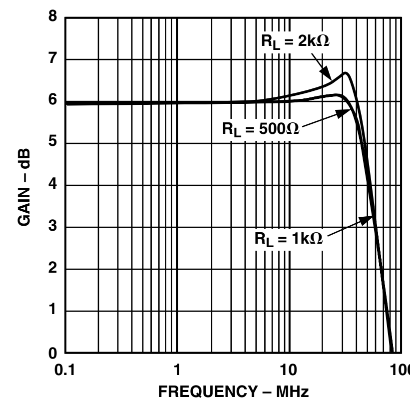
TPC 3. Small Signal Frequency Response for Various R_{LOAD}, V_S = ±5 V, V_{OUT} = 500 mV p-p



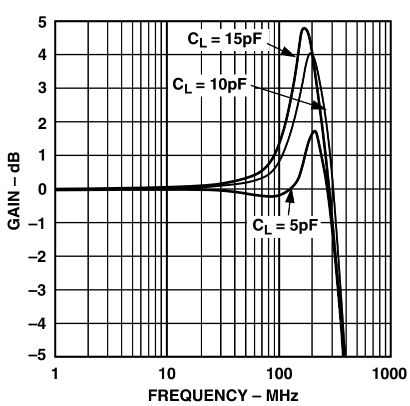
TPC 4. Small Signal Frequency Response for Various R_{LOAD}, V_S = 5 V, V_{OUT} = 500 mV p-p



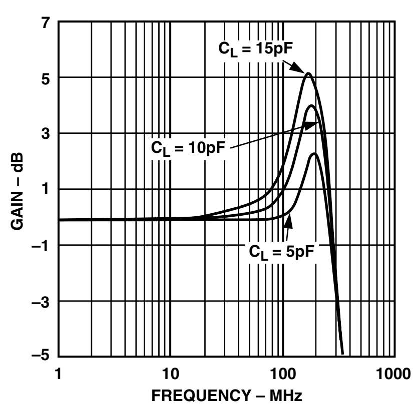
TPC 5. Large Signal Frequency Response for Various R_{LOAD}, V_{OUT} = 3 V p-p, V_S = 5 V



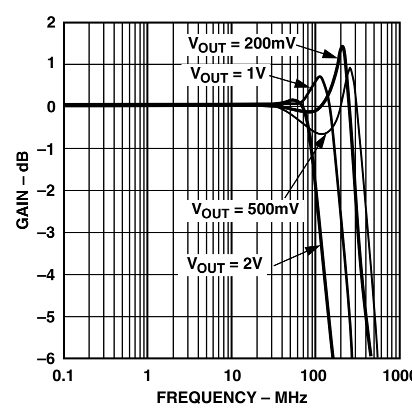
TPC 6. Large Signal Frequency Response for Various R_{LOAD}, V_{OUT} = 4 V p-p, V_S = ±5 V



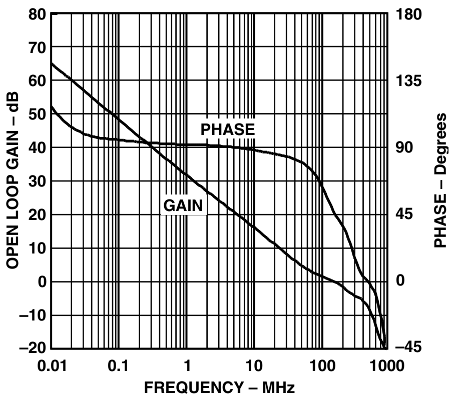
TPC 7. Small Signal Frequency Response for Various C-Load, V_{OUT} = 500 mV, V_S = ±5 V, G = 1



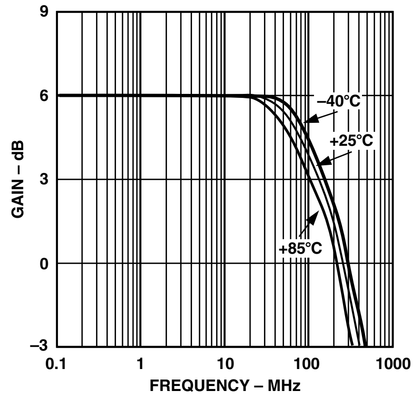
TPC 8. Small Signal Frequency Response for Various C-Load, V_{OUT} = 500 mV, V_S = 5 V, G = 1



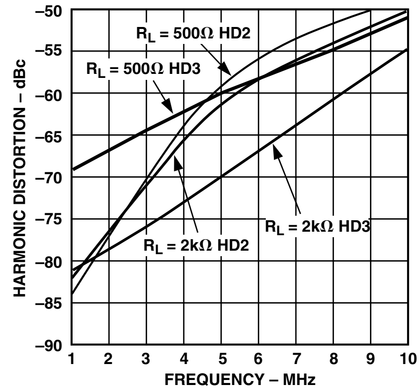
TPC 9. Frequency Response for Various Output Voltage Levels



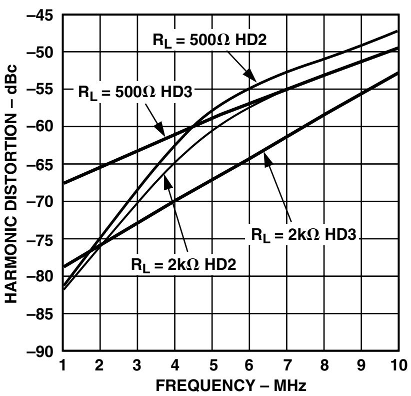
TPC 10. Open-Loop Gain and Phase, $V_S = \pm5$ V



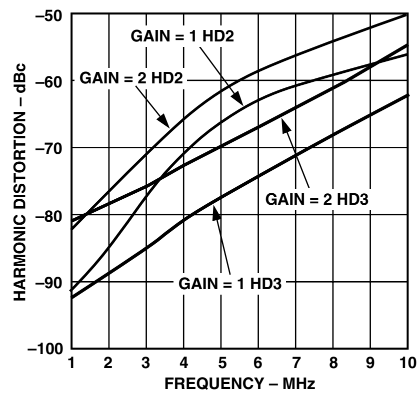
TPC 11. Frequency Response vs. Temperature, Gain = +2



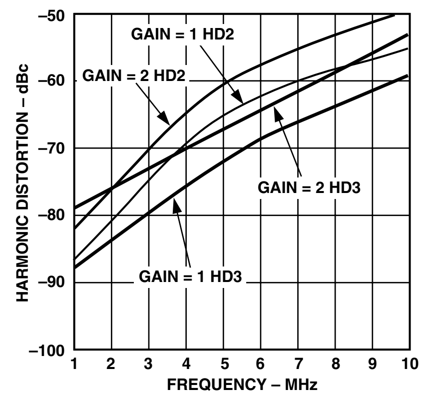
TPC 12. Harmonic Distortion vs. Frequency for Various Loads, $V_S = \pm5$ V, 2 V p-p, G = +2



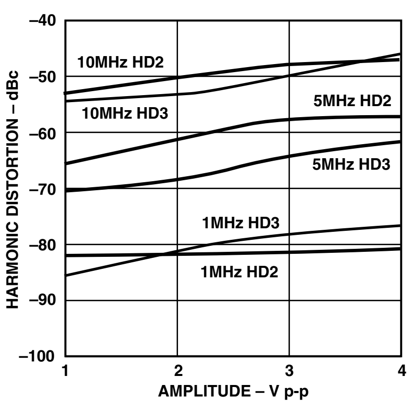
TPC 13. Harmonic Distortion vs. Frequency for Various Loads, $V_S = 5$ V, 2 V p-p, G = +2



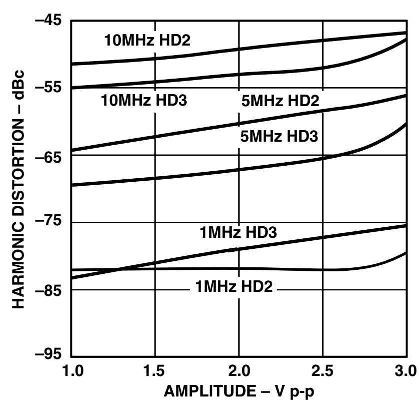
TPC 14. Harmonic Distortion vs. Frequency for Various Gains, $V_S = \pm5$ V, 2 V p-p



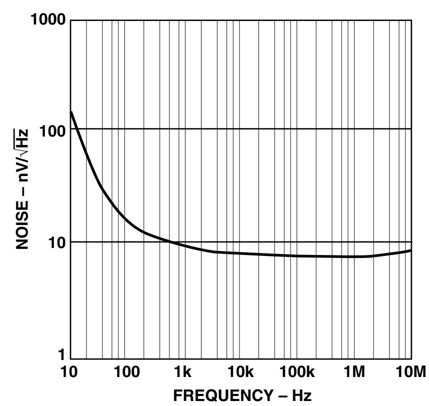
TPC 15. Harmonic Distortion vs. Frequency for Various Gains, $V_S = 5$ V, 2 V p-p



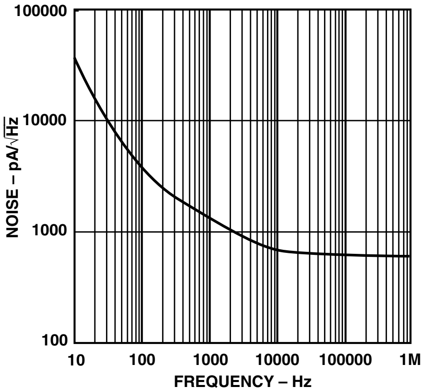
TPC 16. Harmonic Distortion vs. V_{OUT} Amplitude for Various Frequencies, $V_S = \pm5$ V, G = +2



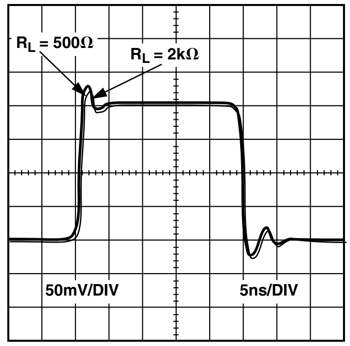
TPC 17. Harmonic Distortion vs. Amplitude for Various Frequencies, $V_S = 5$ V, G = +2



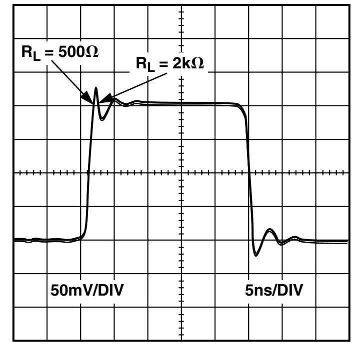
TPC 18. Input Voltage Noise vs. Frequency



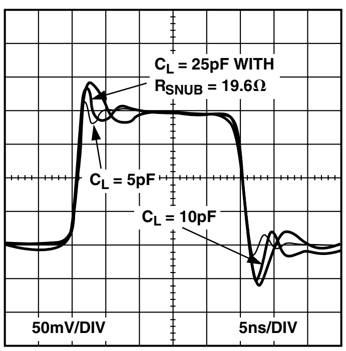
TPC 19. Input Current Noise vs. Frequency



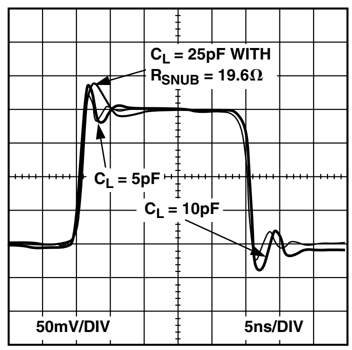
TPC 20. Small Signal Transient Response for Various R-Load, V_S = 5 V



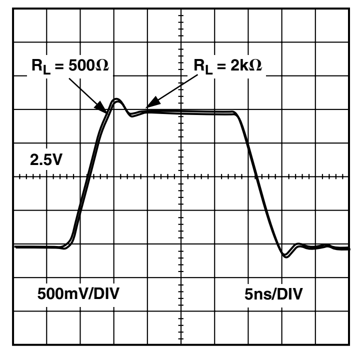
TPC 21. Small Signal Transient Response for Various R-Load, V_S = ±5 V



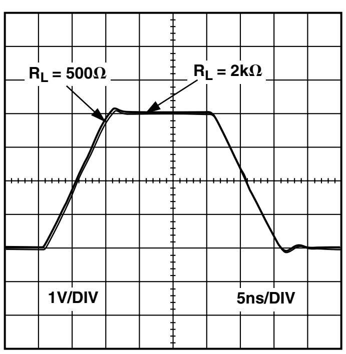
TPC 22. Small Signal Transient Response for Various Capacitive Loads, V_S = 5 V



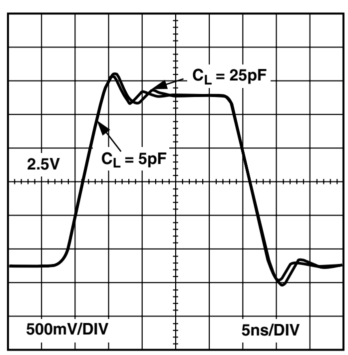
TPC 23. Small Signal Transient Response for Various Capacitive Loads, V_S = ±5 V



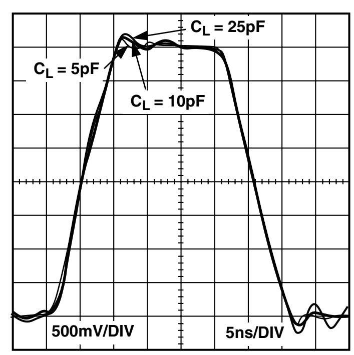
TPC 24. Large Signal Transient Response for Various R-Load, V_S = 5 V



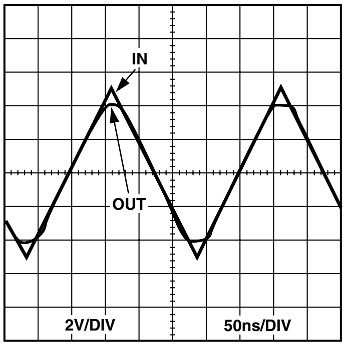
TPC 25. Large Signal Transient Response for Various R-Load, V_S = ±5 V



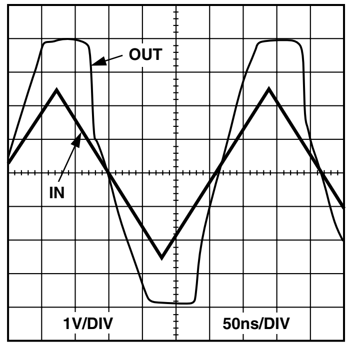
TPC 26. Large Signal Transient Response for Various Capacitive Loads, V_S = 5 V



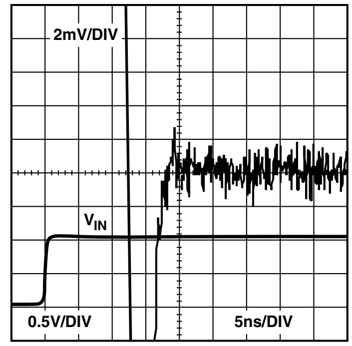
TPC 27. Large Signal Transient Response for Various Capacitive Loads, V_S = ±5 V



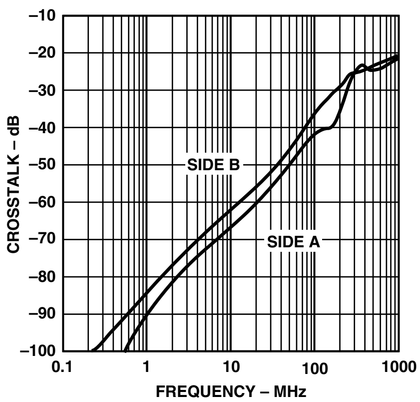
TPC 28. Input Overdrive Recovery, Gain = +1



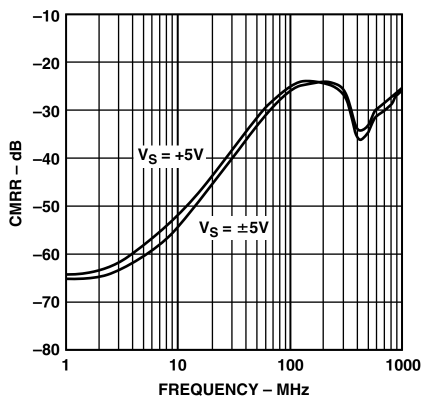
TPC 29. Output Overdrive Recovery, Gain = +2



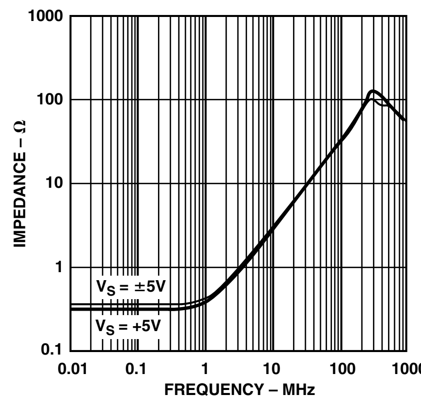
TPC 30. 0.1% Settling Time V_{OUT} = 2 V p-p



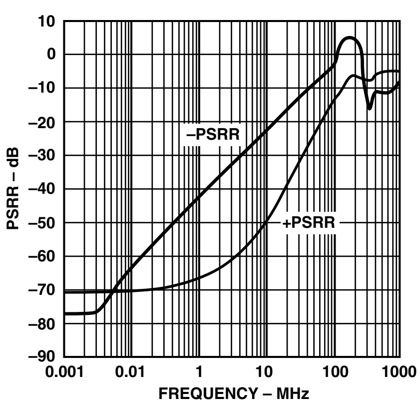
TPC 31. Crosstalk, V_{IN} = 1 V p-p, Gain = +1



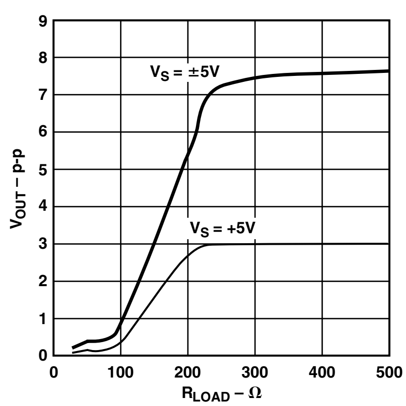
TPC 32. CMRR vs. Frequency, V_{IN} = 1 V p-p



TPC 33. Output Impedance vs. Frequency



TPC 34. PSRR vs. Frequency



TPC 35. Output Swing vs. Load Resistance

LAYOUT, GROUNDING, AND BYPASSING CONSIDERATIONS

Power Supply Bypassing

Power supply pins are actually inputs and care must be taken so that a noise-free stable dc voltage is applied. The purpose of bypass capacitors is to create low impedances from the supply to ground at all frequencies, thereby shunting or filtering a majority of the noise.

Decoupling schemes are designed to minimize the bypassing impedance at all frequencies with a parallel combination of capacitors. 0.01 µF or 0.001 µF (X7R, or NPO) chip capacitors are critical and should be as close as possible to the amplifier package. Larger chip capacitors such as the 0.1 µF capacitor can be shared among a few closely spaced active components in the same signal path. A 10 µF tantalum capacitor is less critical for high-frequency bypassing and, in most cases, only one per board is needed at the supply inputs.

Grounding

A ground plane layer is important in densely packed PC boards to spread the current minimizing parasitic inductances. However, an understanding of where the current flows in a circuit is critical to implementing effective high-speed circuit design. The length of the current path is directly proportional to the magnitude of parasitic inductances and thus the high-frequency impedance of the path. High-speed currents in an inductive ground return will create an unwanted voltage, noise.

The length of the high-frequency bypass capacitor leads are most critical. A parasitic inductance in the bypass grounding will work against the low impedance created by the bypass capacitor. Place the ground leads of the bypass capacitors at the same physical location. Because load currents flow from the supplies as well, the ground for the load impedance should be at the same physical location as the bypass capacitor grounds. For the larger value capacitors, which are intended to be effective at lower frequencies, the current return path distance is less critical.

Input Capacitance

Along with bypassing and ground, high-speed amplifiers can be sensitive to parasitic capacitance between the inputs and ground. A few pF of capacitance will reduce the input impedance at high frequencies in turn increasing the amplifiers gain, causing peaking of the frequency response or even oscillations if severe enough. It is recommended that the external passive components that are connected to the input pins be placed as close as possible to the inputs to avoid parasitic capacitance. The ground and power planes must be kept at a distance of at least 0.05 mm from the input pins on all layers of the board.

Output Capacitance

To a lesser extent, parasitic capacitances on the output can cause peaking of the frequency response. There are two methods to effectively minimize this effect.

1. Put a small value resistor in series with the output to isolate the load capacitor from the amp's output stage. (See TPCs 7, 8, 22, and 23)
2. Increase the phase margin with higher noise gains or add a pole with a parallel resistor and capacitor from –IN to the output.

Input-To-Output Coupling

The input and output signal traces should not be parallel to minimize capacitive coupling between the inputs and output avoiding any positive feedback through.

APPLICATIONS

Low-Power ADC Driver

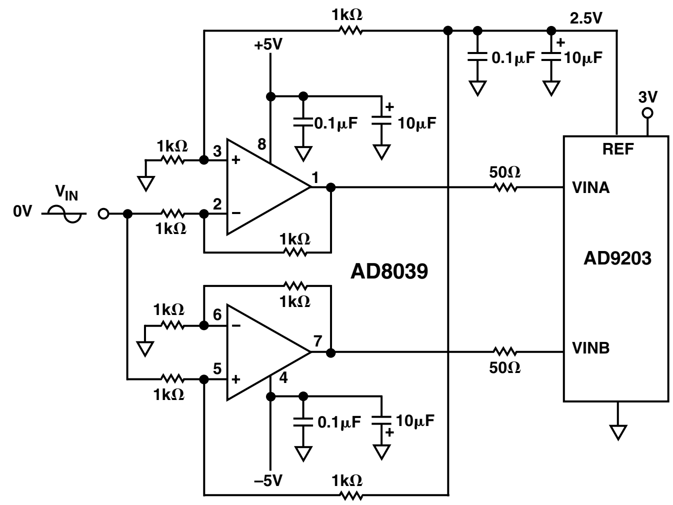


Figure 3. Schematic to Drive AD9203 with the AD8039

Differential A–D Driver

The AD9203 is a low power, 125 mW on a 5 V supply, 40 MSPS 10-bit converter. This represents a breakthrough in power/speed for ADCs. As such, the low-power high-performance AD8039 is an appropriate choice of amplifier to drive it.

In low-supply voltage applications, differential analog inputs are needed to increase the dynamic range of the ADC inputs. Differential driving can also reduce second and other even-order distortion products. The AD8039 can be used to make a dc-coupled, single-ended-to-differential driver for one of these ADCs. Figure 3 is a schematic of such a circuit for driving an AD9203, a 10-bit, 40 MSPS ADC.

The AD9203 works best when the common-mode voltage at the input is at the midsupply or 2.5 V. The output stage design of the AD8039 makes it ideal for driving these types of ADCs.

In this circuit, one of the op amps is configured in the inverting mode, while the other is in the noninverting mode. However, to provide better bandwidth matching, each op amp is configured for a noise gain of +2. The inverting op amp is configured for a gain of –1, while the noninverting op amp is configured for a gain of +2. Each of these has very similar ac response. The input signal to the noninverting op amp is divided by two to normalize its voltage level and make it equal to the inverting output.

The outputs of the op amps are centered at 2.5 V, which is the midsupply level of the ADC. This is accomplished by first taking the 2.5 V reference output of the ADC and dividing it by two with a pair of 1 kΩ resistors. The resulting 1.25 V is applied to each op amp's positive input. This voltage is then multiplied by the gain of 2 of the op amps to provide a 2.5 V level at each output.

Low-Power Active Video Filter

Some composite video signals derived from a digital source contain clock feedthrough that can limit picture quality. Active filters made from op amps can be used in this application, but they will consume 25 mW to 30 mW for each channel. In power sensitive applications this can be too much, requiring the use of passive filters that can create impedance matching problems when driving any significant load.

The AD8039 can be used to make an effective low-pass active filter that consumes one fifth of the power. Figure 4 shows a circuit that uses an AD8039 to create a single ±2.5 V supply, three-pole Sallen-Key filter. This circuit uses a single RC pole in front of a standard two-pole active section.

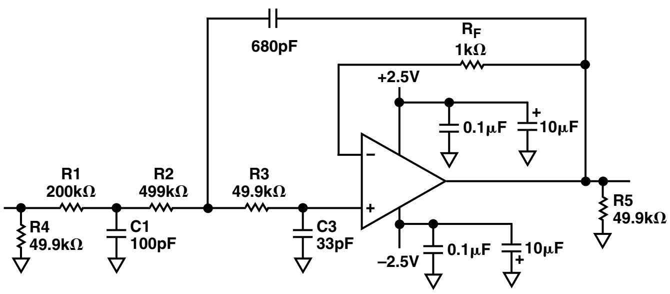


Figure 4. Low-Pass Filter for Video

Figure 5 shows the frequency response of this filter. The response is down 3 dB at 6 MHz, so it passes the video band with little attenuation. The rejection at 27 MHz is 45 dB, which provides more than a factor of 100 in suppression of the clock components at this frequency.

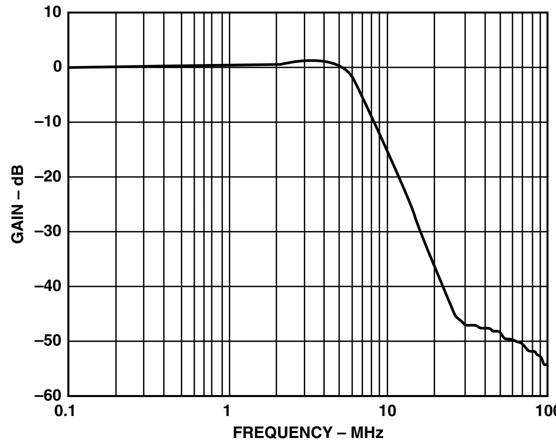
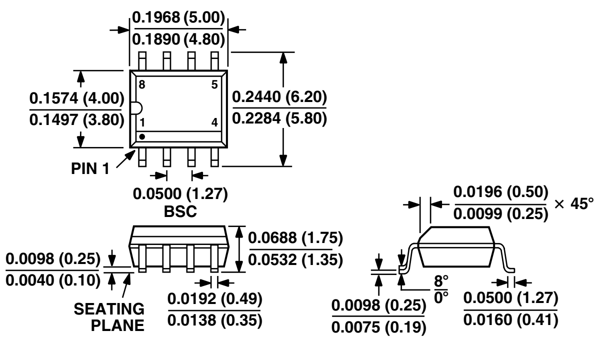


Figure 5. Video Filter Response

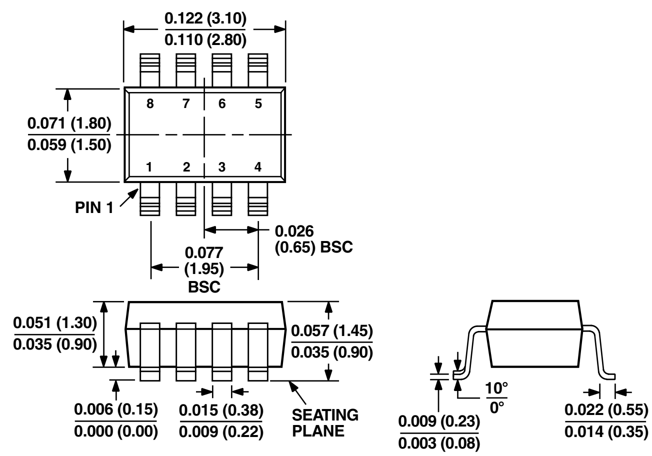
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

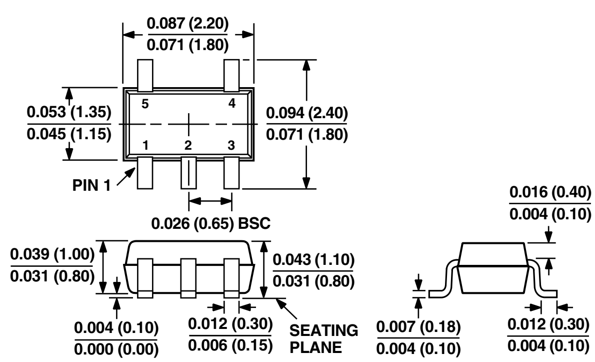
8-Lead Plastic SOIC (R-8)



8-Lead Plastic Surface Mount (SOT23-8)



5-Lead SC70 (KS-5)



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