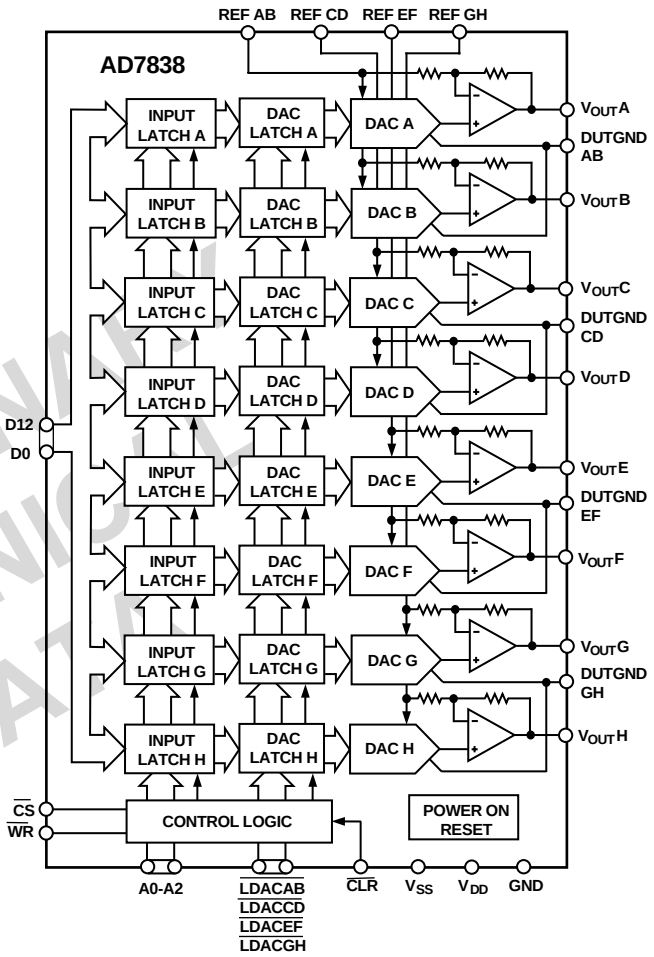
Octal, 13-Bit Voltage-Output DAC with Parallel Interface

Preliminary Technical Data — AD7838

FEATURES
Eight 13-Bit DACs in One Package
Full 13-Bit Performance without Adjustments
Buffered Voltage Outputs
Offset Adjust for Each DAC Pair
±5 V Supply Operation
Unipolar or Bipolar Output Swing to ±4.5 V
Output Settling to 1/2 LSB in 5 μs
Double Buffered Digital Inputs
Microprocessor and TTL/CMOS Compatible
Asynchronous Load Facility using LDAC Inputs
Clear Function to User-Defined Voltage
Power-On-Reset, Outputs Power Up at DUTGND
44-Lead PLCC and PQFP Packages
Pin Compatible with MAX547

APPLICATIONS
Process Control
Automatic Test Equipment
General Purpose Instrumentation
Digital Offset and Gain Adjustment
Arbitrary Function Generators
Avionics Equipment

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7838 contains eight 13-bit, voltage-output digital-to-analog converters (DACs). The output voltages are provided through on-chip precision output amplifiers into which an external offset voltage can be inserted via the DUTGND pins. The AD7838 operates from a ±5 V ± 5% supply. Bipolar output voltages with up to ±4.5 V voltage swing can be achieved with no external components. The AD7838 has four separate reference inputs; each is connected to two DACs, providing different scale output voltages for every DAC pair.

The AD7838 features double-buffered interface logic with a 13-bit parallel data bus. Each DAC has an input latch and a DAC latch. Data in the DAC latch sets the output voltage. The eight input latches are addressed with three address lines. Data is loaded to the input latch with a single write instruction. An asynchronous $\overline{\text{LDAC}}$ input transfers data from the input latch to the DAC latch. The four $\overline{\text{LDAC}}$ inputs each control two DACs, and all DAC latches can be updated simultaneously by asserting all $\overline{\text{LDAC}}$ pins. An asynchronous clear input resets the output of all eight DACs to the relevant DUTGND. Asserting $\overline{\text{CLR}}$ resets both the DAC and the input latch to bipolar zero (1000 Hex). On power-up, reset circuitry performs the same function as $\overline{\text{CLR}}$. All logic inputs are TTL/CMOS compatible.

The AD7838 is available in 44-lead PLCC and PQFP packages.

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AD7838–PRELIMINARY SPECIFICATIONS

(V_{DD} = +5 V; V_{SS} = –5 V; REFXX = 4.096V, DUTGNDXX = GND = 0 V; R_L =10 kV and C_L = 50 pF to GND, T_A[1] = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +258C.)

Parameter	B Version	Units	Test Conditions/Comments
ACCURACY			
Resolution	13	Bits	
Relative Accuracy	±2	LSB max	Typically ±0.5 LSB
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic Over Temperature
Bipolar Zero-Code Error	±20	LSB max	Typically ±5 LSB
Gain Error	±8	LSB max	Typically ±1 LSB
V_{DD} Power Supply Rejection[2]	±0.0025	%/% max	$\Delta Gain/\Delta V_{DD}$
V_{SS} Power Supply Rejection[2]	±0.0025	%/% max	$\Delta Gain/\Delta V_{SS}$
Load Regulation	0.3	LSB typ	R_L = Unloaded to 10 kΩ
REFERENCE INPUTS[3, 4]			
Input Range	DUTGND	V min	
	V_{DD}	V max	
Input Impedance	5	kΩ min	
OUTPUT CHARACTERISTICS			
Maximum Output Voltage	V_{DD} – 0.5	V max	
Minimum Output Voltage	V_{SS} + 0.5	V min	
DYNAMIC PERFORMANCE			
Voltage Output Slew Rate	3	V/µs typ	
Output Settling Time	5	µs typ	Settling to 0.5 LSB of Full Scale[5]
Digital Feedthrough	5	nV-s typ	
Digital Crosstalk	5	nV-s typ	
DIGITAL INPUTS			
V_{INH}, Input High Voltage	2.4	V min	
V_{INL}, Input Low Voltage	0.8	V max	
I_{INH}, Input Current	±1	µA max	V_{IN} = 0 V or V_{DD}
C_{IN}, Input Capacitance[6]	10	pF max	
POWER REQUIREMENTS			
V_{DD}	5	V nom	±5% for Specified Performance
V_{SS}	–5	V nom	±5% for Specified Performance
I_{DD}	44	mA max	Typically 14 mA
I_{SS}	40	mA max	Typically 11 mA

NOTES

[1]Temperature Range for B Version: –40°C to +85°C.

[2]PSRR is tested by changing the respective supply voltage by ±5%.

[3]For best performance, REFxx should be greater than DUTGNDxx by 2 V and less than V_{DD} – 0.6 V. The device operates with reference inputs outside this range, but performance may degrade.

[4]Reference input resistance is code dependent.

[5]Typical settling time with 1000 pF capacitive load is 10 µs.

[6]Guaranteed by design, not production tested.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = +5 V; V_{SS} = –5 V; DUTGND = GND = 0 V, REFxx = 4.096 V)

Parameter	Limit at T_{MIN}, T_{MAX}	Units	Description
t_1	10	ns min	Address Valid to $\overline{WR}$ Setup Time
t_2	0	ns min	Address Valid to $\overline{WR}$ Hold Time
t_3	50	ns min	$\overline{CS}$ Pulse Width
t_4	50	ns min	$\overline{WR}$ Pulse Width
t_5	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_6	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_7	50	ns min	Data Valid to $\overline{WR}$ Setup Time
t_8	0	ns min	Data Valid to $\overline{WR}$ Hold Time
t_9	5	µs typ	Output Settling Time
t_{10}	100	ns min	$\overline{CLR}$ Pulse Width
t_{11}	50	ns min	$\overline{LDAC}$ Pulse Width

NOTES

[1]All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V. Timing applies for all grades of the part.

[2]Rise and fall times should be no longer than 50 ns.

Specifications subject to change without notice.

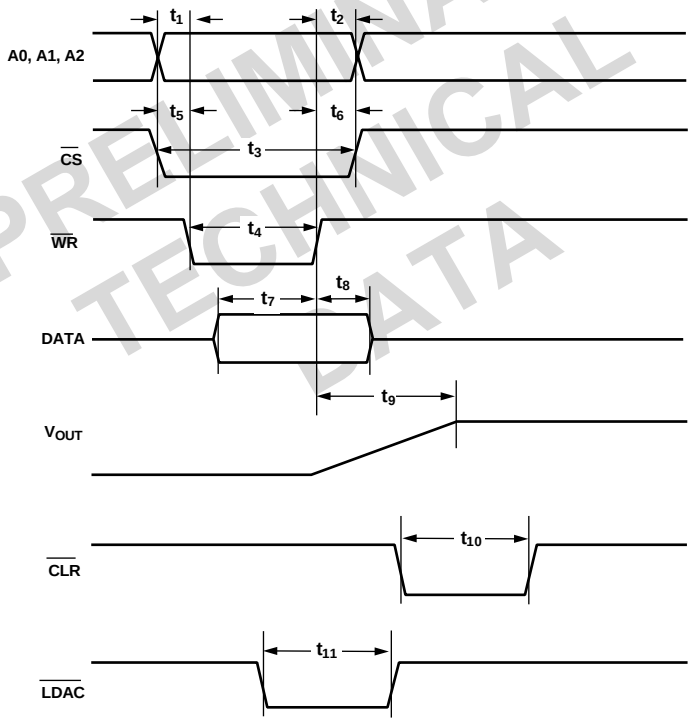


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = +25°C unless otherwise noted)

V_{DD} to GND ..... –0.3 V to +6 V
V_{SS} to GND ..... +0.3 V to –6 V
Digital Inputs to GND ..... –0.3 V to V_{DD} +0.3 V
REFxx ..... DUTGND – 0.3 to V_{DD} +0.3
DUTGNDxx ..... V_{SS} – 0.3 to V_{DD} +0.3
V_{OUT} ..... V_{DD} to V_{SS}
Max Current Into REFxx Pin ..... ±10 mA
Max Current Into Any Other Signal Pin ..... ±50 mA
Operating Temperature Range
  Industrial (B Version) ..... –40°C to +85°C
  Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
PLCC Package, Power Dissipation ..... TBD mW
  θ_{JA} Thermal Impedance ..... 48°C/W
PQFP Package, Power Dissipation ..... TBD mW
  θ_{JA} Thermal Impedance ..... 95°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) ..... +215°C
    Infrared (15 sec) ..... +220°C

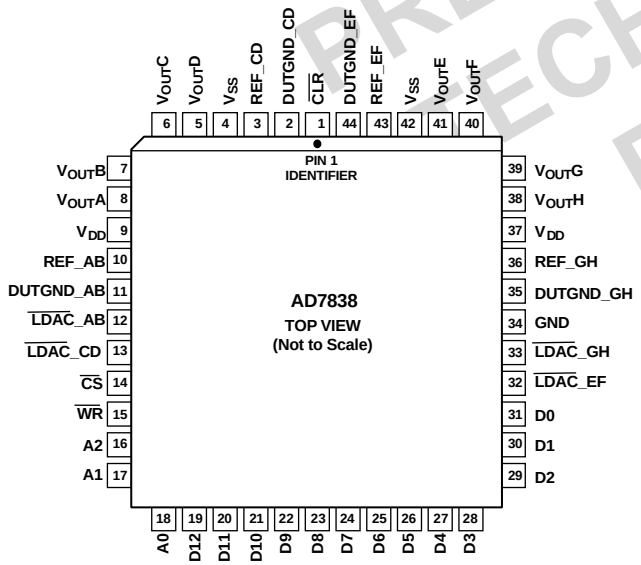
NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latchup.

ORDERING GUIDE

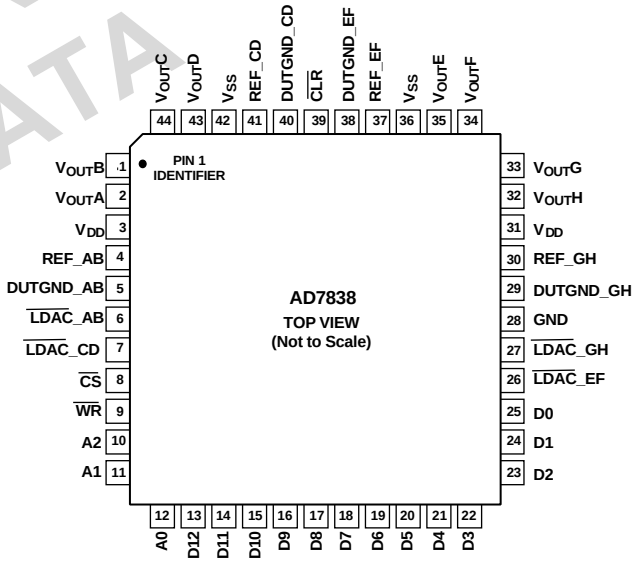
Model	Temperature Range	Relative Accuracy (LSBs)	DNL (LSBs)	Package Description	Package Option
AD7838BP	–40°C to +85°C	±2	±1	Plastic Leaded Chip Carrier (PLCC)	P-44A
AD7838BS	–40°C to +85°C	±2	±1	Plastic Leaded Quad FlatPack (PQFP)	S-44

PIN CONFIGURATIONS

44 Lead PLCC



44 Lead PQFP



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7838 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

PLCC	PQFP	Name	Description
1	39	$\overline{CLR}$	Clear Input (Active Low). Driving this asynchronous input low sets the contents of all latches to 1000 Hex. All DAC outputs are set to DUTGND.
2	40	DUTGND_CD	Device Sense Ground for DAC C and DAC D.
3	41	REF_CD	Reference Voltage Input for DAC C and DAC D.
4, 42	42, 36	V_{SS}	Negative Power Supply (–5 V ± 5%). Both pins should be connected to this supply and decoupled to system analog ground with a 0.1 µF to 1 µF capacitor.
5	43	V_{OUT} D	DAC D Output Voltage.
6	44	V_{OUT} C	DAC C Output Voltage.
7	1	V_{OUT} B	DAC B Output Voltage.
8	2	V_{OUT} A	DAC A Output Voltage.
9, 37	3, 31	V_{DD}	Positive Power Supply (5 V ± 5%). Both pins should be connected to this supply and decoupled to system analog ground with a 0.1 µF to 1 µF capacitor.
10	4	REF_AB	Reference Voltage Input for DAC A and DAC B.
11	5	DUTGND_AB	Device Sense Ground for DAC A and DAC B.
12	6	$\overline{LDAC}$_AB	Active Low Load Input. Driving this asynchronous input low transfers the contents of input latches A and B to their respective DAC latches.
13	7	$\overline{LDAC}$_CD	Active Low Load Input. Driving this asynchronous input low transfers the contents of input latches C and D to their respective DAC latches.
14	8	$\overline{CS}$	Active Low Chip Select Input.
15	9	$\overline{WR}$	Active Low Write input. $\overline{WR}$ in association with $\overline{CS}$ loads data into the input latch selected by the Address pins A0 to A2.
16	10	A2	Address Bit 2.
17	11	A1	Address Bit 1.
18	12	A0	Address Bit 0.
19–31	13-25	D12–D0	Data Inputs.
32	26	$\overline{LDAC}$_EF	Active Low Load Input. Driving this asynchronous input low transfers the contents of input latches E and F to their respective DAC latches.
33	27	$\overline{LDAC}$_GH	Active Low Load Input. Driving this asynchronous input low transfers the contents of input latches G and H to their respective DAC latches.
34	28	GND	Ground.
35	29	DUTGND_GH	Device Sense Ground for DAC G and DAC H.
36	30	REF_GH	Reference Voltage Input for DAC G and DAC H.
38	32	V_{OUT} H	DAC H Output Voltage.
39	33	V_{OUT} G	DAC G Output Voltage.
40	34	V_{OUT} F	DAC F Output Voltage.
41	35	V_{OUT} E	DAC E Output Voltage.
43	37	REF_EF	Reference Voltage Input for DAC E and DAC F.
44	38	DUTGND_EF	Device Sense Ground for DAC E and DAC F.

TERMINOLOGY

INTEGRAL NONLINEARITY

For the DAC, relative accuracy or endpoint nonlinearity is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity.

BIPOLAR ZERO-CODE ERROR

Ideally, with a digital code of 1000 Hex loaded to the DAC latch, the output should be 0 V with respect to DUTGNDxx. Any deviation from 0 V at this code is the bipolar zero-error. Bipolar zero-code error is expressed in LSBs.

GAIN ERROR

This is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal expressed as a percent of the full-scale value. It includes full-scale errors but not offset errors.

DIGITAL FEEDTHROUGH

Digital feedthrough is a measure of the impulse injected into the analog output of a DAC from the digital inputs of the same DAC but is measured when the DAC is not updated. It is specified in nV-secs and is measured with a full-scale code change on the data bus i.e., from all 0s to all 1s and vice versa.

DIGITAL CROSSTALK

Digital crosstalk is the glitch impulse transferred to the output of one converter due to a digital code change to another DAC. It is specified in nV-secs.

POWER SUPPLY REJECTION RATIO (PSRR)

This specification indicates how the output of the DAC is affected by changes in the power supply voltage. Power supply rejection ratio is quoted in terms of % change in output per % change in V_{DD} or V_{SS} for full-scale output of the DAC. V_{DD} or V_{SS} are varied ±5%.

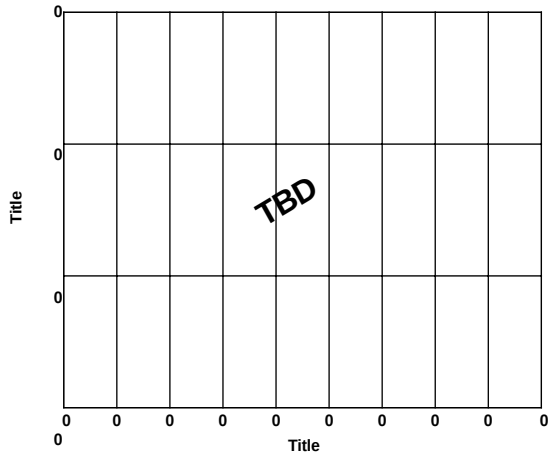


Figure 2. Typical INL Plot

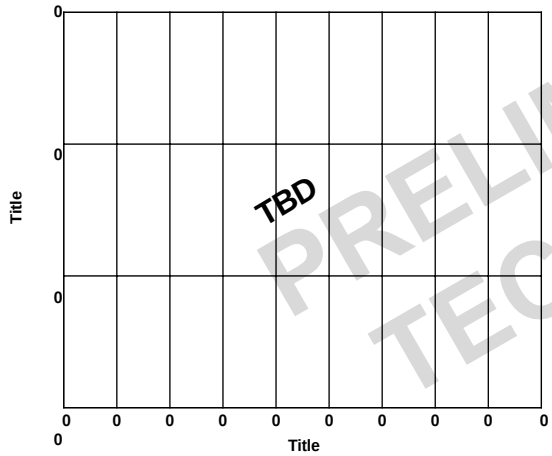


Figure 3. INL vs. Reference Voltage

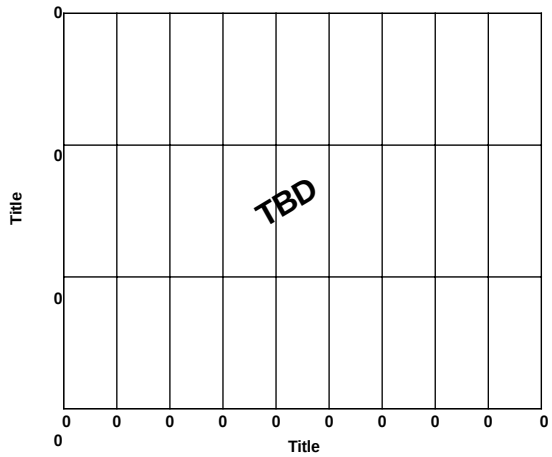


Figure 4. I_{DD}, I_{SS} vs. Temperature

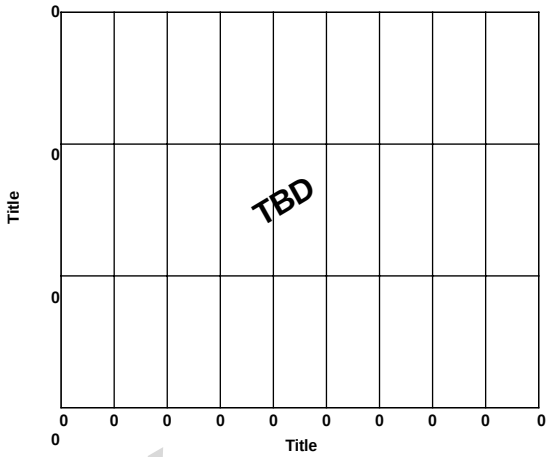


Figure 5. THD vs. Reference Frequency

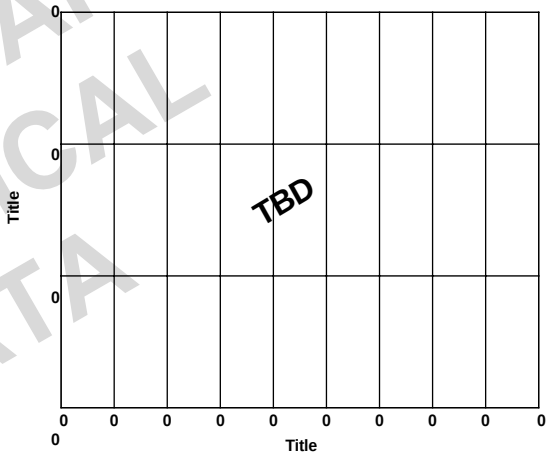


Figure 6. Settling Time vs. Load Capacitance

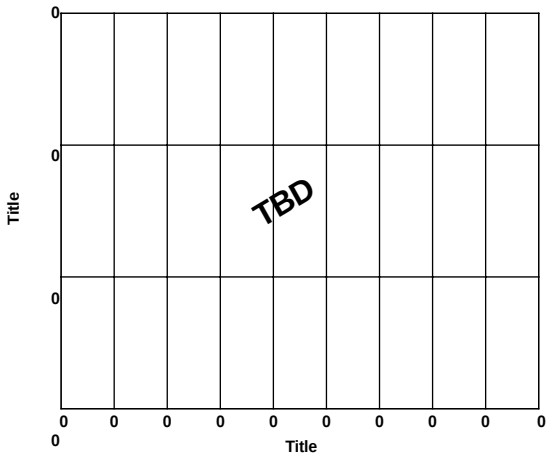


Figure 7. Reference Input Small Signal Frequency Response

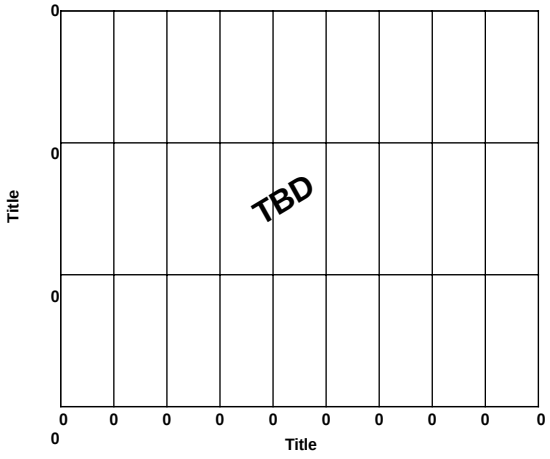


Figure 8. Reference Input Large Signal Frequency Response

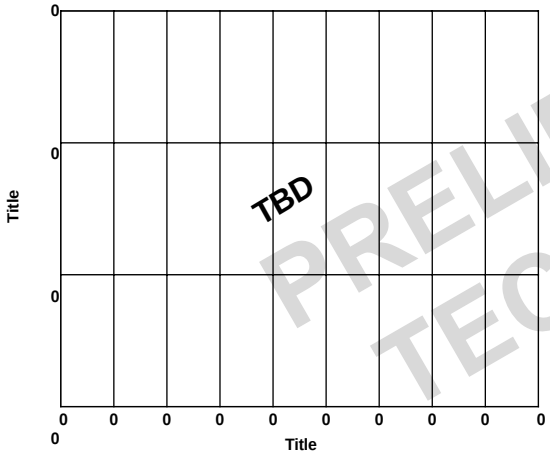


Figure 9. Reference Feedthrough

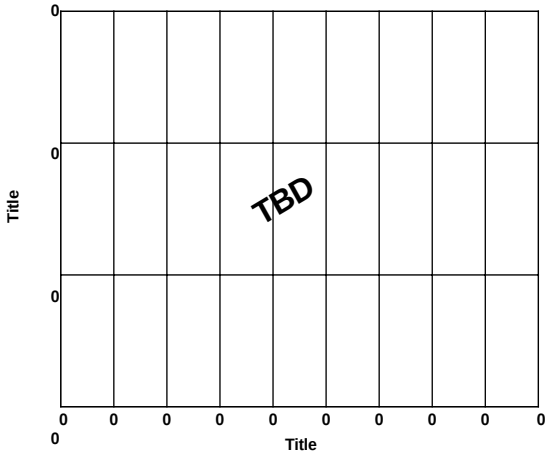


Figure 10. PSRR vs. Frequency

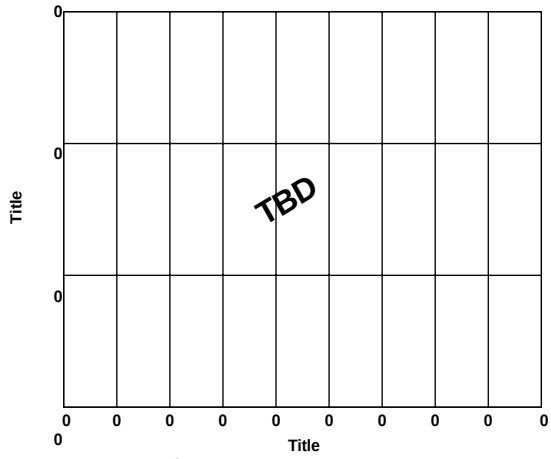


Figure 11. Full-Scale Error vs. Load Resistance

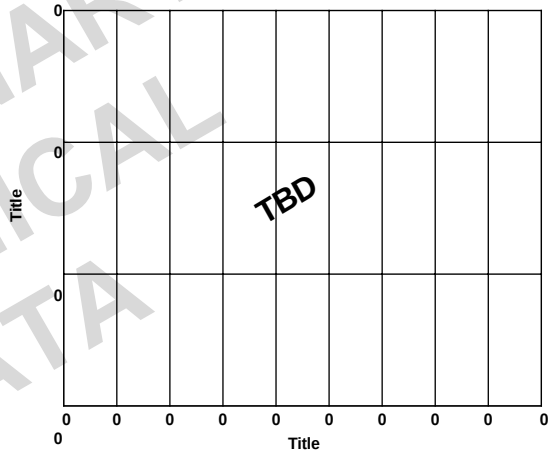


Figure 12. Positive Settling Time to Full-Scale Step (0000 Hex to 1FFF Hex)

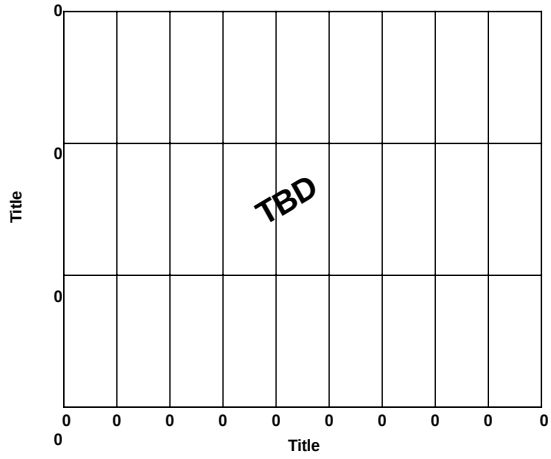


Figure 13. Negative Settling Time to Full-Scale Step (1FFF Hex to 0000 Hex)

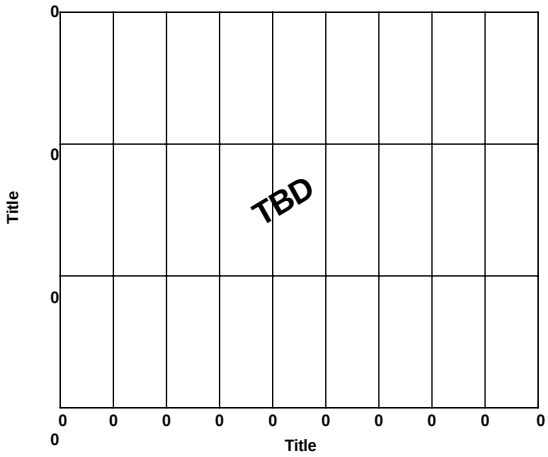


Figure 14. Dynamic Response (0000 Hex to 1FFF Hex)

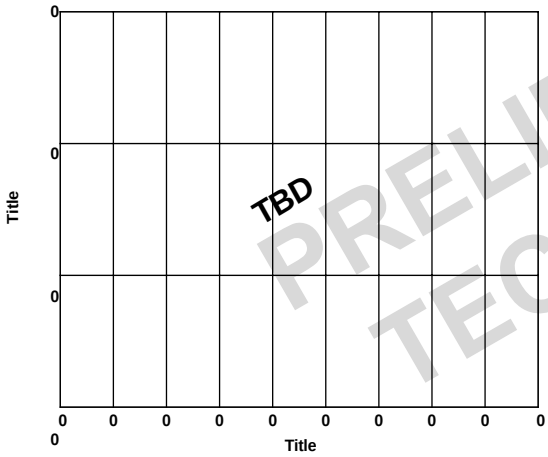


Figure 15. Digital Feedthrough

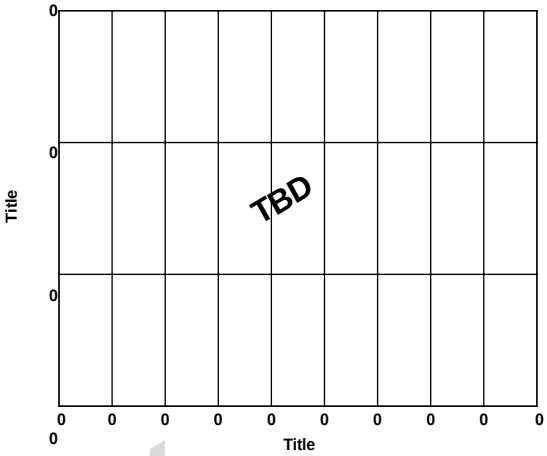


Figure 16. Adjacent Channel Crosstalk

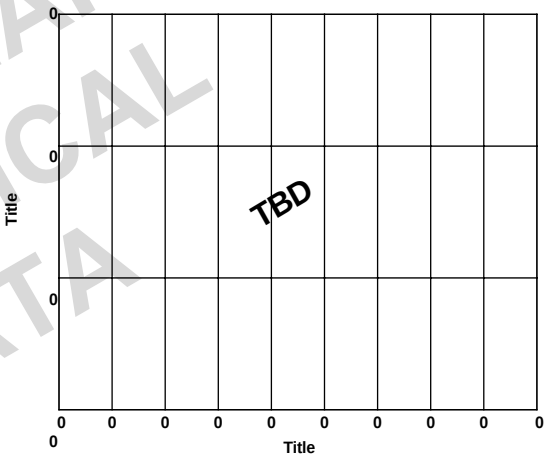


Figure 17. Adjacent Channel Crosstalk

CIRCUIT INFORMATION

D/A SECTION

The AD7838 contains eight identical 13-bit, voltage-mode digital-to-analog converters. Each DAC consists of a highly stable, thin-film, "inverted" R-2R ladder and 13 high-speed switches. The simplified circuit diagram for one channel is shown in Figure 18. Note that the AD7838 has one reference input and one analog-ground input for each pair of DACs. The different REFxx inputs allow each DAC pair to have different full-scale output voltages and the different DUTGNDxx inputs allow each DAC pair to have different offset voltages.

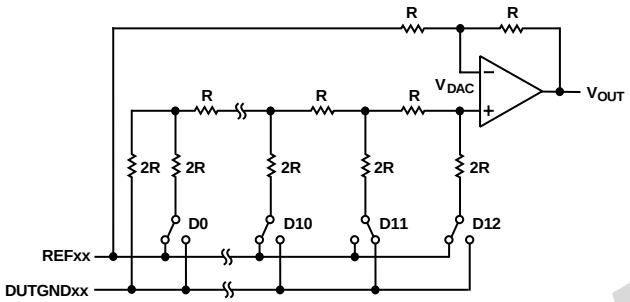


Figure 18. Circuit Diagram

OUTPUT AMPLIFIER SECTION

Each voltage-mode DAC output is buffered by a precision gain-of-two amplifier with a typical slew rate of 3 V/µs. This buffer amplifier will drive a 10 kΩ and 50 pF load to within 0.5 V of V_{DD} and V_{SS}. With a full-scale transition at its output, the typical settling time to ±0.5 LSB is 5 µs when loaded with 10 kΩ in parallel with 50 pF, or 6 µs when loaded with 10 kΩ in parallel with 100 pF. The inverting terminal of the amplifier is connected to the REFxx input which results in a bipolar output voltage range from –REFxx to 4095/4096 REFxx.

The output amplifier multiplies V_{DAC} (the output voltage from the DAC ladder) by two and level-shifts it with the reference voltage.

$$V_{OUT} = 2\ V_{DAC} - REFxx$$

REF AND DUTGND INPUTS

The REFxx inputs can range from DUTGNDxx to V_{DD} and the DUTGNDxx inputs can be offset by any voltage from V_{DD} to V_{SS}. However, the DUTGNDxx offset-voltage potential must be lower than the REFxx reference-voltage potential.

The input impedance at the REFxx pins of the AD7838 is the parallel combination of the two individual DAC reference input impedances. It is code dependent and can vary from 5 kΩ to 50 kΩ. The lowest input impedance occurs when both DACs are loaded with digital code 0 1010 1010 1010 (0AAA Hex). The maximum value occurs when the code is 0000 Hex. Therefore, it is important that the external reference source presents a low output impedance to the REFxx terminal of the AD7838 under changing load conditions. Due to transient currents at the reference inputs during digital code changes a 0.1 µF (or greater) decoupling capacitor is recommended on the REFxx inputs if dc reference voltages are used.

The nodal capacitance at the REFxx terminals is also code dependent and can vary from 125 pF to 300 pF. The minimum capacitance occurs when the code of the DAC pair is 0000 Hex and the maximum value occurs when the code on both DACs is 1FFF Hex.

The maximum current flowing out of a DUTGNDxx pin is:

$$I_{DUTGNDxx} = (REFxx - DUTGNDxx)/5\ k\Omega$$

Therefore, the voltage source used to supply the DUTGNDxx offset voltage must be able to sink/source the required DUTGNDxx input current.

Table I shows the DAC output voltage for various combinations of DUTGND and REF.

Table I. AD7838 DAC Output Voltages

Condition	Code (Hex)	Output	LSB
DUTGND = 0 V REF = +4.50 V	0000 1000 1FFF	–4.50 V +0.00 V +4.50 V	2(REF – DUTGND)/8192 = 1.1 mV
DUTGND = +2.25 V REF = +4.50 V	0000 1000 1FFF	+0.00 V +2.25 V +4.50 V	2(REF – DUTGND)/8192 = 0.55 mV
DUTGND = +2.00 V REF = +2.50 V	0000 1000 1FFF	+1.50 V +2.00 V +2.50 V	2(REF – DUTGND)/8192 = 0.122 mV

DIGITAL INTERFACE

The AD7838 digital inputs are compatible with both TTL and CMOS levels. The AD7838 contains a parallel interface allowing this octal DAC to interface to industry standard microprocessors using a data bus at least 13 bits wide. The AD7838 has a double buffered interface, which allows for simultaneous updating of all DAC outputs. The AD7838 contains two latches for each DAC: an input latch that receives data from the data bus and a DAC latch that receives data from the input latch. Address lines A0, A1 and A2 select which input latch receives data from the data bus. Table II shows the selection table for the eight DACs. Figure 19 shows the input latch control logic.

Table III shows the truth table for AD7838 interface operation. $\overline{CS}$ and $\overline{WR}$ control the loading of data into the input latch. These control signals are level triggered; therefore, the input latch can be made transparent by holding both signals at a logic low level. Input data is latched into the input latch on the rising edge of $\overline{CS}$ or $\overline{WR}$.

Table II. DAC Addressing for the AD7838

A2	A1	A0	Function
0	0	0	DAC A Input Latch
0	0	1	DAC B Input Latch
0	1	0	DAC C Input Latch
0	1	1	DAC D Input Latch
1	0	0	DAC E Input Latch
1	0	1	DAC F Input Latch
1	1	0	DAC G Input Latch
1	1	1	DAC H Input Latch

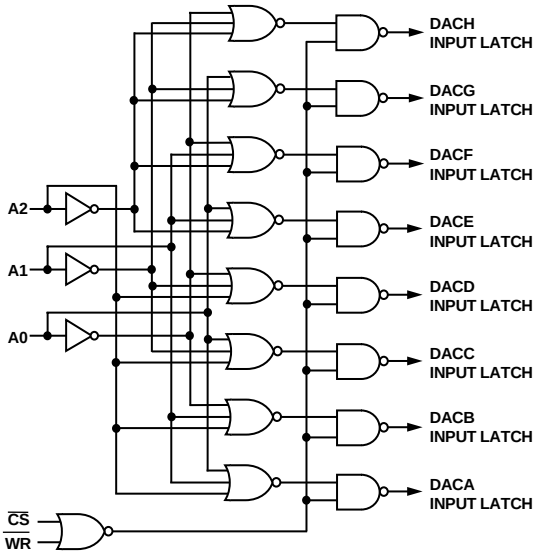


Figure 19. Control Logic for Input Latches

The DAC latches are also level triggered. Data is transferred from the input latches to the DAC latches under control of the asynchronous $\overline{LDxx}$ signal. The AD7838 has one $\overline{LDxx}$ input for each pair of DACs. Only the data in the DAC latch determines each DAC's analog output. The DAC latch is transparent when $\overline{LDxx}$ is low. Figure 20 shows the control logic for the DAC latches.

The address lines (A0–A2) must be valid for the whole time $\overline{CS}$ and $\overline{WR}$ are low to avoid writing data to the wrong input latch. If $\overline{LDxx}$ is brought low when $\overline{WR}$ and $\overline{CS}$ are low, it must be held low for t_3 or longer after $\overline{WR}$ or $\overline{CS}$ go high. The write cycle timing diagram is shown in Figure 1.

A falling edge of the $\overline{CLR}$ signal sets all DAC outputs to a nominal 0 V, regardless of what levels $\overline{CS}$, $\overline{WR}$ and $\overline{LDxx}$ are at. All input latches and DAC latches are latched with 1000 Hex on a rising edge of $\overline{CLR}$.

Table III. Truth Table for AD7838 Interface

$\overline{CLR}$	$\overline{LDxx}$	$\overline{WR}$	$\overline{CS}$	Function
1	0	0	0	Both Latches Are Transparent
1	1	1	X	Both Latches Are Latched
1	1	X	1	Both Latches Are Latched
1	X	0	0	Input Latch Is Transparent
1	X	1	X	Input Latch Is Latched
1	X	X	1	Input Latch Is Latched
1	0	X	X	DAC Latch Is Transparent
0	X	X	X	All Input and DAC Latches Are at 1000 Hex, The Outputs Are at DUTGNDxx

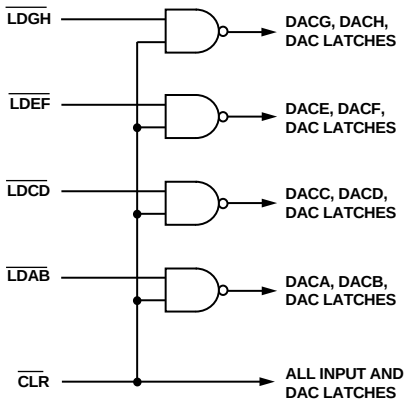


Figure 20. Control Logic for DAC Latches

APPLICATIONS

Bipolar Output Configuration

Figure 21 shows the AD7838 configured for ±4.096 V operation. The REF198 (a low dropout, micropower precision reference) provides a +4.096 V reference for the REFxx input. Tie DUTGNDxx to the system ground for symmetrical bipolar operation. The code table for symmetrical bipolar operation of the AD7838 is shown in Table IV. Other suitable references include other members of the precision REF19x family, the REF192 (+2.5 V) and the REF193 (+3.0 V).

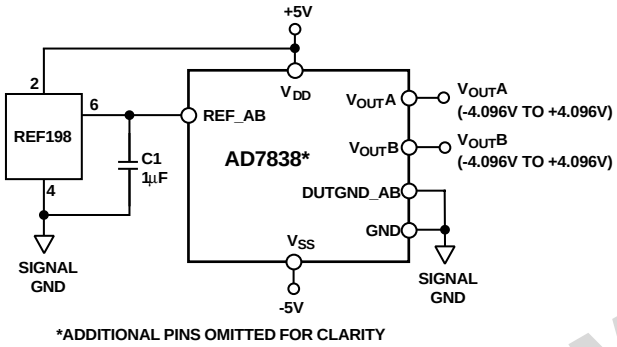


Figure 21. Bipolar ±4.096 V Operation

Table IV. Code Table for Bipolar Operation (DUTGNDxx = 0 V)

Binary Number in DAC Register MSB			LSB	Analog Output (V_{OUT})
1	1111	1111	1111	+REF (4095/4096) V
1	0000	0000	0001	+REF (1/4096) V
1	0000	0000	0000	0 V
0	1111	1111	1111	–REF (1/4096) V
0	0000	0000	0001	–REF (4095/4096) V
0	0000	0000	0000	–REF V

NOTE
For REF = +4.096 V, 1 LSB = 2 REF/2^{13} = 8.192 V/8192 = 1 mV.

Unipolar Output Configuration

Figure 22 shows the AD7838 set up for a unipolar output voltage (0 to REF). The DUTGNDxx pin is offset by REFxx/2 using two matched resistors to divide the +4.096 V reference. The result is an output voltage range from 0 V to 4.0955 V. The code table for this unipolar mode of operation is shown in Table V.

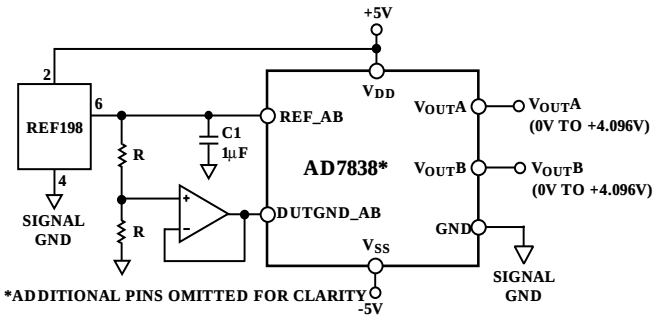


Figure 22. Unipolar 0 V to +4.096 V Operation

Table V. Code Table for Unipolar Operation (DUTGNDxx = REFxx/2 V)

Binary Number in DAC Register MSB			LSB	Analog Output (V_{OUT})
1	1111	1111	1111	+REF (8191/8192) V
1	0000	0000	0000	+REF/2 V
0	0000	0000	0001	+REF (1/8192) V
0	0000	0000	0000	0 V

NOTE
For REF = +4.096 V, 1 LSB = REF/2^{13} = 4.096 V/8192 = 0.5 mV.

The DUTGNDxx pins can also be digitally offset by connecting the output of one DAC to the DUTGND pin of another DAC. A DAC output should not be connected to its own DUTGND input.

AD7838 as a Multiplying DAC

The REF inputs can accept ac signals as well as the dc configurations shown above. This allows the AD7838 to be used for multiplying applications. Multiplying is limited to two quadrant multiplication because the REF inputs only accept positive voltages. When using an ac reference, do not use bypass capacitors at the REF input pins.

Choosing a Reference

Since the REFxx inputs on the AD7838 are unbuffered, they have a code-dependent input impedance which varies from 5 kΩ to 50 kΩ. If one reference is used to drive all four REFxx inputs, the impedances are in parallel and the reference must drive a load which varies from 1.25 kΩ to 12.5 kΩ. If the low dropout REF192 (+2.5 V) is used, the current which the reference needs to supply varies from 2 mA to 0.2 mA (1.8 mA range). The REF192 can supply 30 mA from a +5 V supply. The load regulation of the REF192 is 10 ppm/mA which results in an error of 18 ppm (45 µV) for the 1.8 mA step. This corresponds to a 90 µV error over the ±2.5 V output range (0.147 LSB). The REF198 gives a 4.096 V output resulting in a ±4.096 V output on the DAC. The load regulation is 4 ppm/mA which results in an error of 7.2 ppm (30 µV) for the 1.8 mA step. This corresponds to a 60 µV error over the ±4.096 V output range (0.06 LSB).

This problem can be overcome by buffering the reference with an op amp in a voltage follower configuration before applying the reference to the REFxx pin. The maximum capacitive load

of the DAC ladder is typically 300 pF so the op amp needs to drive 1200 pF if all four REFxx pins are driven from the same source.

If the REFxx pins are driven separately, as seen in Figure 23, the drive requirements of the op amp are less. This configuration also has the advantage that a code transition which causes a change in the load on the reference now only affects the DAC pair where the code transition occurs and not all eight DACs. The effects of board-lead resistance can be eliminated by sensing the feedback voltage for the op amp directly at the REFxx terminal.

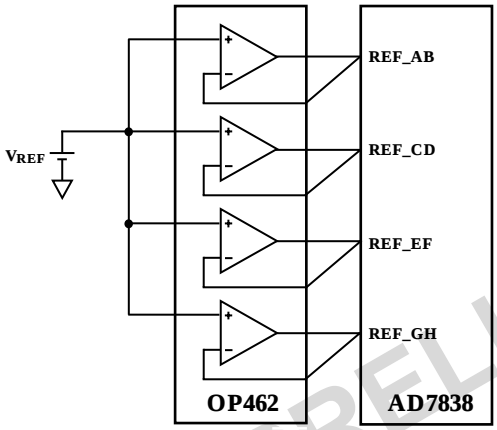


Figure 23. Buffered References

Power Supply Bypassing and Grounding

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD7838 is mounted should be designed such that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be separated easily. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should only be joined at one place. The GND pin of the AD7838 should be connected to the AGND of the system. If the AD7838 is in a system where multiple devices require an AGND to DGND connection, the connection should be made at one point only, a star ground point which should be established as close as possible to the AD7838.

Digital lines running under the device should be avoided as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7838 to avoid noise coupling. The power supply lines of the AD7838 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other parts of the board and should never be run near the analog inputs.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best but not always possible with a double sided board. In this technique, the component side of the board is dedicated to ground plane while signal traces are placed on the solder side.

The AD7838 should have ample supply bypassing located as close to the package as possible, ideally right up against the device. Figure 24 shows the recommended capacitor values of 10 µF in parallel with 0.1 µF on each of the supplies. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low Effective Series Resistance (ESR) and Effective Series Inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

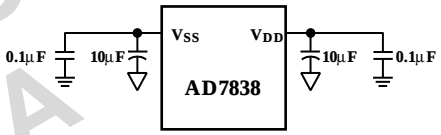


Figure 24. Recommended Decoupling Scheme for AD7838

MICROPROCESSOR INTERFACING

Interfacing the AD7838—16-Bit Interface

The AD7838 can be interfaced to a variety of 16-bit microcontrollers or DSP processors. Figure 25 shows the AD7838 interfaced to a generic 16-bit microcontroller/DSP processor. The lower address lines from the processor are connected to A0, A1 and A2 on the AD7838 as shown. The upper address lines are decoded to provide a chip select signal for the AD7838. The fast interface timing of the AD7838 allows direct interface to a wide variety of microcontrollers and DSPs as shown in Figure 25.

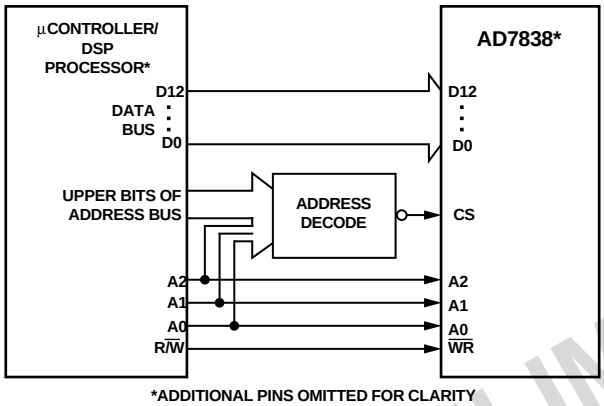


Figure 25. AD7838 Parallel Interface

Automated Test Equipment

The AD7838 is particularly suited for use in an automated test environment. Figure 26 shows the AD7838 providing the necessary voltages for the pin driver and the window comparator in a typical ATE pin electronics configuration. REF194s are used to provide reference voltages of +4.5 V for the AD7838.

One of the REF194s is used as a reference for DACs A and B. These DACs are used to provide high and low levels for the pin driver. DUTGND_AB is set at +2 V with respect to GND. $V_{OUT}A$ and $V_{OUT}B$ vary between –0.5 V and +4.5 V. When a clear is performed on the AD7838, the outputs will be 0 V with respect to DUTGND_AB.

The other REF194 is used to provide a reference voltage for DACs G and H. These provide the reference voltages for the window comparator shown in the diagram. In this case, DUTGND_GH is tied to GND. When the AD7838 is cleared, $V_{OUT}G$ and $V_{OUT}H$ are cleared to 0 V with respect to DUTGND_GH.

Programmable Reference Generation for the AD7838 in An ATE Application

The AD7838 is particularly suited for use in an automated test environment. The reference input for the AD7838 octal 13-bit DAC requires four single-ended references for the eight DACs. Programmable references may be a requirement in some ATE applications.

There are a number of suitable 8- and 10-bit DACs available that would be suitable to drive the reference inputs of the AD7838, such as the AD7804 which is a quad 10-bit digital-to-analog converter with serial load capabilities. The voltage output from this DAC is in the form of $V_{BIAS} \pm V_{SWING}$ and rail-to-rail operation is achievable. The voltage reference for this DAC can be internally generated or provided externally. This DAC also contains an 8-bit SUB DAC which can be used to shift the complete transfer function of each DAC around the V_{BIAS} point. This can be used as a fine trim on the output voltage. In this application, one AD7804 is required to provide programmable reference capability for all eight DACs. The AD7804 is used to drive the $V_{REF}(+)$ pins.

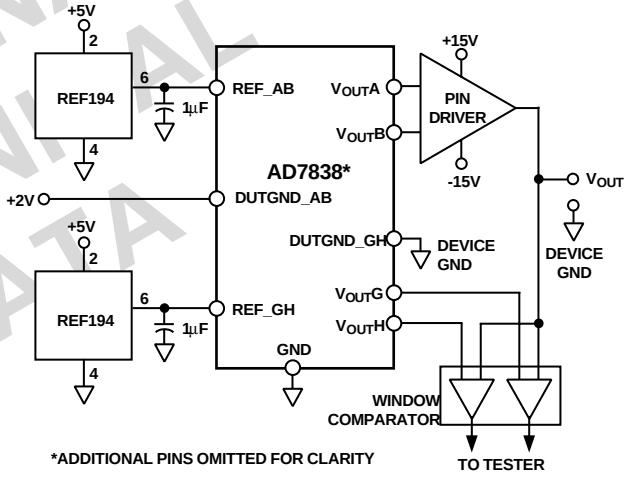


Figure 26. ATE Application

Another suitable DAC for providing programmable reference capability is the AD8803. This is an octal 8-bit TRIMDAC® and provides independent control of both the top and bottom ends of the TRIMDAC. This is helpful in maximizing the resolution of devices with a limited allowable voltage control range.

The AD8803 has an output voltage range of GND to V_{DD} (0 V to +5 V). To trim the REF input, the appropriate trim range on the AD8803 DAC can be set using the V_{REFL} and V_{REFH} pins allowing 8 bits of resolution between the two points. This will allow the REF pin to be adjusted.

Figure 27 shows a typical application circuit to provide programmable reference capabilities for the AD7838.

TRIMDAC is a registered trademark of Analog Devices, Inc.

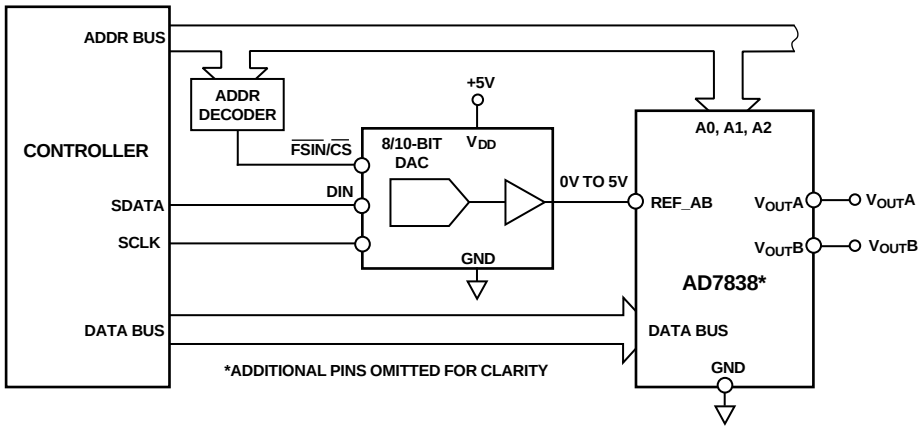
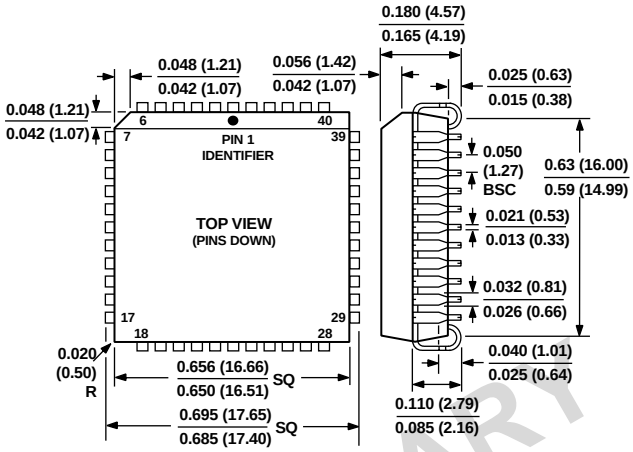


Figure 27. Programmable Reference Generation for the AD7838

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

44-Lead PLCC (P-44A)



44-Lead PQFP (S-44)