a

Dual-Channel, 80 MSPS WCDMA Receive Signal Processor (RSP)

PRODUCT CONCEPT AD6634

FEATURES

80 MSPS Wide Band Inputs (14 linear bit plus 3 RSSI)
Processes 2 WCDMA channels (UMTS or cdma2000 1x) or 4 GSM/EDGE, IS136 channels
Four Independent Digital Receivers in a Single Package
Four Serial Output Ports (Master and Slave modes)
Dual 16-bit Parallel Output Ports and Dual 8-bit Link Ports
Programmable Digital AGC Loops
Digital Re-sampling for non-Integer Decimation rates
Programmable Decimating FIR Filters
Interpolating Half Band Filters
Programmable Attenuator Control for Clip prevention and external gain ranging via Level Indicator
Flexible Control for Multi-Carrier and Phased Array
3.3 Volt I/O, 2.5 Volt CMOS Core
User Configurable Built in Self Test (BIST) capability
JTAG Boundary Scan

APPLICATIONS

Multi-carrier, Multi-mode Digital Receivers
GSM, IS136, EDGE, PHS, IS95, UMTS, cdma2000
Micro and Pico Cell Systems, Software Radios
Wireless Local Loop
Smart Antenna Systems
In Building Wireless Telephony

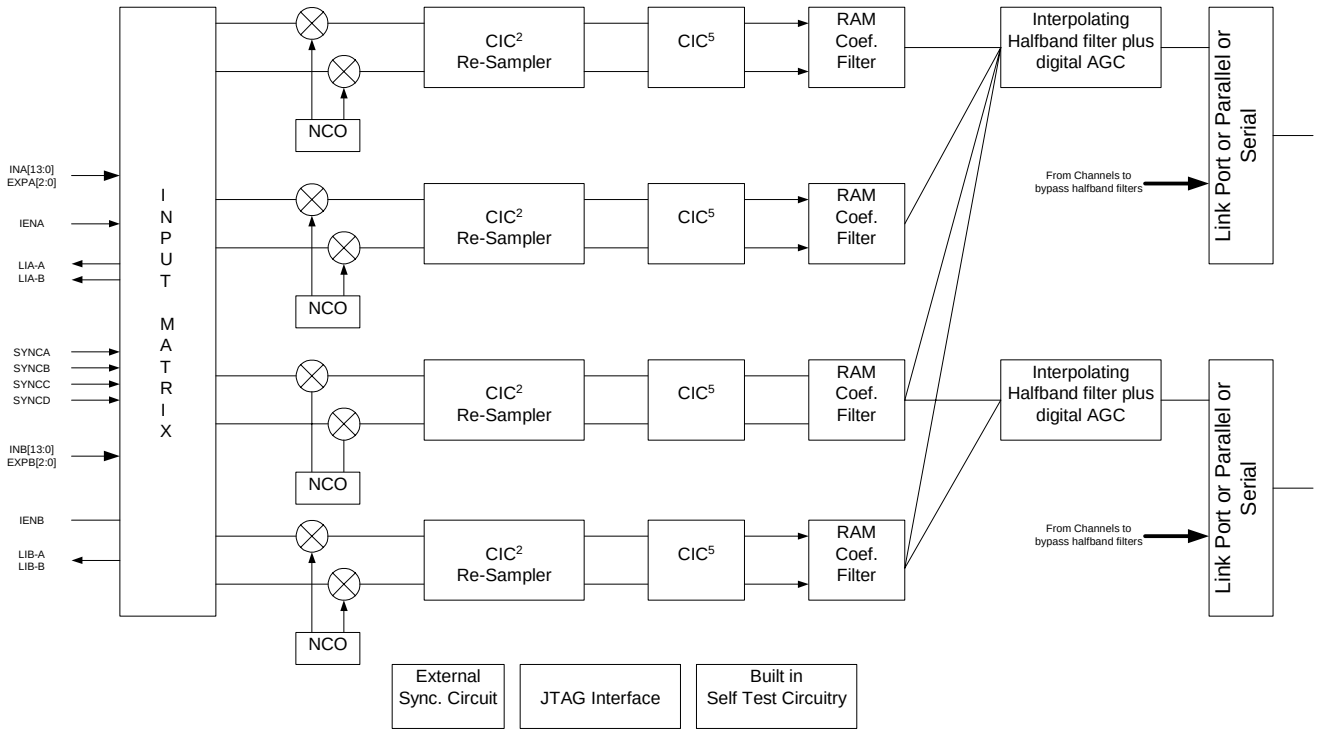


Figure 1. AD6634 Block Diagram

PRODUCT DESCRIPTION

The AD6634 is a multi-mode four channel digital Receive Signal Processor (RSP) capable of processing up to two WCDMA channels. Each channel consists of four cascaded signal-processing elements: a frequency translator, two fixed-coefficient decimating filters, and a programmable coefficient-decimating filter. Each input port has input level threshold detection circuitry and an AGC controller for accommodating large dynamic ranges or situations where gain ranging converters are used. Dual 16-bit parallel output ports accomodate high data rate WBCDMA applications. On-chip interpolating half band can also be used to further increase the output rate. In addition, each parallel output port has a digital AGC for output data scaling. Link port outputs are provided to enable glue-less interfaces to our TigerSHARC™ DSP core.

The AD6634 is part of Analog Devices' SoftCell™ Multi-carrier transceiver chipset designed for compatibility with Analog Devices family of high sample rate IF sampling ADCs (AD6640/AD6644 12 & 14 bit). The SoftCell™ receiver comprises a digital receiver capable of digitizing an entire spectrum of carriers and digitally selecting the carrier of interest for tuning and channel selection. This architecture eliminates redundant radios in wireless base station applications.

High dynamic range decimation filters offer a wide range of decimation rates. The RAM-based architecture allows easy reconfiguration for multi-mode applications.

The decimating filters remove unwanted signals and noise from the channel of interest. When the channel of interest occupies less bandwidth than the input signal, this rejection of out-of-band noise is called "processing gain". By using large decimation factors, this "processing gain" can improve the SNR of the ADC by 30 dB or more. In addition, the programmable RAM Coefficient filter allows anti-aliasing, matched filtering, and static equalization functions to be combined in a single, cost-effective filter. Half band interpolating filters at the output are used in WCDMA applications to increase the output rate from 2x to 4x of the chip rate. The AD6634 is also equipped with two independent automatic gain control (AGC) loops for direct interface to a RAKE receiver.

The AD6634 is compatible with standard ADC converters such as the AD664x, AD9042, AD943X and the AD922x families of data converters. The AD6634 is also compatible with the AD6600 Diversity ADC providing a cost and size reduction path.

CONTENTS

ARCHITECTURE

The AD6634 has four signal processing stages: a Frequency Translator, second order Re-Sampling Cascaded Integrator Comb FIR Filters (rCIC2), a fifth order Cascaded integrator Comb FIR Filter (CIC5) and a RAM Coefficient FIR Filter (RCF). Multiple modes are supported for clocking data into and out of the chip and provide flexibility for interfacing to a wide variety of digitizers. Programming and control is accomplished via serial and microprocessor interfaces.

Frequency translation is accomplished with a 32-bit complex Numerically Controlled Oscillator (NCO). Real data entering this stage is separated into in-phase (I) and quadrature (Q) components. This stage translates the input signal from a digital intermediate frequency (IF) to digital baseband. Phase and amplitude dither may be enabled on-chip to improve spurious performance of the NCO. A phase-offset word is available to create a known phase relationship between multiple AD6634s or between channels.

Following frequency translation a re-sampling, fixed coefficient, high speed, second order, Re-Sampling Cascade Integrator Comb (rCIC2) filter that reduces the sample rate based on the ratio between the decimation and interpolation registers.

The next stage is a fifth order Cascaded Integrator Comb (CIC5) filter whose response is defined by the decimation rate. The purpose of these filters is to reduce the data rate to the final filter stage so that it can calculate more taps per output.

The final stage is a sum-of-products FIR filter with programmable 20-bit coefficients, and decimation rates programmable from 1 to 256 (1-32 in practice). The RAM Coefficient FIR Filter (RCF in Figure 1) can handle a maximum of 160 taps.

The overall filter response for the AD6634 is the composite of all decimating and interpolating stages. Each successive filter stage is capable of narrower transition bandwidths but requires a greater number of CLK cycles to calculate the output. More decimation in the first filter stage will minimize overall power consumption. Data from the chip is interfaced to the DSP via a high-speed synchronous serial port.

Figure 2a illustrates the basic function of the AD6634: to select and filter a single channel from a wide input spectrum. The frequency translator “tunes” the desired carrier to baseband. Figure 2b shows the combined filter response of the rCIC2, CIC5, and RCF.

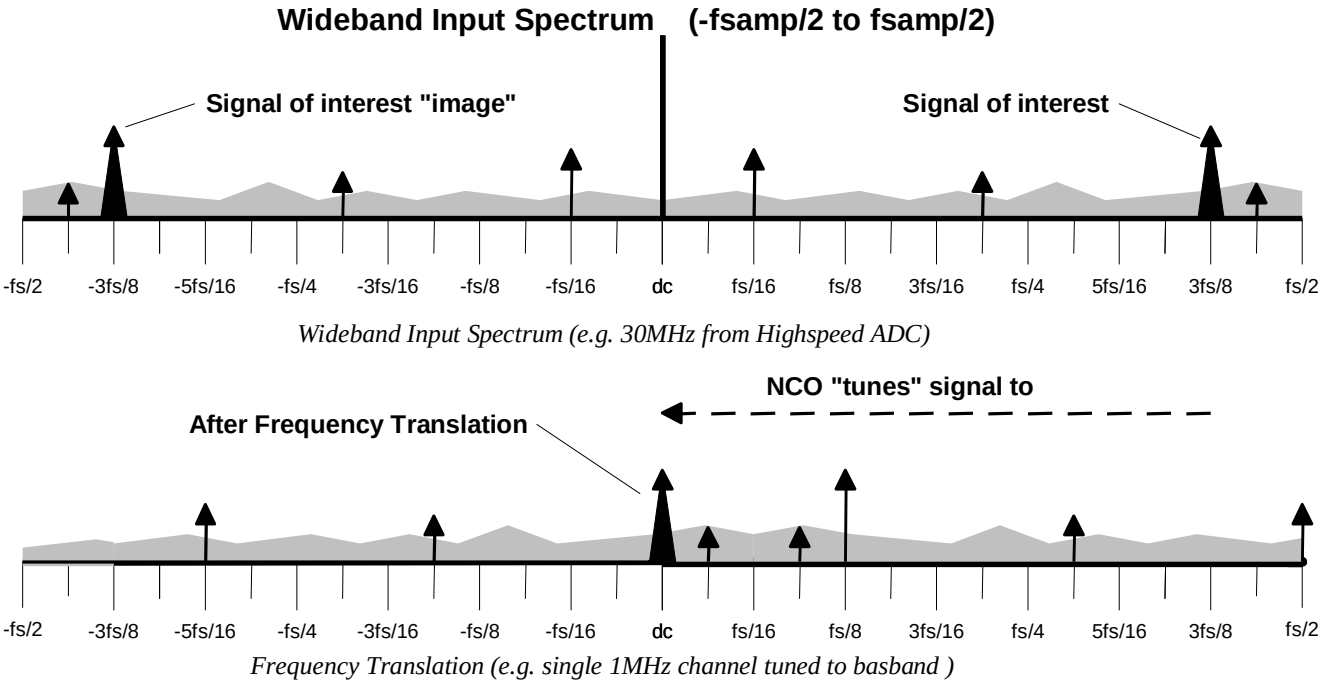


Figure 2a. AD6634 Frequency Translation of Wideband Input Spectrum

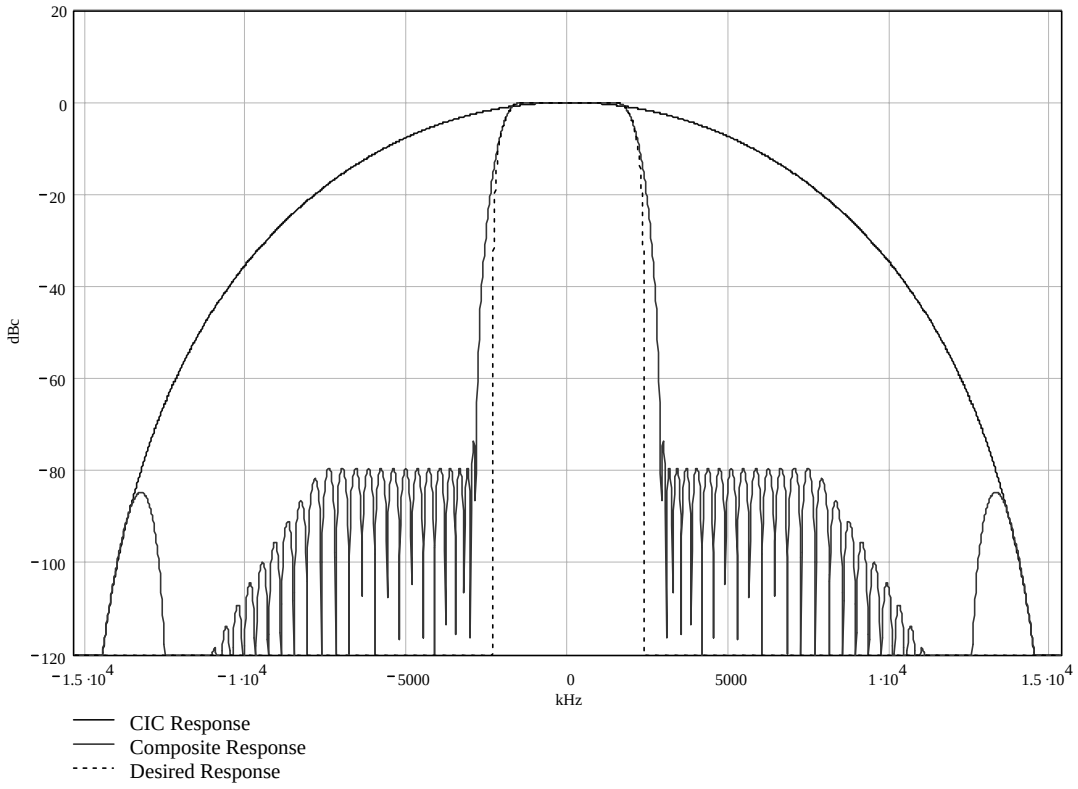


Figure 2b. Composite Filter Response of rCIC2, CIC5, and RCF

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage…….……..…….. +3.6V
Input Voltage……...-0.3 to 5.3V (5V Tolerant)
Output Voltage Swing……...-0.3V to VDDIO +0.3V
Load Capacitance……..……200pF
Junction Temperature Under Bias…..…..……+125°C
Storage Temperature Range…….....-65°C to +150°C
Lead Temperature (5 sec)……..…….…..+280°C

Notes

[1]Stresses greater than those listed above may cause permanent damage to the device These are stress ratings only; functional operation of the devices at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

128-Lead MQFP:
θ_{JA}==41°C /Watt, no airflow
θ_{JA}= 39°C/Watt, 200-lfpm airflow
θ_{JA}= 37°C/Watt, 400-lfpm airflow
Thermal measurements made in the horizontal position on a 4-layer board.

EXPLANATION OF TEST LEVELS

I	100% Production Tested.
II	100% Production Tested at 25°C, and Sampled Tested at Specified Temperatures.
III	Sample Tested Only
IV	Parameter Guaranteed by Design and Analysis
V	Parameter is Typical Value Only
VI	100% Production Tested at 25°C, and Sampled Tested at Temperature Extremes

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD6634XBC[1]	-40°C to +70°C (Ambient)	196-Lead BGA (Ball Grid Array)	196 BGA
AD6634BBC	-40°C to +70°C (Ambient)	196-Lead BGA (Ball Grid Array)	196 BGA
AD6634BC/PCB		Evaluation Board with AD6634 and Software	

Notes

[1]X-Grade Material is Pre-Production material, normally shipped during product characterization and qualification.

ESD SENSITIVITY

The AD6634 is an ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6634 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

RECOMMENDED OPERATING CONDITIONS

Parameter	Temp	Test Level	AD6634AS MIN	Typ	Max	Units
VDD		IV	2.375	2.5	2.675	V
VDDIO		IV	3.0	3.3	3.6	V
$T_{AMBIENT}$		IV	-40	+25	+70	°C

ELECTRICAL CHARACTERISTICS

Parameter (Conditions)	Temp	Test Level	AD6634AS Min	Typ	Max	Units
LOGIC INPUTS (5V TOLERANT)						
Logic Compatibility	Full	IV		3.3V CMOS		
Logic "1" Voltage	Full	IV	2.0		5.0	V
Logic "0" Voltage	Full	IV	-0.3		0.8	V
Logic "1" Current	Full	IV		1	10	uA
Logic "0" Current	Full	IV		1	10	uA
Logic "1" Current (inputs with pull-down)	Full	IV				
Logic "0" Current (inputs with pull-up)	Full	IV				
Input Capacitance	+25°C	V		4		pF
LOGIC OUTPUTS						
Logic Compatibility	Full	IV		3.3V CMOS/TTL		
Logic "1" Voltage (I_{OH}=0.25mA)	Full	IV	2.4	VDD-0.2		V
Logic "0" Voltage (I_{OL}=0.25mA)	Full	IV		0.2	0.4	V
IDD SUPPLY CURRENT						
CLK=80MHz, (VDD=2.75V, VDDIO=3.6V)	Full	IV				
I_{VDD}				400		mA
I_{VDDIO}				60		mA
CLK=GSM Example (65MSPS, VDD=2.5V, VDDIO=3.3V, dec=2/10/6 120 taps 4 chan.)	+25°C	V				
I_{VDD}				250		mA
I_{VDDIO}				24		mA
CLK=IS-136 Example	+25°C	V				
CLK=WBCDMA Example	+25°C	V				
Sleep Mode	Full	IV				mA
POWER DISSIPATION						
CLK=80MHz	Full	IV		1.1		W
CLK=65MHz GSM/EDGE Example		V		700		mW
CLK=80MHz IS-136 Example		V				
Sleep Mode	Full	IV		287		uW

Specifications subject to change without notice

GENERAL TIMING CHARACTERISTICS

Parameter (Conditions)		Temp	Test Level	AD6634AS Min	Typ	Max	Units
CLK Timing Requirements:							
t_{CLK}	CLK Period	Full	I	12.5			ns
t_{CLKL}	CLK Width Low	Full	IV	4.5	0.5 x t_{CLK}		ns
t_{CLKH}	CLK Width High	Full	IV	4.5	0.5 x t_{CLK}		ns
/RESET Timing Requirements:							
t_{RESL}	/RESET Width Low	Full	IV	30.0			ns
Input Wideband Data Timing Requirements:							
t_{SI}	Input to ↑CLK Setup Time	Full	IV	0.8			ns
t_{HI}	Input to ↑CLK Hold Time	Full	IV	2.0			ns
Level Indicator Output Switching Characteristics:							
t_{DLI}	↑CLK to LI(A-A,B; B-A,B) Output Delay Time	Full	IV	3.8		12.6	ns
SYNC Timing Requirements:							
t_{SS}	SYNC(A,B,C,D) to ↑CLK Setup Time	Full	IV	1.0			ns
t_{HS}	SYNC(A,B,C,D) to ↑CLK Hold Time	Full	IV	2.0			ns
Master Mode Serial Port Timing Requirements (SBM=1):							
Switching Characteristics[2]							
t_{DSCLK1}	↑CLK to ↑SCLK Delay (divide by 1)	Full	IV	3.9		13.4	ns
t_{DSCLKH}	↑CLK to ↑SCLK Delay (for any other divisor)	Full	IV	4.4		14.0	ns
t_{DSCLKL}	↑CLK to ↓SCLK Delay (divide by 2 or even #)	Full	IV	3.25		6.7	ns
$t_{DSCLKLL}$	↓CLK to ↓SCLK Delay (divide by 3 or odd #)	Full	IV	3.8		6.9	ns
t_{DSDFS}	↑SCLK to SDFS Delay	Full	IV	0.2		5.3	ns
t_{DSDFE}	↑SCLK to SDFE Delay	Full	IV	-0.4		4.7	ns
t_{DSDO}	↑SCLK to SDO Delay	Full	IV	-1.0		4.0	ns
t_{DSDR}	↑SCLK to DR Delay	Full	IV	-0.3		4.6	ns
t_{DDR}	↑CLK to DR Delay	Full	IV	5.4		17.6	ns
	Input Characteristics						
t_{SSI}	SDI to ↓SCLK Setup Time	Full	IV	2.4			ns
t_{HSI}	SDI to ↓SCLK Hold Time	Full	IV	3.0			ns
Slave Mode Serial Port Timing Requirements (SBM=0):							
Switching Characteristics[2]							
t_{SCLK}	SCLK Period	Full	IV	16			ns
t_{SCLKL}	SCLK low time (when SDIV=1, divide by 1)	Full	IV	5.0			ns
t_{SCLKH}	SCLK high time (when SDIV=1, divide by 1)	Full	IV	5.0			ns
t_{DSDFE}	↑SCLK to SDFE Delay	Full	IV	3.8		15.4	ns
t_{DSDO}	↑SCLK to SDO Delay	Full	IV	3.7		15.2	ns
t_{DSDR}	↑SCLK to DR Delay	Full	IV	3.9		15.9	ns
	Input Characteristics						
t_{SSF}	SDFS to ↑SCLK Setup Time	Full	IV	1.9			ns
t_{HSF}	SDFS to ↑SCLK Hold Time	Full	IV	0.7			ns
t_{SSI}	SDI to ↓SCLK Setup Time	Full	IV	2.4			ns
t_{HSI}	SDI to ↓SCLK Hold Time	Full	IV	2.0			ns

NOTES

[1]All Timing Specifications valid over VDD range of 2.375V to 2.675V and VDDIO range of 3.0V to 3.6V.

[2]The timing parameters for SCLK, SDFS, SDFE, SDO, SDI, and DR apply to all four channels (0, 1, 2, and 3). The Slave serial port's (SCLK) operating frequency is limited to 62.5Mhz.

[3]Specification pertains to control signals: RW, (/WR), /DS, (/RD), /CS

[4](C_{LOAD}=40pF on all outputs unless otherwise specified)

Specifications subject to change without notice

MICROPROCESSOR PORT TIMING CHARACTERISTICS[1]

MICROPROCESSOR PORT, MODE INM (MODE=0)		Temp	Test Level	AD6634AS Min	Typ	Max	Units
MODE INM Write Timing:							
t_{SC}	Control[3] to ↑CLK Setup Time	Full	IV	5.5			ns
t_{HC}	Control[3] to ↑CLK Hold Time	Full	IV	1.0			ns
t_{HWR}	/WR(RW) to RDY(/DTACK) Hold Time	Full	IV	8.0			ns
t_{SAM}	Address/Data to /WR(RW) Setup Time	Full	IV	-0.5			ns
t_{HAM}	Address/Data to RDY(/DTACK) Hold Time	Full	IV	7.0			ns
t_{DRDY}	/WR(RW) to RDY(/DTACK) Delay	Full	IV	4.0			ns
t_{ACC}	/WR(RW) to RDY(/DTACK) High Delay	Full	IV	$4*t_{CLK}$	$5*t_{CLK}$	$9*t_{CLK}$	ns
MODE INM Read Timing:							
t_{SC}	Control[3] to ↑CLK Setup Time	Full	IV	4.0			ns
t_{HC}	Control[3] to ↑CLK Hold Time	Full	IV	2.0			ns
t_{SAM}	Address to /RD(/DS) Setup Time	Full	IV	0.0			ns
t_{HAM}	Address to Data Hold Time	Full	IV	7.0			ns
t_{ZD}	Data Tri-state Delay	Full	IV				ns
t_{DD}	RDY(/DTACK) to Data Delay	Full	IV				ns
t_{DRDY}	/RD(/DS) to RDY(/DTACK) Delay	Full	IV	4.0			ns
t_{ACC}	/RD(/DS) to RDY(/DTACK) High Delay	Full	IV	$8*t_{CLK}$	$10*t_{CLK}$	$13*t_{CLK}$	ns

MICROPROCESSOR PORT, MODE MNM (MODE=1)		Temp	Test Level	AD6634AS Min	Typ	Max	Units
MODE MNM Write Timing:							
t_{SC}	Control[3] to ↑CLK Setup Time	Full	IV	5.5			ns
t_{HC}	Control[3] to ↑CLK Hold Time	Full	IV	1.0			ns
t_{HDS}	/DS(/RD) to /DTACK(RDY) Hold Time	Full	IV	8.0			ns
t_{HRW}	RW(/WR) to /DTACK(RDY) Hold Time	Full	IV	8.0			ns
t_{SAM}	Address/Data To RW(/WR) Setup Time	Full	IV	-0.5			ns
t_{HAM}	Address/Data to RW(/WR) Hold Time	Full	IV	7.0			ns
t_{DDTACK}	/DS(/RD) to /DTACK(RDY) Delay	Full	IV				ns
t_{ACC}	RW(/WR) to /DTACK(RDY) Low Delay	Full	IV	$4*t_{CLK}$	$5*t_{CLK}$	$9*t_{CLK}$	ns
MODE MNM Read Timing:							
t_{SC}	Control[3] to ↑CLK Setup Time	Full	IV	4.0			ns
t_{HC}	Control[3] to ↑CLK Hold Time	Full	IV	2.0			ns
t_{HDS}	/DS(/RD) to /DTACK(RDY) Hold Time	Full	IV	8.0			ns
t_{SAM}	Address to /DS(/RD) Setup Time	Full	IV	0.0			ns
t_{HAM}	Address to Data Hold Time	Full	IV	7.0			ns
t_{ZD}	Data Tri-State Delay	Full	IV				ns
t_{DD}	/DTACK(RDY) to Data Delay	Full	IV				ns
t_{DDTACK}	/DS(/RD) to /DTACK(RDY) Delay	Full	IV				ns
t_{ACC}	/DS(/RD) to /DTACK(RDY) Low Delay	Full	IV	$8*t_{CLK}$	$10*t_{CLK}$	$13*t_{CLK}$	ns

[1]All Timing Specifications valid over VDD range of 2.375V to 2.675V and VDDIO range of 3.0V to 3.6V.
[2]The timing parameters for SCLK, SDFS, SDFE, SDO, SDI, and DR apply to all four channels (0, 1, 2, and 3)
[3]Specification pertains to control signals: RW, (/WR), /DS, (/RD), /CS
[4](C_{LOAD}=40pF on all outputs unless otherwise specified)
Specifications subject to change without notice

TIMING DIAGRAMS

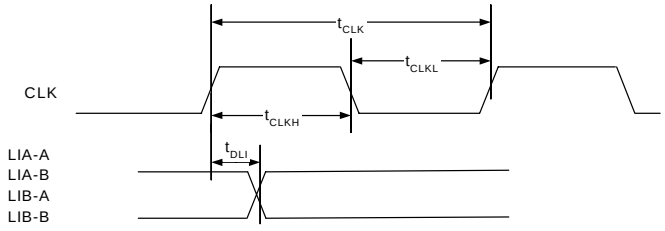


Figure 3. Level Indicator Output Switching Characteristics.

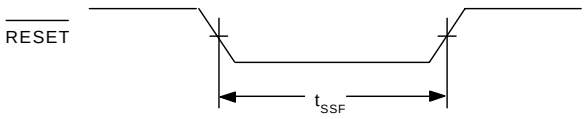


Figure 4. Reset Timing Requirements

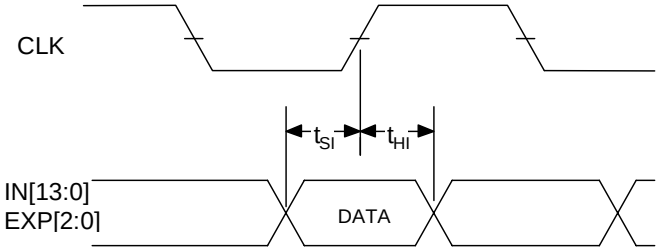


Figure 5. Input Data Timing Requirements

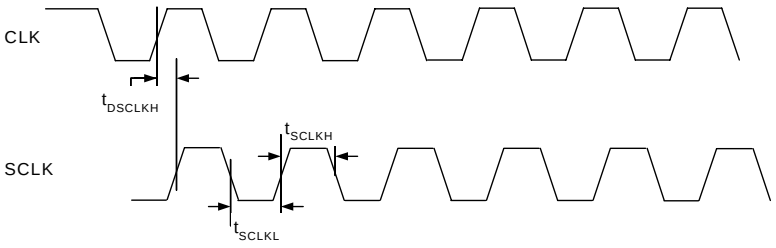


Figure 6. SCLK Switching Characteristics (Divide by 1)

TIMING DIAGRAMS

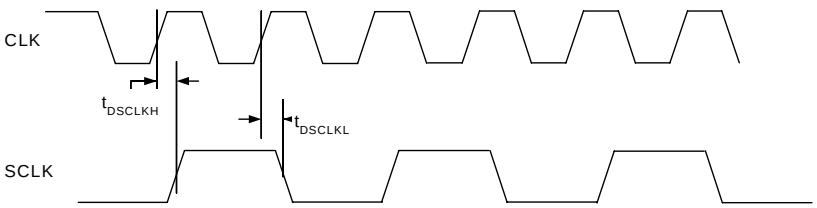


Figure 7. SCLK Switching Characteristics (Divide by 2 or EVEN integer)

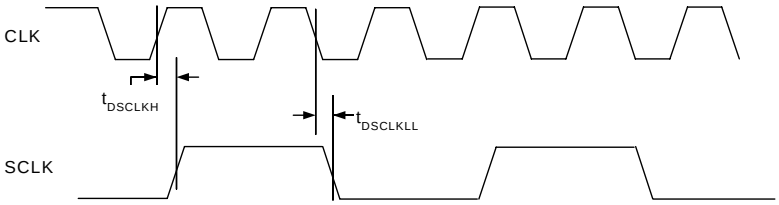


Figure 8. SCLK Switching Characteristics (Divide by 3 or ODD integer)

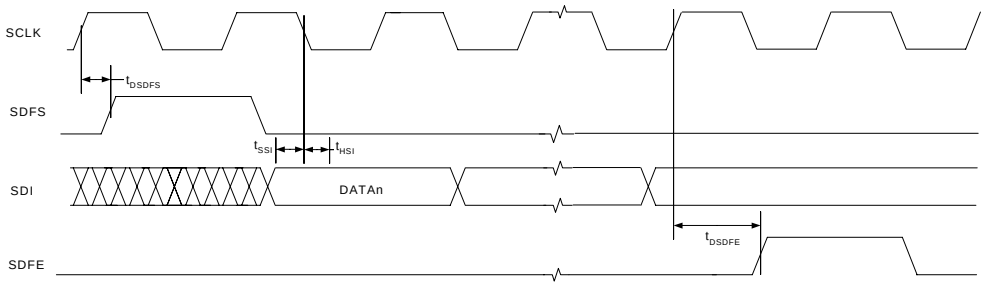


Figure 9. Serial Port Switching Characteristics

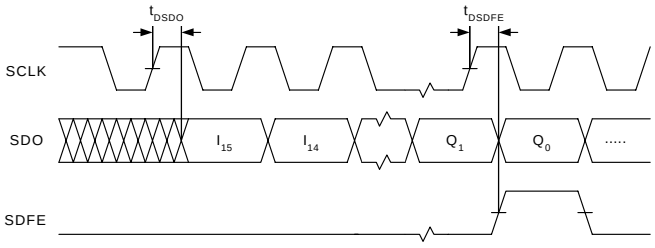


Figure 10. SDO, SDFE Switching Characteristics

TIMING DIAGRAMS

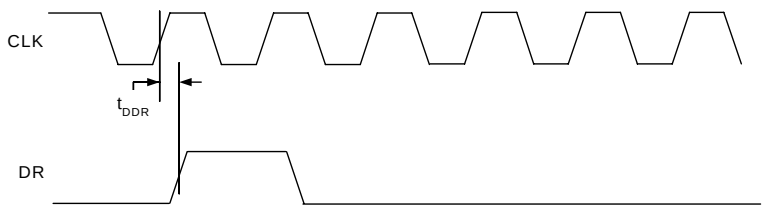


Figure 11. CLK, DR Switching Characteristics

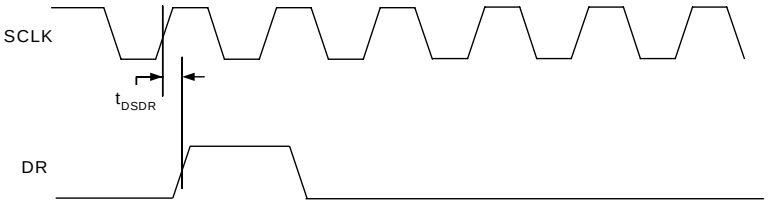


Figure 12. SCLK, DR Switching Characteristics

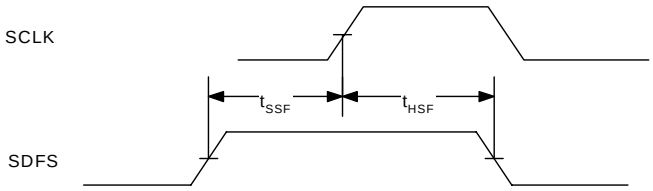


Figure 13. SDFS Timing Requirements (SBM=0)

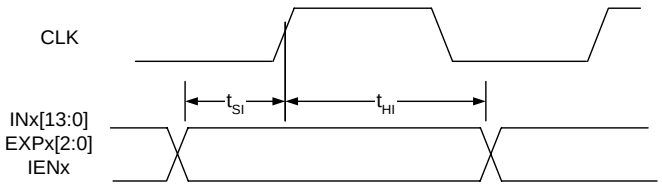


Figure 14. Input Timing for A and B Channels

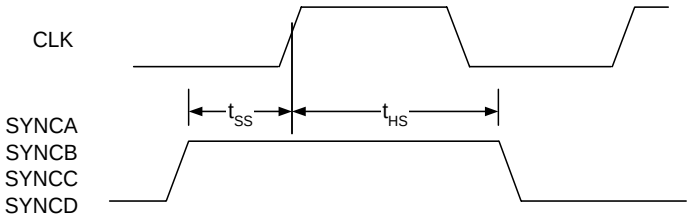


Figure 15. SYNC Timing Inputs

TIMING DIAGRAMS

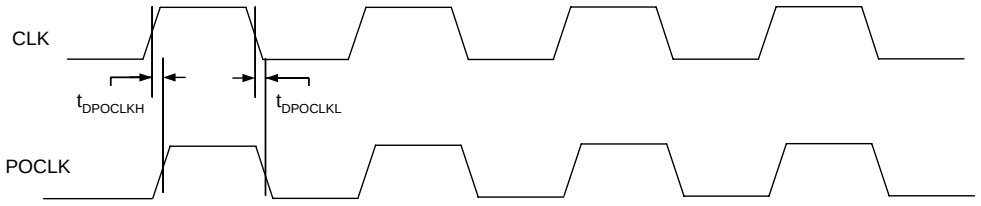


Figure 16. POCLK to CLK Switching Characteristics Divide by 1

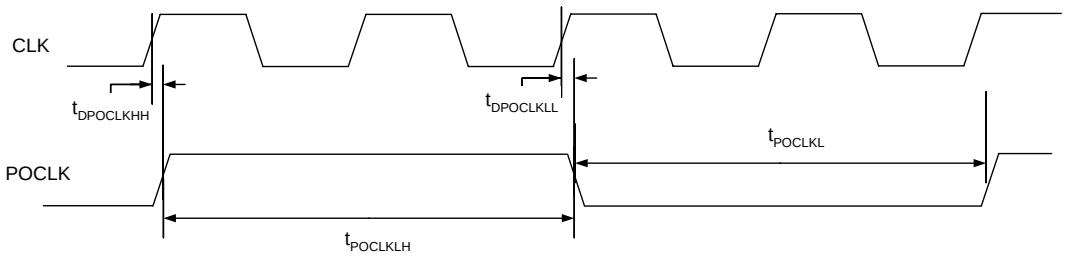


Figure 17. POCLK to CLK Switching Characteristics Divide by 2,4, or 8

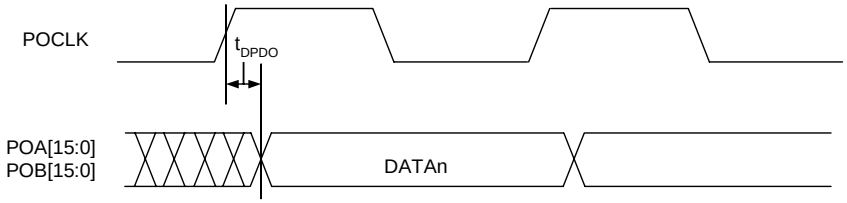


Figure 18. POA, POB Switching Characteristics

TIMING DIAGRAMS – INM Microport Mode

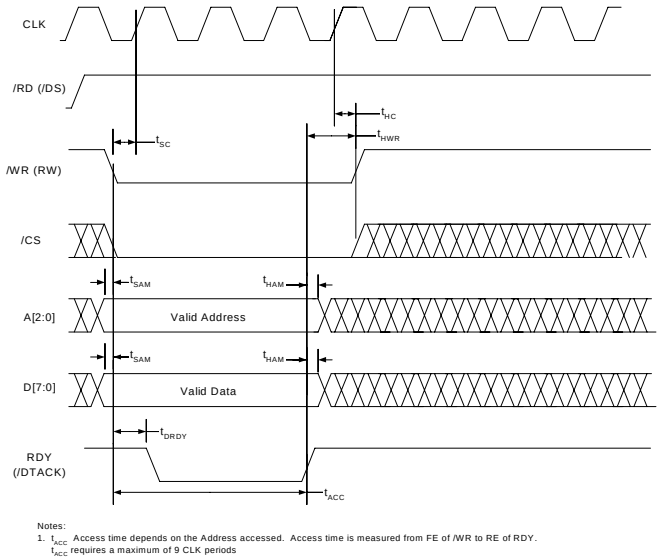


Figure 16. INM Microport Write Timing Requirements.

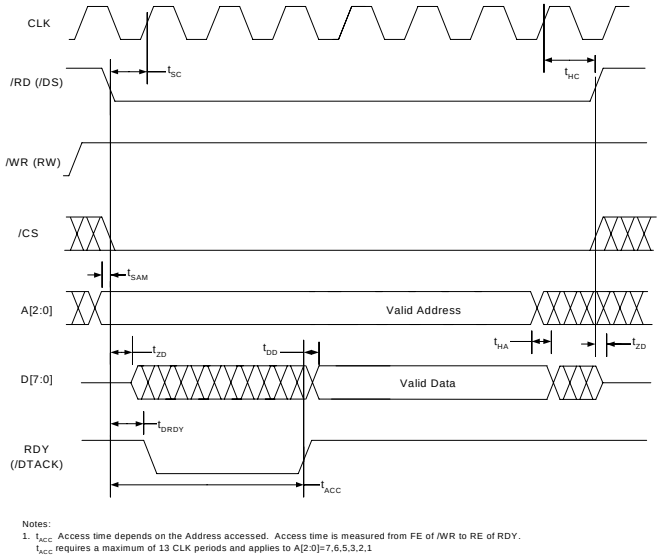


Figure 17. INM Microport Read Timing Requirements.

TIMING DIAGRAMS – MNM Microport Mode

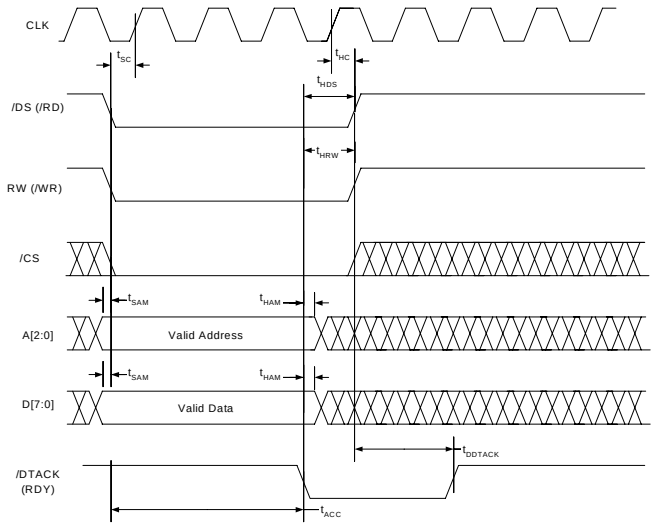


Figure 18. MNM Microport Write Timing Requirements.

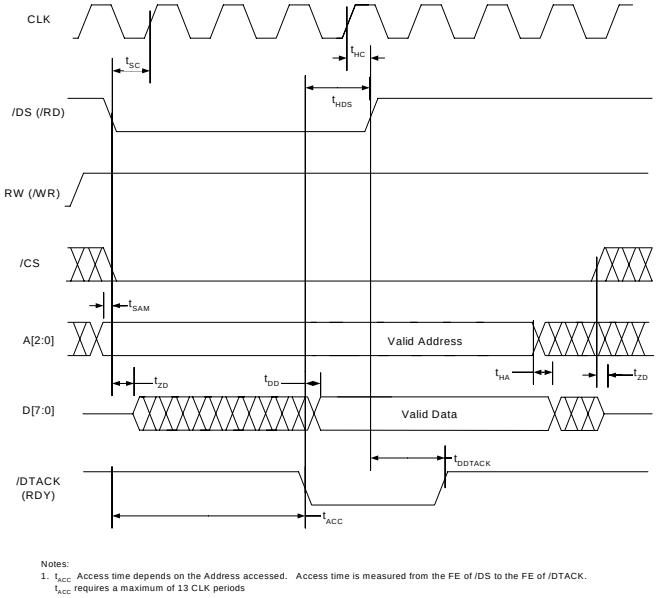
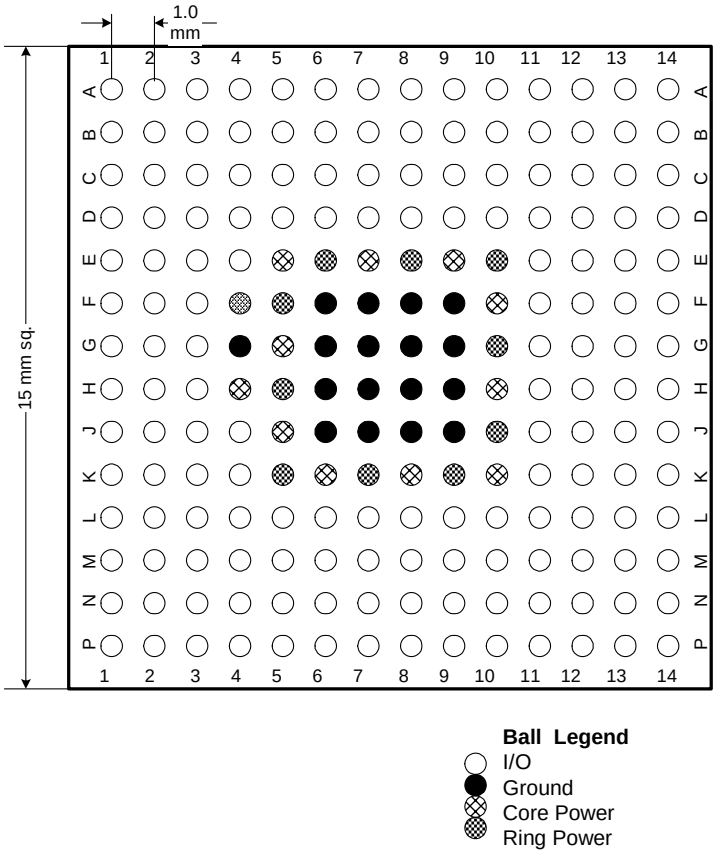


Figure 19. MNM Microport Read Timing Requirements.

PIN CONFIGURATION

196 Lead BGA (15mm x 15mm) Top View



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	No Connect	No Connect	INB5	INB6	No Connect	INB12	EXPB1	EXPB0	SDIN3 PB15	SDFS3 PB12	PBREQ DR2	LB5 PB5	SDFS2 LB1 PB1	No Connect	A
B	INB3	No Connect	No Connect	INB4	INB7	INB10	INB13	PBACK DR3	SD03 PB14	SDFE2 PB11	SDO2 PB8	LB4 PB4	LB0 PB0	No Connect	B
C	INB1	No Connect	No Connect	INB8	No Connect	INB9	INB11	EXPB2	SDFE3 PB13	SCLK3 PB10	SDIN2 LB7 PB7	SCLK2 LB3 PB3	PBIQ	SDFE1 PCLK	C
D	LIB-B	INB2	INB0	No Connect	No Connect	No Connect	PAL/SER	LBCLKIN PBCH1	LBCLKOUT PBCH0	PB9	LB6 PB6	SDFS1 LB2 PB2	PAACK DR1	SDIN1 PAIQ	D
E	CLK	IENB	LIB-A	No Connect	**VDDIO**	**VDD**	**VDDIO**	**VDD**	**VDDIO**	**VDD**	No Connect	No Connect	SDO1 PA15	POA14	E
F	EXPA1	EXPA0	EXPA2	**VDDIO**	**VDD**	**GND**	**GND**	**GND**	**GND**	**VDDIO**	No Connect	SCLK1 PA13	PAREQ DR0	SDIN0	F
G	INA12	INA13	INA10	**GND**	**VDDIO**	**GND**	**GND**	**GND**	**GND**	**VDD**	No Connect	SDFE0 PA12	SDO0 PA11	SCLK0	G
H	INA11	INA9	INA7	**VDD**	**VDD**	**GND**	**GND**	**GND**	**GND**	**VDDIO**	No Connect	SDFS0 PA10	SDIV1 PA9	SDIV0 POA8	H
J	INA8	INA6	INA4	No Connect	**VDDIO**	**GND**	**GND**	**GND**	**GND**	**VDD**	No Connect	SDIV2 LA7 PA7	SBM0 LA6 PA6	SDIV3 POA5	J
K	INA5	INA2	INA0	No Connect	**VDD**	**VDDIO**	**VDD**	**VDDIO**	**VDD**	**VDDIO**	No Connect	CHIP_ID1	CHIP_ID3	CHIP_ID0	K
L	INA1	No Connect	INA3	No Connect	No Connect	No Connect	No Connect	No Connect	LACLKOUT PCHA0	LA0 PA0	No Connect	TDI	TMS	CHIP_ID2	L
M	IENA	No Connect	No Connect	SYNCD	SYNCA	D5	D2	/DS(/RD)	LACLKIN PCHA1	A0	MODE	/TRST	No Connect	TDO	M
N	No Connect	No Connect	No Connect	LIA-A	SYNCC	D7	D4	D1	/DTACK(RDY)	A2	/CS	LA2 PA2	LA4 PA4	TCLK	N
P	No Connect	LIA-B	No Connect	SYNCB	/RESET	D6	No Connect	D3	D0	R/W(/WR)	A1	LA1 PA1	L3 PA3	No Connect	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PIN FUNCTIONS

Name	Type	Function
POWER SUPPLY		
VDD	P	2.5V Supply
VDDIO	P	3.3V IO Supply
GND	G	Ground
INPUTS		
[1]INA[13:0]	I	A Input Data (Mantissa)
[1]EXPA[2:0]	I	A Input Data (Exponent)
[2]IENA	I	Input Enable – Input A
[1]INB[13:0]	I	B Input Data (Mantissa)
[1]EXPB[2:0]	I	B Input Data (Exponent)
[2]IENB	I	Input Enable – Input B
/RESET	I	Active Low Reset Pin
CLK	I	Input Clock
PCLK	I/O	Link/Parallel Port Clock
LACLKIN	I	Link Port A Data Ready
LBCLKIN	I	Link Port B Data Ready
[1]SYNCA	I	All Sync pins go to all four output channels
[1]SYNCB	I	All Sync pins go to all four output channels
[1]SYNCC	I	All Sync pins go to all four output channels
[1]SYNCD	I	All Sync pins go to all four output channels
[1]SDIN0	I	Serial Data Input – Channel 0
[1]SDIN1	I	Serial Data Input – Channel 1
[1]SDIN2	I	Serial Data Input – Channel 2
[1]SDIN3	I	Serial Data Input – Channel 3
[1]/CS	I	Chip Select
[1]CHIP_ID[3:0]	I	Chip ID Selector
CONTROL		
[1]SBM0	I	Serial Bus Master – Channel 0 only
[1]SCLK0	I/O	Bi-directional Serial Clock – Channel 0
[1]SCLK1	I/O	Bi-directional Serial Clock – Channel 1
[1]SCLK2	I/O	Bi-directional Serial Clock – Channel 2
[1]SCLK3	I/O	Bi-directional Serial Clock – Channel 3
[1]SDIV[3:0]	I	Serial Clock Divisor – Channel 0
[1]SDFS0	I/O	Bi-directional Serial Data Frame Sync – Channel 0
[1]SDFS1	I/O	Bi-directional Serial Data Frame Sync – Channel 1
[1]SDFS2	I/O	Bi-directional Serial Data Frame Sync – Channel 2
[1]SDFS3	I/O	Bi-directional Serial Data Frame Sync – Channel 3
SDFE0	O	Serial Data Frame End – Channel 0
SDFE1	O	Serial Data Frame End – Channel 1
SDFE2	O	Serial Data Frame End – Channel 2
SDFE3	O	Serial Data Frame End – Channel 3
PAACK	I	Parallel Port A Acknowledge
PAREQ	O	Parallel Port A Request
PBACK	I	Parallel Port B Acknowledge
PBREQ	O	Parallel Port B Request
[1]PAR/SER	I	Parallel or Serial Output Port Select

PIN FUNCTIONS Continued

Name	Type	Function
MICROPORT CONTROL		
D[7:0]	I/O/T	Bi-directional Microport Data
A[2:0]	I	Microport Address Bus
/DS(/RD)	I	Active Low Data Strobe (Active Low Read)
[2]/DTACK(RDY)	O/T	Active Low Data Acknowledge (Microport Status Bit)
RW (/WR)	I	Read Write (Active Low Write)
MODE	I	Intel or Motorola mode select
OUTPUTS		
LIA-A	O	Level Indicator – Input A, Interleaved-Data A
LIA-B	O	Level Indicator – Input A, Interleaved-Data B
LIB-B	O	Level Indicator – Input B, Interleaved-Data B
LIB-A	O	Level Indicator – Input B, Interleaved-Data A
[1]SDO0	O/T	Serial Data Output – Channel 0
[1]SDO1	O/T	Serial Data Output – Channel 1
[1]SDO2	O/T	Serial Data Output – Channel 2
[1]SDO3	O/T	Serial Data Output – Channel 3
DR0	O	Output Data Ready Indicator – Channel 0
DR1	O	Output Data Ready Indicator – Channel 1
DR2	O	Output Data Ready Indicator – Channel 3
DR3	O	Output Data Ready Indicator – Channel 3
LACLKOUT	O	Link Port A Clock Output
LBCLKOUT	O	Link Port B Clock Output
LA[7:0]	O	Link Port A Output Data
LB[7:0]	O	Link Port B Output Data
PA[15:0]	O	Parallel Output Data Port A
PB[15:0]	O	Parallel Output Data Port B
PACH[1:0]	O	Parallel Output Port A Channel Indicator
PBCH[1:0]	O	Parallel Output Port B Channel Indicator
PAIQ	O	Parallel Port A I/Q Data Indicator
PBIQ	O	Parallel Port B I/Q Data Indicator
JTAG & BIST		
[2]/TRST	I	Test Reset Pin
[1]TCLK	I	Test Clock Input
[2]TMS	I	Test Mode Select Input
TDO	O/T	Test Data Output
[2]TDI	I	Test Data input

[1]Pins with a Pull-Down resistor of nominal 70K ohms
[2]Pins with a Pull-Up resistor of nominal 70K ohms

EXAMPLE FILTER RESPONSE

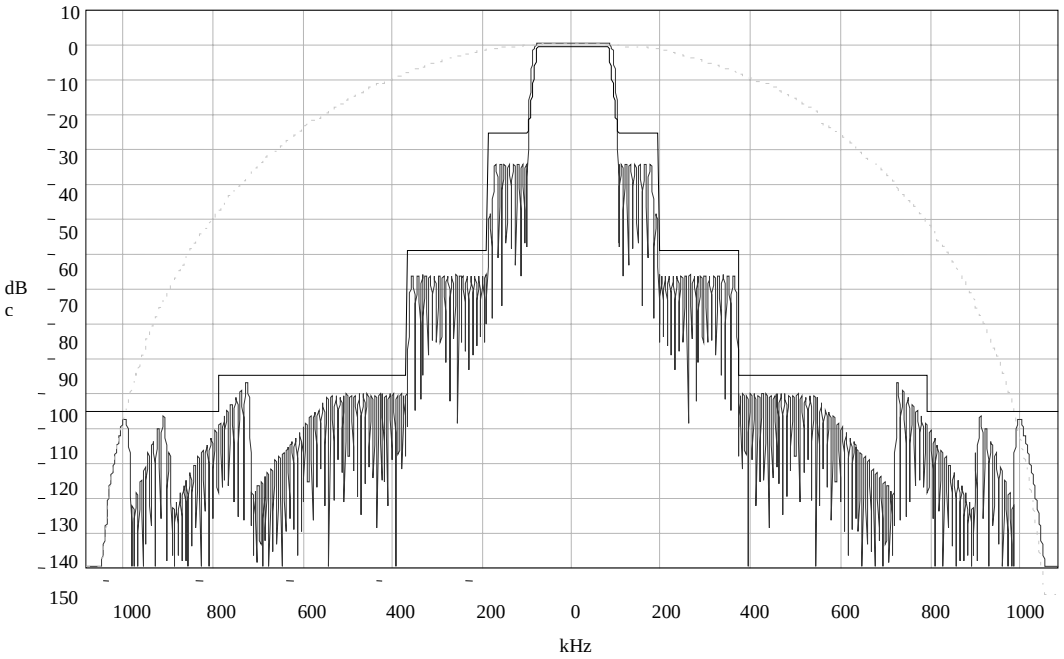


Figure 20. The filter above is based on a 65 MSPS input data rate and an output rate of 541.6666 kSPS (2 samples per symbol for EDGE). Total decimation rate is 120 distributed between the rCIC2, CIC5 and RCF.

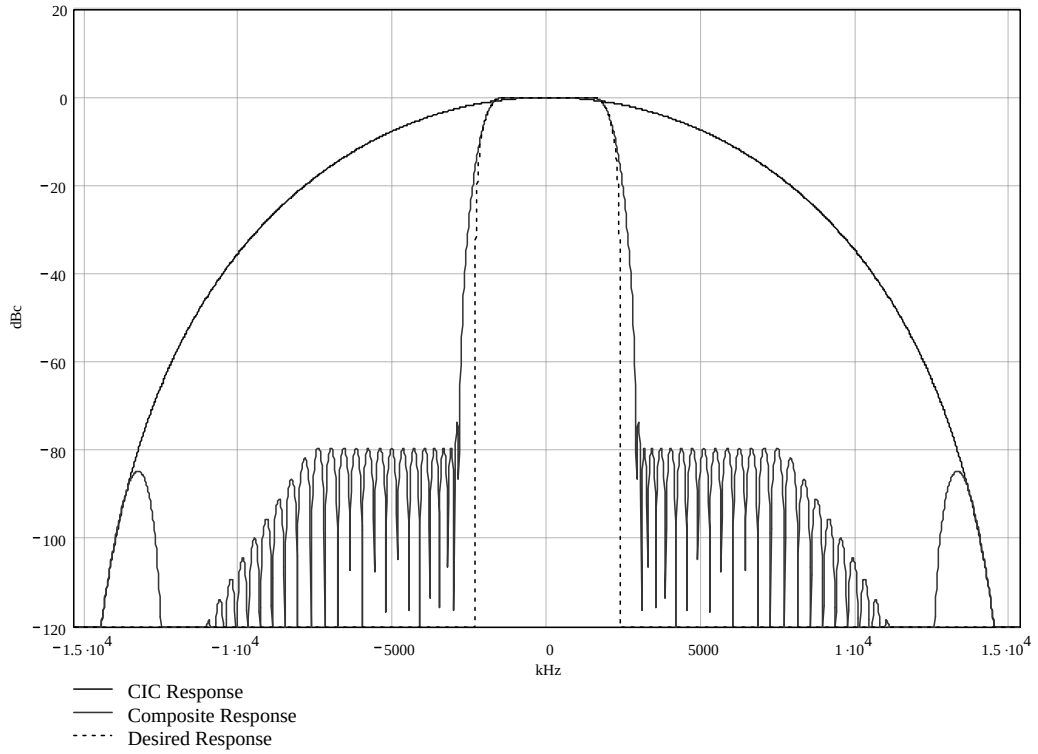


Figure 21. The filter above is designed to meet the UMTS specifications. For this configuration, the clock is set to 76.8 MSPS with 20x chip rate (3.84MCPS) and a 2x output data rate of 7.68MCPS using two channels of the AD6634.

INPUT DATA PORTS

The AD6634 features dual high speed ADC input ports, input port A and input port B. The dual input ports allow for the most flexibility with a single tuner chip. These can be diversity inputs or truly independent inputs such as separate antenna segments. Either ADC port can be routed to one of four tuner channels. For added flexibility, each input port can be used to support multiplexed inputs such as found on the AD6600 or other ADCs with mux'ed outputs. This added flexibility can allow for up to 4 different analog sources to be processed simultaneously by the four internal channels.

In addition, the front end of the AD6634 contains circuitry that enables high speed signal level detection and control. This is accomplished with a unique high speed level detection circuit that offers minimal latency and maximum flexibility to control up to four analog signal paths. The overall signal path latency from input to output on the AD6634 can be expressed in high speed clock cycles. The equation below can be used to calculate the latency.

$$T_{latency} = M_{rCIC2}\left(M_{CIC5} + 7\right) + N_{taps} + 4\left(SDIV + 1\right) + 18$$

M_{rCIC2} and M_{CIC5} are decimation values for the rCIC2 and CIC5 filters respectively, N_{taps} is the number RCF taps chosen, and SDIV is the chosen SCLK divisor factor.

Input Data Format
Each input port consists of a 14-bit mantissa and 3-bit exponent. If interfacing to a standard ADC is required, the exponent bits can be grounded. If connected to a floating point ADC such as the AD6600, then the exponent bits from that product can be connected to the input exponent bits of the AD6634. The mantissa data format is two's complement and the exponent is unsigned binary.

Input Timing
The data from each high-speed input port is latched on the rising edge of CLK. This clock signal is used to sample the input port and clock the synchronous signal processing stages that follow in the selected channels.

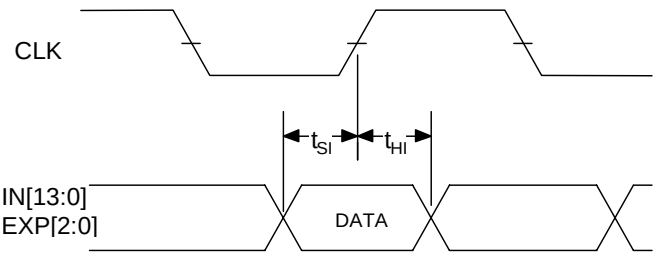


Figure 22. Input Data Timing Requirements

The clock signals can operate up to 80 MHz and have a 50% duty cycle. In applications using high speed ADCs, the ADC sample clock or data valid strobe is typically used to clock the AD6634.

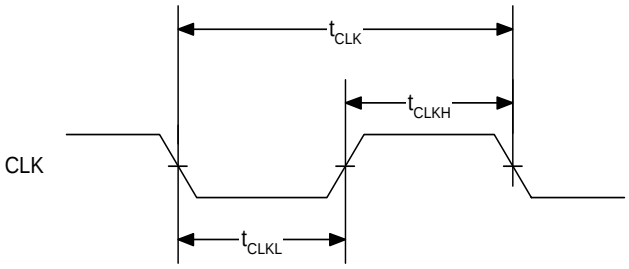


Figure 23. CLK Timing Requirements

Input Enable Control
There is an IENA and an IENB pin for the Input Port A and Input Port B respectively. There are four modes of operation using for each IEN pin. Using these modes, it is possible to emulate operation of the other RSPs such as the AD6620, which offer dual channel modes normally associated with diversity operations. These modes are: IEN transition to Low, IEN transition to High, IEN High and Blank on IEN low.

In the IEN High mode, the inputs and normal operations occur when the Input Enable is High. In the IEN transition to Low mode, normal operations occur on the first rising edge of the clock after the IEN transitions to Low. Likewise in the IEN transition to High mode, operations occur on the rising edge of the clock after the IEN transitions to High. See the **Numerically Controlled Oscillator** section for more details on configuring the Input Enable Modes. In Blank on IEN low mode, the input data is interpreted as zero when IEN is low.

A typical application for this feature would be to take the data from an AD6600 Diversity ADC to one of the inputs of the AD6634. The A/B_OUT from that chip would be tied to the IEN. Then one channel within the AD6634 would be set so that IEN transition to Low is enabled. Another channel would be configured so that IEN transition to High is enabled. One of the serial outputs would be configured as the Serial Bus Master and the other as a serial bus slave and the output bus configured as shown in Figure 26. This would allow two of the AD6634 channels to be configured to emulate that AD6620 in diversity mode. Of course the NCO frequencies and other channel characteristics would need to be set similarly, but this feature allows the AD6634 to handle interleaved data streams such as found on the AD6600.

The difference between the IEN transition to high and the IEN high is found when a system clock is provided that is higher than the data rate of the converter. It is often advantageous to supply a clock that runs faster than the data

rate so that additional filter taps can be computed. This naturally provides better filtering. In order to ensure that other parts of the circuit properly recognize the faster clock in the simplest manner, the IEN transition to low or high should be used. In this mode, only the first clock edge that meets the setup and hold times will be used to latch and process the input data. All other clocks pulses are ignored by front end processing. However, each clock cycle will still produce a new filter computation pair.

Gain Switching

The AD6634 includes circuitry that is useful in applications where either large dynamic ranges exist or where gain ranging converters are employed. This circuitry allows digital thresholds to be set such that an upper and a lower threshold can be programmed.

One such use of this may be to detect when an ADC converter is about to reach full-scale with a particular input condition. The results would be to provide a flag that could be used to quickly insert an attenuator that would prevent ADC overdrive. If 18 dB (or any arbitrary value) of attenuation (or gain) is switched in, then the signal dynamic range of the system will have been increased by 18 dB. The process begins when the input signal reaches the upper-programmed threshold. In a typical application, this may be set 1 dB (user definable) below full-scale. When this input condition is met, the appropriate LI (LIA-A, LIA-B, LIB-A or LIB-B) signal associated with either the A or B input port is made active. This can be used to switch the gain or attenuation of the external circuit. The LI line stays active until the input condition falls below the lower programmed threshold. In order to provide hysterisis, a dwell time register (see Memory Map for Input Control Registers) is available to hold off switching of the control line for a predetermined number of clocks. Once the input condition is below the lower threshold, the programmable counter begins counting high-speed clocks. As long as the input signal stays below the lower threshold for the number of high-speed clock cycles programmed, the attenuator will be removed on the terminal count. However, if the input condition goes above the lower threshold with the counter running, it will be reset and must fall below the lower threshold again to initiate the process. This will prevent un-necessary switching between states.

This is illustrated in the drawing below. When the input signal goes above the upper threshold, the appropriate LI signal becomes active. Once the signal falls below the lower threshold, the counter begins counting. If the input condition goes above the lower threshold, the counter is reset and starts again as shown in the drawing below. Once the counter has terminated to 0, the LI line goes inactive.

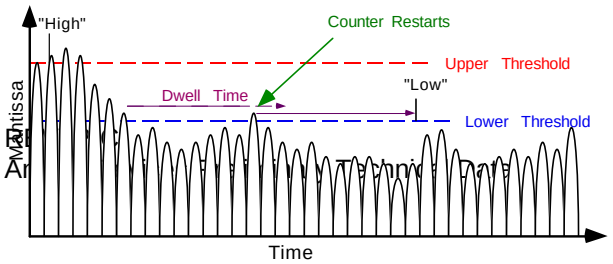


Figure 24. Threshold Settings for LI

The LI line can be used for a variety of functions. It can be used to set the controls of an attenuator, DVGA or integrated and used with an analog VGA. To simplify the use of this feature, the AD6634 includes two separate gain settings, one when this line is inactive (rCIC2_QUIET[4:0]) and the other when active (rCIC2_LOUD[4:0]). This allows the digital gain to be adjusted to the external changes. In conjunction with the gain setting, a variable hold-off is included to compensate for the pipeline delay of the ADC and the switching time of the gain control element. Together, these two features provide seamless gain switching.

Another use of this pin is to facilitate a gain range hold off within a gain ranging ADC. For converters that use gain ranging to increase total signal dynamic range, it may be desirable to prohibit internal gain ranging from occurring in some instances. For such converters, the LI (A or B) line can be used to hold this off. For this application, the upper threshold would be set based on similar criterion. However, the lower threshold would be set to a level consistent with the gain ranges of the specific converter. Then the hold off delay can be set appropriately for any of a number of factors such as fading profile, signal peak to average ratio or any other time based characteristics that might cause un-necessary gain changes.

Since the AD6634 has a total of 4 gain control circuits which can be used if both A and B input ports have interleaved data . Each respective LI pin is independent and can be set to different set points. It should be noted that the gain control circuits are wideband and are implemented prior to any filtering elements to minimize loop delay. Any of the 4 channels can be set to monitor any of the possible 4 input channels (two in normal mode and 4 when the inputs are time multiplexed).

The chip also provides appropriate scaling of the internal data based on the attenuation associated with the LI signal. In this manner, data to the DSP maintains a correct scale value throughout the process, making it totally independent. Since there often are finite delays associated with external gain switching components, the AD6634 includes a variable pipeline delay that can be used to compensate for external pipeline delays or gross settling times associated with gain/attenuator devices. This delay may be set up to 7 high-speed clocks. These features ensure smooth switching between gain settings.

Input Data Scaling

The AD6634 has two data input ports an A input port and a B input port. Each accepts 14-bit mantissa (two's complement integer) IN[13:0], a 3-bit exponent (unsigned integer) EXP[2:0] and the Input Enable(IEN). Both inputs are clocked by CLK. These pins allow direct interfacing to both standard fixed-point ADCs such as the AD9225 and

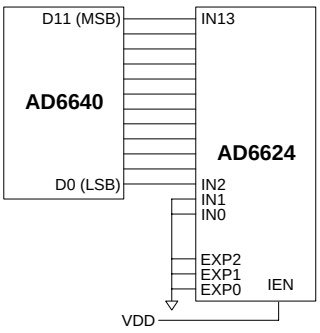
AD6640, as well as to gain-ranging ADCs such as the AD6600. For normal operation with ADCs having fewer than 14 bits, the active bits should be MSB justified and the unused LSBs should be tied low.

The 3-bit exponent, EXP[2:0] is interpreted as an unsigned integer. The exponent will subsequently be modified by either of the 5-bit scale values stored in register x92 bits 4-0 or bits 9-5. These 5 bit registers contain the sum of the rCIC2 scale value plus the external attenuator scale settings plus the Exponent Offset (ExpOff). If no external attenuator is used, these values can be set to only the value of the rCIC2 scale. If an external attenuator is used, bit position 4-0 (register 0x92 rCIC2_LOUD[4:0]) contains the scale value for the largest input range. Bit positions 9-5 (register 0x92 rCIC2_QUIET[4:0]) are used for the non-attenuated input signal range.

Scaling with fixed-point ADCs

For fixed-point ADCs the AD6634 exponent inputs, EXP[2:0] are typically not used and should be tied low. The ADC outputs are tied directly to the AD6634 Inputs, MSB-justified. The ExpOff bits in 0x92 should be programmed to 0. Likewise, the Exponent Invert bit should be 0.

Thus for fixed-point ADCs, the exponents are typically static and no input scaling is used in the AD6634.



(ExpOff = 0, ExpInv = 0)

Figure 25. Typical Interconnection of the AD6640 fixed point ADC and the AD6634.

Scaling with floating-point or gain ranging ADCs

An example of the exponent control feature combines the AD6600 and the AD6634. The AD6600 is an 11-bit ADC with 3-bits of gain ranging. In effect, the 11-bit ADC provides the mantissa, and the 3-bits of relative signal strength indicator (RSSI) for the exponent. Only five of the eight available steps are used by the AD6600. See the AD6600 data sheet for additional details.

For gain-ranging ADCs such as the AD6600,

$$scaled\_input = IN \cdot 2^{-\mathrm{mod}(7-Exp+rCIC2,8)}, ExpInv = 1,$$

ExpWeight=0

where: IN is the value of IN[13:0], Exp is the value of EXP[2:0], and rCIC2 is the rCIC scale register value (0x92 bits 9-5 and 4-0).

The RSSI output of the AD6600 numerically grows with increasing signal strength of the analog input (RSSI = 5 for a large signal, RSSI=0 for a small signal). When the Exponent Invert Bit (ExpInv) is set to zero, the AD6634 will consider the smallest signal at the IN[13:0] to be the largest and as the EXP word increases, it shifts the data down internally (EXP = 5 will shift an 14 bit word right by 5 internal bits before passing the data to the rCIC2). In this example where ExpInv=0, the AD6634 regards the largest signal possible on the AD6600 as the smallest signal. Thus, we can use the Exponent Invert Bit to make the AD6634 exponent agree with the AD6600 RSSI. By setting ExpInv=1, this forces the AD6634 to shift the data up (left) for growing EXP instead of down. The exponent invert bit should always be set high for use with the AD6600.

The Exponent Offset is used to shift the data up. For example, Table 2_1 shows that with no rCIC2 scaling, 12 dB of range is lost when the ADC input is at the largest level. This is undesired because this lowers the Dynamic Range and SNR of the system by reducing the signal of interest relative to the quantization noise floor.

To avoid this automatic attenuation of the full-scale ADC signal the ExpOff is used to move the largest signal (RSSI = 5) up to the point where there is no down shift. In other words, once the Exponent Invert bit has been set, the Exponent Offset should be adjusted so that mod(7-5 + ExpOff,8) = 0. This is the case when Exponent Offset is set to 6 since mod(8,8) = 0. Table 2_2 illustrates the use of ExpInv and ExpOff when used with the AD6600 ADC.

ADC INPUT LEVEL	AD6600 RSSI[2:0]	AD6634 DATA	SIGNAL REDUCTION
LARGEST	101 (5)	/4 (>> 2)	-12 dB
	100 (4)	/8 (>>3)	-18 dB
	011 (3)	/16 (>> 4)	-24 dB
	010 (2)	/32 (>> 5)	-30 dB
	001 (1)	/64 (>> 6)	-36 dB
SMALLEST	000 (0)	/128(>> 7)	-42 dB

(ExpInv = 1, rCIC2 Scale = 0)

Table 2_1. AD6600 transfer function with AD6634 ExpInv = 1, and no ExpOff.

ADC INPUT LEVEL	AD6600 RSSI[2:0]	AD6634 DATA	SIGNAL REDUCTION
LARGEST	101 (5)	/ 1 (>> 0)	-0 dB
	100 (4)	/ 2 (>> 1)	-6 dB
	011 (3)	/ 4 (>> 2)	-12 dB
	010 (2)	/ 8 (>> 3)	-18 dB

	001 (1)	/ 16 (>> 4)	-24 dB
SMALLEST	000 (0)	/ 32 (>> 5)	-30 dB

(ExpInv = 1, ExpOff = 6, ExpWeight = 0)

Table 2_2. AD6600 transfer function with AD6620 ExpInv = 1, and ExpOff = 6.

This flexibility in handling the exponent allows the AD6634 to interface with other gain ranging ADCs besides the AD6600. The Exponent Offset can be adjusted to allow up to 7 RSSI(EXP) ranges to be used as opposed to the AD6600s 5. It also allows the AD6634 to be tailored in a system that employs the AD6600 but does not utilize all of its signal range. For example if only the first 4 RSSI ranges are expected to occur then the ExpOff could be adjusted to 5 which would then make RSSI = 4 correspond to the 0 dB point of the AD6634.

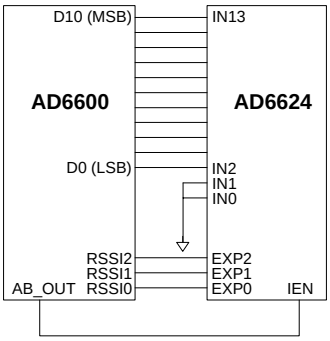


Figure 26. Typical Interconnection of the AD6600 gain-ranging ADC and the AD6634.

NUMERICALLY CONTROLLED OSCILLATOR

Frequency Translation
This processing stage comprises a digital tuner consisting of two multipliers and a 32-bit complex NCO. Each channel of the AD6634 has an independent NCO. The NCO serves as a quadrature local oscillator capable of producing a NCO frequency between –CLK/2 and +CLK/2 with a resolution of $CLK/2^{32}$ in the complex mode. The worst-case spurious signal from the NCO is better than -100dBc for all output frequencies.

The NCO frequency value in registers 0x85 and 0x86 are interpreted as a 32-bit unsigned integer. The NCO frequency is calculated using the equation below.

$$NCO\_FREQ = 2^{32} * \mathrm{mod}(\frac{f_{channel}}{CLK})$$

where:
NCO_FREQ is the 32-bit integer (registers 0x85 and 0x86)
$f_{channel}$ is the desired channel frequency and
*CLK is the AD6634 master clock rate (CLK).
*See NCO Mode control Section Below

NCO Frequency Hold-Off Register
When the NCO Frequency registers are written, data is actually passed to a shadow register. Data may be moved to the main registers by one of two methods. The first is to start the chip using the soft sync feature which will directly load the NCO registers. The second allows changes to be pre-written and then updated through direct software control. To accomplish this, there is an NCO Frequency Hold-Off Counter. The counter (0x84) is a 16-bit unsigned integer and is clocked at the master CLK rate. This hold off counter is also used in conjunction with the frequency hopping feature of this chip.

Phase Offset
The phase offset register (0x87) adds an offset to the phase accumulator of the NCO. This is a 16-bit register and is interpreted as a 16-bit unsigned integer. A 0x0000 in this register corresponds to a 0 Radian offset and a 0xFFFF corresponds to an offset of 2π (1-1/(2^16)) Radians. This register allows multiple NCOs to be synchronized to produce sine waves with a known and steady phase difference.

NCO Control Register
The NCO control register located at 0x88 is used to configure the features of the NCO. These are controlled on a per channel basis. These are described below.

By-Pass
The NCO in the front end of the AD6634 can be by-passed. By-Pass mode is enabled by setting bit 0 of 0x88 high. When they are by-passed, down conversion is not performed and the AD6634 channel functions simply as a real filter on complex data. This is useful for base-band sampling application where the A input is connected to the I signal path within the filter and the B input is connected to the Q signal path. This may be desired if the digitized signal has already been converted to base-band in prior analog stages or by other digital pre-processing.

Phase Dither
The AD6634 provides a phase dither option for improving the spurious performance of the NCO. Phase Dither is enabled by setting bit 1. When phase dither is enabled by setting this bit high, spurs due to phase truncation in the NCO are randomized. The energy from these spurs is spread into the noise floor and Spurious Free Dynamic Range is increased at the expense of very slight decreases in the SNR. The choice of whether Phase Dither is used in a system will ultimately be decided by the system goals. If lower spurs are desired at the expense of a slightly raised noise floor, it should be employed. If a low noise floor is desired and the higher spurs can be tolerated or filtered by subsequent stages, then Phase Dither is not needed.

Amplitude Dither
Amplitude Dither can also be used to improve spurious performance of the NCO. Amplitude Dither is enabled by setting bit 2. Amplitude Dither improves performance by randomizing the amplitude quantization errors within the angular to Cartesian conversion of the NCO. This option may reduce spurs at the expense of a slightly raised noise floor. Amplitude Dither and Phase Dither can be used together, separately or not at all.

Clear Phase Accumulator on HOP
When bit 3 is set, the NCO phase accumulator is cleared prior to a frequency hop. This ensures a consistent phase of the NCO on each hop. The NCO phase offset is un-effected by this setting and is still in effect. If phase continuous hopping is desired, this bit should be cleared and the last phase in the NCO phase register will be the initiating point for the new frequency.

Input Enable Control
There are four different modes of operation for the input enable. Each of the high-speed input ports includes an IEN line. Any of the four filter channels can be programmed to take data from either of the two A or B input ports (See **WB Input Select** below). Along with data is the IEN(A,B) signal. Each filter channel can be configured to process the IEN signal in one of four modes. Three of the modes are associated with when data is processed based on a time division multiplexed data stream. The fourth mode is used in applications that employ time division duplex such as radar, sonar, ultrasound and communications that involve TDD.

Mode 00: Blank on IEN low
In this mode, data is blanked while the IEN line is low. During the period of time when the IEN line is high, new data is strobed on each rising edge of the input clock. When the IEN line is lowered, input data is replaced with zero values. During this period, the NCO continues to run such that when the IEN line is raised again, the NCO value will be at the value it would have otherwise been in had the IEN line never been lowered. This mode has the effect of blanking the digital inputs when the IEN line is lowered. Back end processing (rCIC2, CIC5 and RCF) continues while the IEN line is high. This mode is useful for time division multiplexed applications.

Mode 01: Clock on IEN high
In this mode, data is clocked into the chip while the IEN line is high. During the period of time when the IEN line is high, new data is strobed on each rising edge of the input clock. When IEN line is lowered, input data is no longer latched into the channel. Additionally, NCO advances are halted. However, back end processing (rCIC2, CIC5 and RCF) continues during this period. The primary use for this mode is to allow for a clock that is faster than the input sample data rate to allow more filter taps to be computed than would otherwise be possible. In the diagram below, input data is strobed only during the period of time while IEN is high despite the fact that the CLK continues to run at a rate 4 times faster than the data.

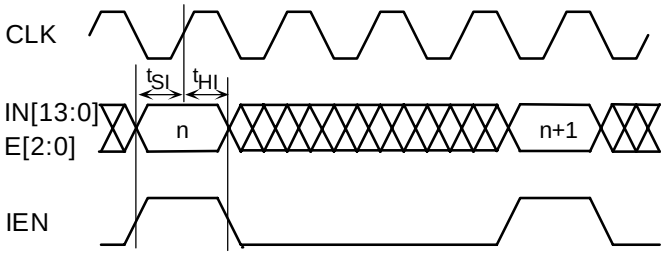


Figure 27. Fractional Rate Input Timing (4X CLK) in mode 01.

Mode 10: Clock on IEN transition to high
In this mode, data is clocked into the chip only on the first clock edge after the rising transition of the IEN line. Although data is only latched on the first valid clock edge, the back end processing (rCIC2, CIC5 and RCF) continues on each available clock that may be present, similar to Mode 01. The NCO phase accumulator is incremented only once for each new input data sample and not once for each input clock.

Mode 11: Clock on IEN transition to low
In this mode, data is clocked into the chip only on the first clock edge after the falling transition of the IEN line. Although data is only latched on the first valid clock edge, the back end processing (rCIC2, CIC5 and RCF) continues one each available clock that may be present, similar to Mode 01. The NCO phase accumulator is incremented only once for each new input data sample and not once for each input clock.

WB Input Select
Bit 6 in this register controls which input port is selected for signal processing. If this bit is set high, then input port B (INB, EXPB and IENB) is connected to the selected filter channel. If this bit is cleared, then input port A (INA, EXPA and IENA) are connected to the selected filter channel.

Sync Select
Bits 7 and 8 of this register determine which external sync pin is associated with the selected channel. The AD6634 has four sync pins named SYNCA, SYNCB, SYNCC, and SYNCD. Any of these sync pins can be associated with any of the four receiver channels within the AD6634. Additionally, if only one sync signal is required for the system, all 4 receiver channels can reference the same sync pulse. Bit value 00 is channel A, 01 is channel B, 10 is channel C and 11 is channel D.

2nd ORDER rCIC FILTER

The rCIC2 filter is a second order Cascaded re-sampling Integrator Comb filter. The resampler is implemented using a unique technique, which does not require the use of a high-speed clock, thus simplifying the design and saving power. The re-sampler allows for non-integer relationships between the master clock and the output data rate. This allows easier implementation of systems that are either multi-mode or require a master clock that is not a multiple of the data rate to be used.

Interpolation up to 512 and decimation up to 4096 is allowed in the rCIC2. The re-sampling factor for the rCIC2 (L) is a 9-bit integer. When combined with the decimation factor M, a 12-bit number, the total rate-change can be any fraction in the form of:

$$R_{rCIC2} = \frac{L}{M}$$
$$R_{rCIC2} \le 1$$

The only constraint is that the ratio L/M must be less than or equal to one. This implies that the rCIC2 decimates by 1 or more.

Re-sampling is implemented by apparently increasing the input sample rate by the factor L, using zero stuffing for the new data samples. Following the re-sampler is a second order cascaded integrator comb filter. Filter characteristics are determined only by the fractional rate-change (L/M).

The filter can process signals at the full rate of the input port 80 MHz. The output rate of this stage is given by the equation below.

$$f_{SAMP\ 2} = \frac{L_{rCIC\ 2}\, f_{SAMP}}{M_{\ rCIC\ 2}}$$

Both L_{rCIC2} and M_{rCIC2} are unsigned integers. The interpolation rate (L_{rCIC2}) may be from 1 to 512 and the decimation (M_{rCIC2}) may be between 1 and 4096. The stage can be bypassed by setting the decimation to 1/1.

The frequency response of the rCIC2 filter is given by the following equations.

$$H(z) = \frac{1}{2^{S_{rCIC2}} \cdot L_{rCIC2}} \cdot \left(\frac{1 - z^{-\frac{M_{rCIC2}}{L_{rCIC2}}}}{1 - z^{-1}} \right)^2$$

$$H(f) = \frac{1}{2^{S_{rCIC2}} \cdot L_{rCIC2}} \cdot \left(\frac{\sin\left(\pi \frac{M_{rCIC2} \cdot f}{L_{rCIC2} \cdot f_{SAMP}} \right)}{\sin\left(\pi \frac{f}{f_{SAMP}} \right)} \right)^2$$

The scale factor, S_{rCIC2} is a programmable unsigned 5 bit between 0 and 31. This serves as an attenuator that can reduce the gain of the rCIC2 in 6dB increments. For the best dynamic range, S_{rCIC2} should be set to the smallest value possible (i.e. lowest attenuation) without creating an overflow condition. This can be safely accomplished using the equation below, where *input_level* is the largest fraction of full-scale possible at the input to the AD6634 (normally 1). The rCIC2 scale factor is always used whether or not the rCIC2 is bypassed.

Moreover, there are two scale registers (rCIC2_LOUD[4:0] bits 4-0 in x92), and (rCIC2_QUIET[4:0] bits 9-5 in x92) which are used in conjunction with the computed S_{rCIC2} which determines the overall rCIC2 scaling. The S_{rCIC2} value must be summed with the values in each respective scale registers and ExpOff to determine the scale value that must be placed in the rCIC2 scale register. This number must be less than 32 or the interpolation and decimation rates must be adjusted to validate this equation. The ceil function denotes the next whole integer and the floor function denotes the previous whole integer. For example, the ceil(4.5) is 5 while the floor(4.5) is 4.

The gain and pass-band droop of the rCIC2 should be calculated by the equations above, as well as the filter transfer equations that follow. Excessive passband droop can be compensated for in the RCF stage by peaking the passband by the inverse of the roll-off.

$$S_{rCIC2} = ceil\left[\log_2\left(M_{rCIC2} + floor\left(\frac{M_{rCIC2}}{L_{rCIC2}} \right) * \left(2 * M_{rCIC2} - L_{rCIC2} * floor\left(\frac{M_{rCIC2}}{L_{rCIC2}} + 1 \right) \right) \right) \right]$$

$$OL_{CIC2} = \frac{\left(M_{rCIC2}{}^2 \right)}{L_{rCIC2} * 2^{S_{rCIC2}}} \cdot input\_level$$

$$scaled\_input = IN \cdot 2^{-\mathrm{mod}(Exp+rCIC2,8)}, ExpInv = 0$$

$$scaled\_input = IN \cdot 2^{-\mathrm{mod}(7-Exp+rCIC2,8)}, ExpInv = 1$$

where: IN is the value of IN[15:0], Exp is the value of EXP[2:0], and rCIC2 is the value of the 0x92 (rCIC2_QUIET[4:0] and rCIC2_LOUD[4:0]) scale register.

rCIC2 Rejection

The table below illustrates the amount of bandwidth in percent of the data rate into the rCIC2 stage. The data in this table may be scaled to any other allowable sample rate up to 80 MHz in Single Channel Mode or 40 MHz in Diversity Channel Mode. The table can be used as a tool to decide how to distribute the decimation between rCIC2, CIC5 and the RCF.

M_{rCIC2}/L_{rCIC2}	-50dB	-60dB	-70dB	-80dB	-90dB	-100dB
2	1.79	1.007	0.566	0.318	0.179	0.101
3	1.508	0.858	0.486	0.274	0.155	0.087
4	1.217	0.696	0.395	0.223	0.126	0.071
5	1.006	0.577	0.328	0.186	0.105	0.059
6	0.853	0.49	0.279	0.158	0.089	0.05
7	0.739	0.425	0.242	0.137	0.077	0.044
8	0.651	0.374	0.213	0.121	0.068	0.038
9	0.581	0.334	0.19	0.108	0.061	0.034
10	0.525	0.302	0.172	0.097	0.055	0.031
11	0.478	0.275	0.157	0.089	0.05	0.028
12	0.439	0.253	0.144	0.082	0.046	0.026
13	0.406	0.234	0.133	0.075	0.043	0.024
14	0.378	0.217	0.124	0.07	0.04	0.022
15	0.353	0.203	0.116	0.066	0.037	0.021
16	0.331	0.19	0.109	0.061	0.035	0.02

Table 3 SSB rCIC2 Alias Rejection Table (f_{SAMP} = 1) Bandwidth shown in percentage of $f_{SAMP.}$

Example Calculations

Goal: Implement a filter with an Input Sample Rate of 10MHz requiring 100dB of Alias Rejection for a +/- 7kHz passband.

Solution: First determine the percentage of the sample rate that is represented by the pass band.

$$BW_{fraction} = 100 * \frac{7kHz}{10MHz} = 0.07$$

Find the -100dB column on the right of the table and look down this column for a value greater than or equal to your passband percentage of the clock rate. Then look across to the extreme left column and find the corresponding rate change factor (M_{rCIC2}/L_{rCIC2}). Referring to the table, notice that for a M_{rCIC2}/L_{rCIC2} of 4, the frequency having -100dB of alias rejection is 0.071 percent, which is slightly greater than the 0.07 percent calculated. Therefore, for this example, the maximum bound on rCIC2 rate change is 4. A higher chosen M_{rCIC2}/L_{rCIC2} means less alias rejection than the 100dB required.

An M_{rCIC2}/L_{rCIC2} of less than 4 would still yield the required rejection, however, the power consumption can be minimized by decimating as much as possible in this rCIC2 stage. Decimation in rCIC2 lowers the data rate, and thus reduces power consumed in subsequent stages. It should also be noted that there is more than one way to get the decimation by 4. A decimation of 4 is the same as an L/M ratio of 0.25. Thus any integer combination of L/M that yields 0.25 will work (1/4, 2/8 or 4/16). However, for the best dynamic range, the simplest ratio should be used. For example, ¼ gives better performance than 4/16.

Decimation and Interpolation Registers

rCIC2 decimation values are stored in register 0x90. This register is a 12-bit register and contains the decimation portion less 1. The interpolation portion is stored in register 0x91. This 9-bit value holds the interpolation less one.

rCIC2 Scale

Register 0x92 contains the scaling information for this section of the circuit. The primary function is to store the scale value computed in the sections above.

Bits 4-0 (rCIC2_LOUD[4:0]) of this register are used to contain the scaling factor for the rCIC2 during conditions of strong signals. These 5 bits represent the rCIC2 scalar calculated above plus any external signal scaling with an attenuator.

Bits 9-5 (rCIC2_QUIET[4:0]) of this register are used to contain the scaling factor for the rCIC2 during conditions of weak signals. In this register, no external attenuator would be used and is not included. Only the value computed above is stored in these bits.

Bit 10 of this register is used to indicate the value of the external exponent. If this bit is set LOW, then each external exponent represents 6 dB per step as in the AD6600. If this bit is set to HIGH, each exponent represents a 12 dB step.

Bit 11 of this register is used to invert the external exponent before internal calculation. This bit should be set HIGH for gain ranging ADCs that use an increasing exponent to represent an increasing signal level. This bit should be set LOW for gain ranging ADCs that use a decreasing exponent for representing an increasing signal level.

In applications that do not require the features of the rCIC2, it may be by setting the L/M ratio to 1/1. This effectively

bypasses all circuitry of the rCIC2 except the scaling which is still effectual.

5th ORDER CIC FILTER

The third signal processing stage, CIC5, implements a sharper fixed-coefficient, decimating filter than rCIC2. The input rate to this filter is f_{SAMP2}. The maximum input rate is given by the equation below. N_{CH} equals two for Diversity Channel Real input mode; otherwise N_{CH} equals one. In order to satisfy this equation, M_{rCIC2} can be increased, N_{CH} can be reduced, or f_{CLK} can be increased (reference fractional rate input timing described in the "Input Timing" section).

$$f_{SAMP2} \le \frac{f_{CLK}}{N_{CH}}$$

The decimation ratio, M_{CIC5}, may be programmed from 2 to 32 (all integer values). The frequency response of the filter is given by the following equations. The gain and passband droop of CIC5 should be calculated by these equations. Both parameters may be compensated for in the RCF stage.

$$H(z) = \frac{1}{2^{S_{CIC5}+5}} \cdot \left(\frac{1 - z^{-M_{CIC5}}}{1 - z^{-1}} \right)^5$$

$$H(f) = \frac{1}{2^{S_{CIC5}+5}} \cdot \left(\frac{\sin\left(\pi \frac{M_{CIC5} \cdot f}{f_{SAMP2}} \right)}{\sin\left(\pi \frac{f}{f_{SAMP2}} \right)} \right)^5$$

The scale factor, S_{CIC5} is a programmable unsigned integer between 0 and 20. It serves to control the attenuation of the data into the CIC5 stage in 6dB increments. For the best dynamic range, S_{CIC5} should be set to the smallest value possible(lowest attenuation) without creating an overflow condition. This can be safely accomplished using the equation below, where OL_{rCIC2} is the largest fraction of full scale possible at the input to this filter stage. This value is output from the rCIC2 stage then pipe-lined into the CIC5.

$$S_{CIC5} = ceil\left(\log_2 \left({M_{CIC5}}^5 \cdot OL_{CIC2} \right) \right) - 5$$

$$OL_{CIC5} = \frac{\left({M_{CIC5}}^5 \right)}{2^{S_{CIC5}+5}} \cdot OL_{CIC2}$$

The output rate of this stage is given by the equation below.

$$f_{SAMP5} = \frac{f_{SAMP2}}{M_{CIC5}}$$

CIC5 Rejection

The table below illustrates the amount of bandwidth in percentage of the clock rate that can be protected with various decimation rates and alias rejection specifications. The maximum input rate into the CIC5 is 32.5MHz. As in the previous table, these are the ½ bandwidth characteristics of the CIC5. Notice that the CIC5 stage can protect a much wider band to any given rejection.

M_{CIC5}	-50dB	-60dB	-70dB	-80dB	-90dB	-100dB
2	10.227	8.078	6.393	5.066	4.008	3.183
3	7.924	6.367	5.11	4.107	3.297	2.642
4	6.213	5.022	4.057	3.271	2.636	2.121
5	5.068	4.107	3.326	2.687	2.17	1.748
6	4.267	3.463	2.808	2.27	1.836	1.48
7	3.68	2.989	2.425	1.962	1.588	1.281
8	3.233	2.627	2.133	1.726	1.397	1.128
9	2.881	2.342	1.902	1.54	1.247	1.007
10	2.598	2.113	1.716	1.39	1.125	0.909
11	2.365	1.924	1.563	1.266	1.025	0.828
12	2.17	1.765	1.435	1.162	0.941	0.76
13	2.005	1.631	1.326	1.074	0.87	0.703
14	1.863	1.516	1.232	0.998	0.809	0.653
15	1.74	1.416	1.151	0.932	0.755	0.61
16	1.632	1.328	1.079	0.874	0.708	0.572
17	1.536	1.25	1.016	0.823	0.667	0.539
18	1.451	1.181	0.96	0.778	0.63	0.509
19	1.375	1.119	0.91	0.737	0.597	0.483
20	1.307	1.064	0.865	0.701	0.568	0.459
21	1.245	1.013	0.824	0.667	0.541	0.437
22	1.188	0.967	0.786	0.637	0.516	0.417
23	1.137	0.925	0.752	0.61	0.494	0.399
24	1.09	0.887	0.721	0.584	0.474	0.383
25	1.046	0.852	0.692	0.561	0.455	0.367
26	1.006	0.819	0.666	0.54	0.437	0.353
27	0.969	0.789	0.641	0.52	0.421	0.34
28	0.934	0.761	0.618	0.501	0.406	0.328
29	0.902	0.734	0.597	0.484	0.392	0.317
30	0.872	0.71	0.577	0.468	0.379	0.306
31	0.844	0.687	0.559	0.453	0.367	0.297
32	0.818	0.666	0.541	0.439	0.355	0.287

Table 4. SSB CIC5 Alias Rejection Table (f_{SAMP2} = 1)

This table helps to calculate an upper bound on decimation, M_{CIC5}, given the desired filter characteristics.

RAM COEFFICIENT FILTER

The final signal processing stage is a sum-of-products decimating filter with programmable coefficients. A simplified block diagram is shown below. The data memories I-RAM and Q-RAM store the 160 most recent complex samples from the previous filter stage with 20-bit resolution. The coefficient memory, CMEM, stores up to 256 coefficients with 20-bit resolution. On every CLK cycle one tap for I and one tap for Q are calculated using the same coefficients. The RCF output consists of 24 bit data bits.

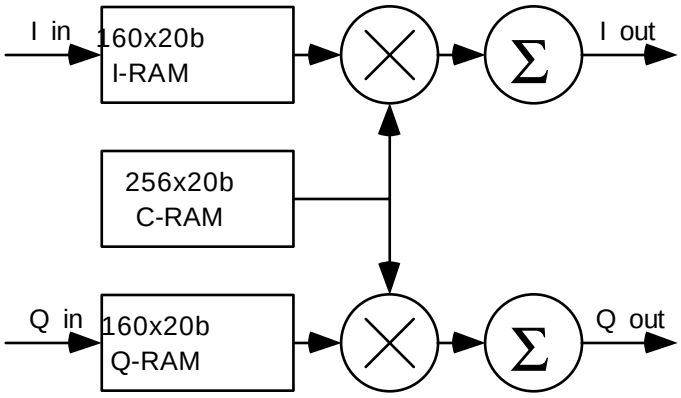


Figure 28. RAM Coefficient Filter Block Diagram

RCF Decimation Register

Each RCF channel can be used to decimate the data rate. The decimation register is an 8 bit register and can decimate from 1 to 256. The RCF decimation is stored in 0xA0 in the form of M_{RCF}-1. The input rate to the RCF is f_{SAMP5}.

RCF Decimation Phase

The RCF decimation phase can be used to synchronize multiple filters within a chip. This is useful when using multiple channels within the AD6634 to implement poly-phase filter allowing the resources of several filters to be paralleled. In such an application, two RCF filters would be processing the same data from the CIC5. However, each filter will be delayed by one half the decimation rate, thus creating a 180-degree phase difference between the two halves. The AD6634 filter channel uses the value stored in this register to pre-load the RCF counter. Therefore instead of starting from 0, the counter is loaded with this value, thus creating an offset in the processing that should be equivalent to the required processing delay. This data is stored in 0xA1 as an 8-bit number.

RCF Filter Length

The maximum number of taps this filter can calculate, N_{taps}, is given by the equation below. The value N_{taps}-1 is written to the channel register within the AD6634 at address 0xA2.

$$N_{taps} \le \min\left(\frac{f_{CLK} \cdot M_{RCF}}{f_{SAMP5}}, 160\right)$$

The RCF coefficients are located in addresses 0x00 to 0x7F and are interpreted as 20-bit 2's complement numbers. When writing the coefficient RAM, the lower addresses will be multiplied by relatively older data from the CIC5 and the higher coefficient addresses will be multiplied by relatively newer data from the CIC5. The coefficients need not be symmetric and the coefficient length, N_{taps}, may be even or odd. If the coefficients are symmetric, then both sides of the impulse response must be written into the coefficient RAM.

Although the base memory for coefficients is only 128 words long, the actual length is 256 words long. There are two pages, each of 128 words long. The page is selected by bit 8 of 0xA4. Although this data must be written in pages, the internal core handles filters that exceed the length of 128 taps. Therefore, the full length of the data RAM may be used as the filter length (160 taps).

The RCF stores the data from the CIC5 into a 160x40 RAM. 160x20 is assigned to I data and 160x20 is assigned to Q data. The RCF uses the RAM as a circular buffer, so that it is difficult to know in which address a particular data element is stored. To avoid start-up transients due to undefined data RAM values, the data RAM should be cleared upon initialization.

When the RCF is triggered to calculate a filter output, it starts by multiplying the oldest value in the data RAM by the first coefficient, which is pointed to by the RCF Coefficient Offset Register (0xA3). This value is accumulated with the products of newer data words multiplied by the subsequent locations in the coefficient RAM until the coefficient address RCF_{OFF} +N_{taps}-1 is reached.

Coefficient Address	Impulse Response	Data
0	h(0)	N(0) oldest
1	h(1)	N(1)
2 =(N_{taps} - 1)	h(2)	N(2) newest

Table 5. Three-tap Filter

The RCF Coefficient Offset register can be used for two purposes. The main purpose of this register is allow for multiple filters to loaded into memory and selected simply by changing the offset as a pointer for rapid filter changes. The other use of this register is to form part of symbol timing adjustment. If the desired filter length is padded with zeros on the ends, then the starting point can be adjusted to form slight delays in when the filter is computed with reference to the high-speed clock. This allows for vernier adjustment of the symbol timing. Course adjustments can be made with the RCF Decimation Phase.

The output rate of this filter is determined by the output rate of the CIC5 stage and M_{RCF}.

$$f_{SAMPR} = \frac{f_{SAMP5}}{M_{RCF}}$$

RCF Output Scale Factor and Control Register
Register 0xA4 is a compound register and is used to configure several aspects of the RCF register. Bits 3-0 are used to set the scale of the fixed-point output mode. This scale value may also be used to set the floating-point outputs in conjunction with bit 6 of this register.

Bits 4 and 5 determine the output mode. Mode 00 sets the chip up in fixed-point mode. The number of bits is determined by the serial port configuration. See serial port configuration below.

Mode 01 selects floating-point mode 8+4. In this mode, an 8-bit mantissa is followed by a 4-bit exponent. In mode 1x (x is don't care), the mode is 12+4, or 12 bit mantissa and 4-bit exponent.

Floating Point 8 + 4	1x
Floating Point 12 + 4	01
Fixed Point	00

Table 6. Output Mode Formats

Normally, the AD6634 will determine the exponent value that optimizes numerical accuracy. However, if bit 6 is set, the value stored in bits 3-0 is used to scale the output. This ensures that consistent scaling and accuracy during conditions that may warrant predictable output ranges.

If bit 7 is set, the same exponent will be used for both the real and imaginary (I and Q) outputs. The exponent used will be the one that prevents numeric overflow at the expense of small signal accuracy. However, this is seldom a problem as small numbers would represent 0 regardless of the exponent used.

Bit 8 is the RCF bank select bit used to program the register. When this bit is 0, the lowest block of 128 is selected (taps 0 through 127). When high, the highest block is selected (taps 128 through 255). It should be noted that while the chip is computing filters, tap 127 is adjacent to 128 and there are no paging issues.

Bit 9 Selects where the input to each RCF comes from. If bit 9 is clear, then the RCF input comes from the CIC5 normally associated with the RCF. If however, the bit is set, then the input comes from CIC5 channel 1. The only exception is channel 1, which uses the output of CIC5 channel 0 as its alternate. Using this feature, each RCF can either operate on its own channel data or be paired with the RCF of channel 1. The RCF of channel 1 can also be pared with channel 0. This control bit is used with poly-phase distributed filtering.

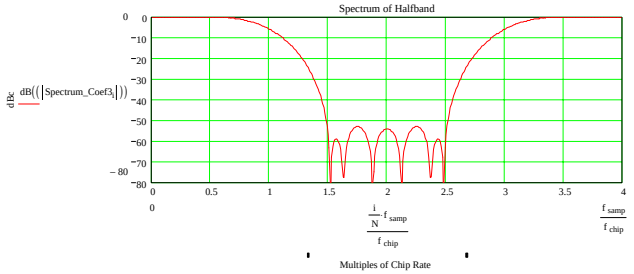
If bit 10 is clear, the AD6634 channel operates in normal mode. However, if bit 10 is set, then the RCF is by-passed to Channel BIST. See BIST (Built In Self Test) section below for more details.

INTERPOLATING HALF BAND FILTERS

The AD6634 has two interpolating half band finite impulse response filters that immediately precede the two digital AGCs and after the four RCF channel outputs. Each interpolating half band takes 16-bit I and 16-bit Q data from the preceding RCF and outputs 16-bit I and 16-bit Q to the AGC. The half band and AGC operate independently of each other, so the AGC can be bypassed, in which case the output of the half band is sent directly to the output data port. The half bands also operate independent of each other -- either one can be enabled or disabled. The control register for half band A is at address 0x08 and for half band B is at address 0x09.

Half band A can listen to all 4 channels: channels 0, 1, 2, and 3; channel 0 and 1; or only channel 0. Half band B can listen to channels 2 and 3,or only channel 2. Each half band interleaves the channels specified in its control register and interpolates by two on the combined data from those channels. For one channel running at twice the chip rate, the halfband can be used to output channel data at 4x the chip rate.

The frequency response of the interpolating halfband FIR is shown in the graph with respect to the chip rate.



Interpolating Halfband Frequency Response

The SNR of the interpolating halfband is around –149.6 dB. The highest error spurs due to fixed-point arithmetic are around –172.9 dB. The coefficients of the 13-tap interpolating halfband FIR are given in the table.

0
14
0
-66
0
309
512
309
0
-66
0
14
0

Halfband Coefficients

AUTOMATIC GAIN CONTROL

The AD6634 is equipped with two independent automatic gain control (AGC) loops for direct interface with a RAKE receiver. It is important that the decimating filters of the AD6634 preceding the AGC reject undesired signals, so that each AGC loop is only operating on the carrier of interest and carriers at other frequencies do not affect the ranging of the loop.

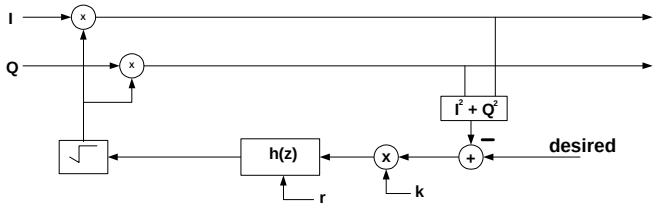
The AGC compresses the 23-bit complex output of the interpolating half band filter into a programmable word size of 4-8, or 16 bits. The AGC maintains a constant mean power on the output despite the level of the signal of interest, allowing operation in environments where the dynamic range of the signal exceeds the dynamic range of the output resolution.

There are three sources of error introduced by the AGC function: underflow, overflow, and modulation. Underflow is caused by truncation of bits below the output range. Overflow is caused by clipping errors when the output signal exceeds the output range. Modulation error occurs when the output gain varies during the reception of a data.

The desired signal level should be set based on the probability density function of the signal so that the errors due to underflow and overflow are balanced. The gain and damping values of the loop filter should be set so that the AGC is fast enough to track long term amplitude variations of the signal that might cause excessive underflow or overflow, but slow enough to avoid excessive loss of amplitude information due to the modulation of the signal.

The AGC Loop

The AGC adjusts the gain of the incoming data according to how far it is from a given desired signal level. First, the loop finds the square of the incoming complex data signal by squaring I and Q and adding them. All loop processing is done on the square of the magnitude of the output signal.



Conceptual Block Diagram of the AGC

The output power is subtracted from the desired signal level specified in registers (0x0B ,0x012) leaving an error term to be processed by the loop filter. This error is then multiplied by the programmable gain parameter, k, and fed to the loop filter, h(z). The loop filter has a programmable parameter, r, which allows adjustment of the filter time constant that determines the window for calculating the peak-to-average ratio.

Since the loop operates on the square of the magnitude, the square root of the loop gain is taken at the end of the loop. The square root of the loop filter output provides the controlled gain used to modify the incoming data stream.

Desired Clipping Level Mode

Each AGC can also be configured so that the loop locks on a desired clipping level or a desired signal level. For signals that tend to exceed the bounds of the peak-to-average ratio, this option allows a way to keep from truncating those signals and still provide an AGC that attacks quickly and settles to the desired output level. This option is not shown in the block diagram but operates similarly to the desired signal level option.

First, the incoming data signal is truncated to a lower resolution and an error term is generated that is the difference between the two signals. This term is passed to the complex squared magnitude block. The desired clipping level is then subtracted out, leaving an error term to be processed by the rest of the loop filter. The rest of the loop operates the same as the desired signal level mode.

Addresses 0x0C – 0x10 have been reserved for configuring AGC A and addresses 0x11 – 0x17 have been reserved for configuring AGC B.

USER CONFIGURABLE BUILT IN SELF TEST (BIST)

The AD6634 includes two built in test features to test the integrity of each channel. The first is a RAM BIST (Built In Self Test) and is intended to test the integrity of the high-speed random access memory within the AD6634. The second is Channel BIST, which is designed to test the integrity of the main signal paths of the AD6634. Each BIST function is independent of the other meaning that each channel can be tested independently at the same time.

RAM BIST

The RAM BIST can be used to validate functionality of the on-chip RAM. This feature provides a simple pass/fail test, which will give confidence that the channel ram is operational. The following steps should be followed to perform this test.

- The Channels to be tested should be put into Sleep mode via the external address register 0x011.
- The RAM BIST Enable bit in the RCF register xA8 should be set high.
- Wait 1600 clock cycles.
- Register 0xA8 should be read back. If bit 0 is high, the test is not yet complete. If bit 0 is low, the test is complete and bits 1 and 2 indicate the condition of the internal ram. If bit 1 is high, then CMEM is bad. If bit 2 is high then DMEM is bad.

XA8	Coefficient MEM	Data MEM
XX1	Test incomplete	Test incomplete
000	PASS	PASS
010	FAIL	PASS
100	PASS	FAIL
110	FAIL	FAIL

Table 7. BIST Register 0xA8

CHANNEL BIST

The Channel BIST is a thorough test of the selected AD6634 signal path. With this test mode, it is possible to use externally supplied vectors or an internal pseudo-random generator. An error signature register in the RCF monitors the output data of the channel and is used to determine if the proper data exits the RCF. If errors are detected then each internal block may be bypassed and another test can be run to debug the fault. The I and Q paths are tested independently. The following steps should be followed to perform this test.

- The Channels to be tested should be configured as required for the application setting the decimation rates, scalars and RCF coefficients.
- The Channels should remain in the Sleep mode.
- The Start Hold-Off counter of the channels to be tested should be set to 1.
- Memory location 0xA5 and 0xA6 should be set to 0.
- The Channel BIST located at 0xA7 should be enabled by setting bits 19-0 to the number of RCF outputs to observe.
- Bit 4 of external address register 5 should be set high to start the soft sync.
- Set the SYNC bits high for the channels to be tested.
- Bit 6 must be set to 0 to allow the user to provide test vectors. The internal pseudo-random number generator may also be used to generate an input sequence by setting bit 7 high.
- An internal –FS sine can be inserted when bit 6 is set to 1 and bit 7 is cleared.
- When the SOFT_SYNC is addressed, the selected channels will come out of the sleep mode and processing will occur.
- If the user is providing external vectors, then the chip may be brought out of Sleep mode by one of the other methods provided that either of the IEN inputs is inactive until the Channel is ready to accept data.
- After a sufficient amount of time, the Channel BIST Signature registers 0xA5 and 0xA6 will contain a numeric value that can be compared to the expected value for a known good AD6634 with the exact same configuration. If the values are the same, then there is a very low probability that there is an error in the channel.

CHIP SYNCHRONIZATION

Two types of synchronization can be achieved with the AD6634. These are Start and Hop. Each is described in detail below. The synchronization is accomplished with the use of a shadow register and a hold off counter. See Figure 29 below for a simplistic schematic of the NCO shadow register and NCO Freq Hold Off counter to understand basic operation. Enabling the clock (AD6634 CLK) for the hold off counter can occur with either a Soft_Sync (via the micro port), or a Pin Sync (via any of the four AD6634 SYNC pins A,B,C, and D). The functions that include shadow registers to allow synchronization include:

1. Start
2. Hop (NCO Frequency)

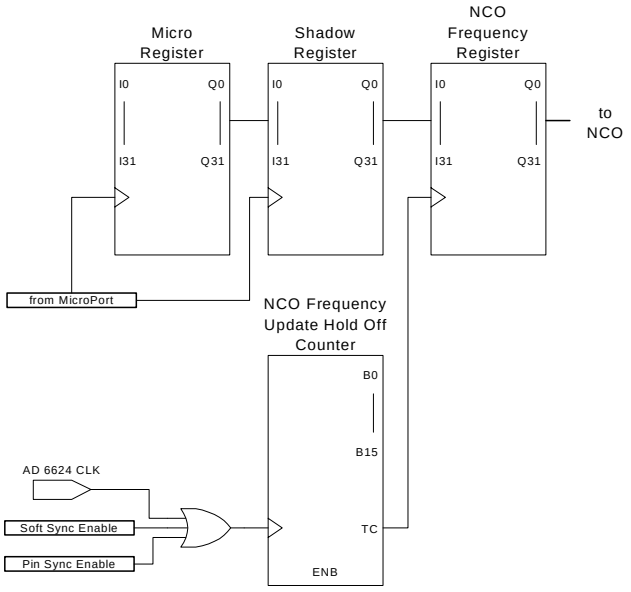


Figure 29. NCO Shadow Register and Hold Off Counter

Start

Start refers to the start-up of an individual channel, chip, or multiple chips. If a channel is not used, it should be put in the Sleep Mode to reduce power dissipation. Following a hard reset (low pulse on the AD6634 /Reset pin), all channels are placed in the Sleep Mode. Channels may also be manually put to sleep by writing to the mode register controlling the sleep function.

Start With No Sync

If no synchronization is needed to start multiple channels or multiple AD6634s, the following method should be used to initialize the device.

1. To program a channel, it must first be set to the Program Mode (bit high) and Sleep Mode (bit high) (Ext Address 3). The Program Mode allows programming of data memory and coefficient memory (all other registers are programmable whether in Program Mode or not). Since no synchronization is used all Sync bits are set low (External Address 4). All appropriate control and memory registers (filter) are then loaded. The Start Update Hold Off Counter (0x83) should be set to 1.
2. Set the appropriate Program and Sleep bits low (Ext Address 3). This enables the channel. The channel must have Program and Sleep Mode low to activate a channel.

Start With Soft Sync

The AD6634 includes the ability to synchronize channels or chips under microprocessor control. One action to synchronize is the start of channels or chips. The Start Update Hold Off Counter (0x00) in conjunction with the Start bit and Sync bit (Ext Address 5) allow this synchronization. Basically the Start Update Hold Off Counter delays the Start of a channel(s) by its value (number of AD6634 CLKs. The following method is used to synchronize the start of multiple channels via microprocessor control.

1. Set the appropriate channels to sleep mode (a hard reset to the AD6634 Reset pin brings all 4 channels up in sleep mode).
2. Note that the time from when the RDY (pin 57) goes high to when the NCO begins processing data is the contents of the Start Update Hold Off Counter(s) (0x83) + 6 master clock cycles.
3. Write the Start Update Hold Off Counter(s) (0x83) to the appropriate value (greater than 1 and less than 2^16-1). If the chip(s) is not initialized, all other registers should be loaded at this step.
4. Write the Start bit and the SyncX(s) bit high (Ext Address 4).
5. This starts the Start Update Hold Off Counter counting down. The counter is clocked with the AD6634 CLK signal. When it reaches a count of one the Sleep bit of the appropriate channel(s) is set low to activate the channel(s).

Start With Pin Sync

The AD6634 has 4 Sync pins A, B, C and D that can be used to provide for very accurate synchronization channels. Each channel can be programmed to look at any of the 4 sync pins. Additionally, any or all channels can monitor a single Sync pin or each can monitor a separate pin, providing complete flexibility of synchronization. Synchronization of Start with one of the external signal is accomplished with the following method.

1. Set the appropriate channels to sleep mode (a hard reset to the AD6634 Reset pin brings all 4 channels up in sleep mode).
2. Note that the time from when the SYNC pin goes high to when the NCO begins processing data is the contents of the Start Update Hold Off Counter(s) (0x83) + 3 master clock cycles.

3. Write the Start Update Hold Off Counter(s) (0x83) to the appropriate value (greater than 1 and less than 2^16-1). If the chip(s) is not initialized, all other registers should be loaded at this step.
4. Set the Start on Pin Sync bit and the appropriate Sync Pin Enable high (Ext Address 4) (A, B, C or D).
5. When the Sync pin is sampled high by the AD6634 CLK this enables the count down of the Start Update Hold Off Counter. The counter is clocked with the AD6634 CLK signal. When it reaches a count of one the Sleep bit of the appropriate channel(s) is set low to activate the channel(s).

Hop

Hop is a jump from one NCO frequency to a new NCO frequency. This change in frequency can be synchronized via microprocessor control (Soft Sync) or an external Sync signal (PIN Sync) as described below.

To set the NCO frequency without synchronization the following method should be used.

Set Freq No Hop

1. Set the NCO Freq Hold Off counter to 0.
2. Load the appropriate NCO frequency. The new frequency will be immediately loaded to the NCO.

Hop With Soft Sync

The AD6634 includes the ability to synchronize a change in NCO frequency of multiple channels or chips under microprocessor control. The NCO Freq Hold Off counter (0x84) in conjunction with the Hop bit and the Sync bit (Ext Address 4) allow this synchronization. Basically the NCO Freq Hold Off counter delays the new frequency from being loaded into the NCO by its value (number of AD6634 CLKs). The following method is used to synchronize a hop in frequency of multiple channels via microprocessor control.

1. Note that the time from when the RDY (pin 57) goes high to when the NCO begins processing data is the contents of the NCO Freq Hold Off counter (0x84) + 7 master clock cycles.
2. Write the NCO Freq Hold Off (0x84) counter to the appropriate value (greater than 1 and less then 2^16-1).
3. Write the NCO Frequency register(s) to the new desired frequency.
4. Write the Hop bit and the Sync(s) bit high (Ext Address 4).
5. This starts the NCO Freq Hold Off counter counting down. The counter is clocked with the AD6634 CLK signal. When it reaches a count of one the new frequency is loaded into the NCO.

Hop With Pin Sync

The AD6634 include 4 Sync pins to provide the most accurate synchronization, especially between multiple AD6634s. Synchronization of Hopping to a new NCO frequency with an external signal is accomplished with the following method.

1. Note that the time from when the SYNC pin goes high to when the NCO begins processing data is the contents of the NCO Freq Hold Off counter (0x84) + 5 master clock cycles.
2. Write the NCO Freq Hold Off counter(s) (0x84) to the appropriate value (greater than 1 and less than 2^16-1).
3. Write the NCO Frequency register(s) to the new desired frequency.
4. Set the Hop on Pin Sync bit and the appropriate Sync Pin Enable high.
5. When the selected Sync pin is sampled high by the AD6634 CLK this enables the count down of the NCO Freq Hold Off counter. The counter is clocked with the AD6634 CLK signal. When it reaches a count of one the new frequency is loaded into the NCO.

PARALLEL OUTPUT PORTS

The AD6634 incorporates two independent 16-bit parallel ports for output data transfer. Both parallel ports share pins and internal mux circuitry with the two Link Ports and the serial ports. As a result, the parallel ports and serial ports cannot be used simultaneously. The PAR/SER pin is pulled HIGH to enable the parallel output port. In addition, a single parallel port and a single Link Port can be used simultaneously, but only if they do not share the same data path; the two possible choices are Parallel Port A with Link Port B, or Parallel Port B with Link Port A. Figure XXX presents a simplified block diagram showing the AD6634's output data routing configuration.

{Graphic}
Figure XXX

Parallel port configuration is specified by accessing Port Control Register addresses 0x18 and 0x1A for parallel ports A and B, respectively. Port clock Master/Slave mode (described later) is configured using the Port Clock Control register at address 0x1C. Note that to access these registers, bit 5 (Access Port Control Registers) of external address 3 (SLEEP register) must be set. The address is then selected by programming the CAR register at external address 6.

The parallel ports are enabled by setting bit 7 of the Link Control registers at addresses 0x19 and 0x1B for ports A and B, respectively.

Each parallel port is capable of operating in either Channel mode or AGC mode. Each mode is described in detail below.

Channel mode

Parallel port Channel mode is selected by setting bit 0 of addresses 0x18 and 0x1A for parallel ports A and B, respectively. In Channel mode, I and Q words from each channel is directed to the parallel port, bypassing the AGC. The specific channels output by the port is selected by setting bits 1 through 4 of Input Port Control Register 0x18 (port A) and 0x1A (port B).

Channel mode provides two data formats. Each format requires a different number of parallel port clock (PCLK) cycles to complete the transfer of data. In each case, each data element is transferred during one PCLK cycle. See Figure XXX presents parallel port timing.

{ Graphic }
Figure XXX

The 16-bit Interleaved format provides I and Q data for each output sample on back-to-back PCLK cycles. Both I and Q words consist of the full port width of 16 bits. Data output is triggered on the rising edge of PCLK when both REQ and ACK are asserted. I data is output during the first PCLK cycle; and the PAIQ and PBIQ output indicator pins are set high to indicate that I data is on the bus. Q data is output during the subsequent PCLK cycle; and the PAIQ and PBIQ output indicator pins are low during this cycle.

The 8-bit Concurrent format provides 8 bits of I data and 8 bits of Q data simultaneously during one PCLK cycle, also triggered on the rising edge of PCLK. The I byte occupies the most significant byte of the port, while the Q byte occupies the least significant byte. The PAIQ and PBIQ output indicator pins are set high during the PCLK cycle. Note that if data from multiple channels are output consecutively, the PAIQ and PBIQ output indicator pins will remain high until data from all channels has been output.

The PACH[1:0] and PBCH[1:0] pins provide a 2-bit binary value indicating the source channel of the data currently being output.

Care should be taken to read data from the port as soon as possible. If not, the sample will be overwritten when the next new data sample arrives. This occurs on a per-channel basis; i.e., a channel 0 sample will only be overwritten by a new channel 0 sample, etc.

The order of data output is dependent on when data arrived at the port, which is is a function of total decimation rate, Start-Holdoff values, etc. Priority order is, from highest to lowest, channels 0, 1, 2, 3.

AGC mode

Parallel port Channel mode is selected by clearing bit 0 of addresses 0x18 and 0x1A for parallel ports A and B, respectively. I and Q data output in AGC mode are output from the AGC, not the individual channels. Each AGC receives data from only two AD6634 channels; AGC A accepts data from channels 0 and 1, while AGC B accepts data from channels 2 and 3. Each pair of channels is required to be configured such that the generation of output samples from the channels is out of phase (by typically 180 degrees). Each parallel port can provide data from either one or both AGCs. Bits 1 and 2 of register addresses 0x18 (port A) and 0x1A (port B) control the inclusion of data from AGCs A and B, respectively.

AGC mode provides only one format, which is similar to the 16-bit Interleaved format of Channel mode. When both REQ and ACK are asserted, the next rising edge of PCLK triggers the output of a 16-bit AGC I word for one PCLK cycle. The PAIQ and PBIQ output indicator pins are high during this

cycle, and is low otherwise. A 16 bit AGC Q word is provided during the subsequent PCLK cycle. If the AGC Gain word has been updated since the last sample, a 16-bit Gain word is provided during the PCLK cycle following the Q word.

The data provided by the PACH[1:0] and PBCH[1:0] pins in AGC mode is different than that provided in Channel mode. In AGC mode, PACH[0] and PBCH[0] indicate the AGC source of the data currently being output (0=AGC A, 1=AGC B). PACH[1] and PBCH[1] indicate whether the current data is and I/Q word or an AGC Gain word (0=I/Q word, 1=AGC Gain word).

Master/Slave PCLK modes

The parallel ports may operate in either Master or Slave mode. The mode is set via the Port Clock Control register (address 0x1C). The parallel ports power up in Slave mode to avoid possible contentions on the PCLK pin.

In Master mode, PCLK is an output whose frequency is the AD6634 clock frequency divided by the PCLK divisor. Since values for PCLK_divisor[2:1] can range from 0 to 3, integer divisors of 1 to 4, respectively, can be obtained. Since the maximum clock rate of the AD6634 is 80 MHz, the highest PLCK rate in Master mode is also 80 MHz. Master mode is selected by setting bit 0 of address 0x1C.

In Slave mode, external circuitry provides the PCLK signal. Slave-mode PCLK signals may be either synchronous or asynchronous. The maximum Slave-mode PCLK frequency is 100 MHz.

Parallel Port Pin Functionality

The following describes the functionality of the pins used by the parallel ports.

PAR/SER Enables the parallel output port when set HIGH.

PCLK: Input/output. As an output (Master mode), the maximum frequency is CLK/N, where CLK is AD6634 clock and N is an integer divisor from 1 to 4. As an input (Slave mode), it may be asynchronous relative to the AD6634 CLK. This pin powers up as an input to avoid possible contentions. Other port outputs change on the rising edge of PCLK.

REQ: Active HIGH output, synchronous to PCLK. A logic HIGH on this pin indicates that data is available to be shifted out of the port. A logic HIGH value remains high until all pending data has been shifted out.

ACK: Active HIGH asynchronous input. Applying a logic LOW on this pin inhibits parallel port data shifting. Applying a logic HIGH to this pin when REQ is high causes the parallel port to shift out data according the programmed data mode. ACK is sampled on the rising edge of PCLK. Assuming REQ is asserted, the latency from the assertion of ACK to data appearing at the parallel port output is no more than 1.5 PCLK cycles (see Figure XXX). ACK may be held high continuously; in this case, when data becomes available, shifting begins 1 PCLK cycle after the assertion of REQ (see Figure XXX).

PAIQ, PBIQ: High whenever I data is present on the port output, low otherwise.

PACH[1:0], PBCH[1:0]: These pins serve to identify data in both of the data modes. In Channel mode, these pins form a 2-bit binary number identifying the source channel of the current data word. In AGC mode, [0] indicates the AGC source (0=AGC A, 1=AGC B), and [1] indicates whether the current data word is I/Q data (0) or a Gain word (1).

PA[15:0], PB[15:0]: Parallel output data ports. Contents and format are mode-dependent.

SERIAL OUTPUT DATA PORT

The AD6634 has 4 configurable serial output ports (SDO0, SDO1, SDO2, and SDO3). Each port can be operated independent of the other making it possible to connect each to a different DSP. In the case where a single DSP is required, the ports can easily be configured to work with a single serial port on a single DSP. As such, each output may be configured as either serial master or slaves. Additionally, each channel can be configured independent of the others.

Serial Output Data Format

The AD6634 works with a variety of output data formats. These include word lengths of 12, 16 and 24-bit precision. In addition to the normal linear binary data format, the AD6634 offers a floating-point data format to simplify numeric processing. These formats are 8-bit mantissa with 4-bit exponent and 12-bit mantissa and 4-bit exponent. These modes are available regardless of the bit precision of the serial data frame. In the normal linear binary data format, a programmable internal 4 bit-scaling factor is used to scale the output. See the section title "RCF Output Scale Factor and Control Register" above for more details. In all modes, the data is shifted out of the device in Big Endian format (MSB first).

In floating point mode, the chip normally determines the exponent automatically, however, the chip can be forced to use the same exponent for both the real and imaginary portion of the data. The choice of exponents favors prevention of numerical overflow at the expense of small number accuracy. However, this should not be a problem as small numbers imply numbers close to zero anyway.

Finally, the AD6634 channel can be forced to use a pre-selected scale factor if desired. This allows for a consistent range of data useful to many applications.

Serial Data Frame (Serial Bus Master)

The serial data frame is initiated with the Serial Data Frame Sync (SDFS0, SDFS1, SDFS2, or SDFS3). As each channel within the AD6634 completes a filter cycle, data is transferred into the serial data buffer. In the Serial Bus Master (SBM) mode, the internal serial controller initiates the SDFS on the next rising edge of the serial clock. In the AD6634, there are 3 different modes that the frame sync may be generated in as a Serial Bus Master.

In the first mode, the SDFS is valid for one complete clock cycle prior to the data shift. On the next clock cycle the AD6634 begins shifting out the digitally processed data stream. Depending on the bit precision of the serial configuration, either 12, 16 or 24 bits of I data are shifted out followed by 12, 16 or 24 bits of Q data. The format of this data will be in one of the formats listed above. In the second mode, the SDFS is high for the entire time that valid bits are being shifted. The SDFS bit goes high concurrent with the first bit shifted out of the AD6634.

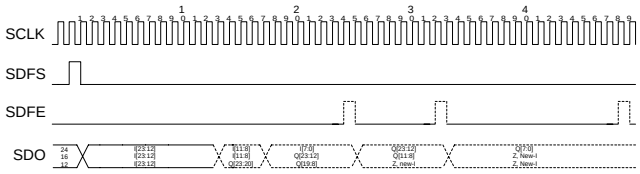


Figure 30. SDFS Valid for One SCLK Cycle

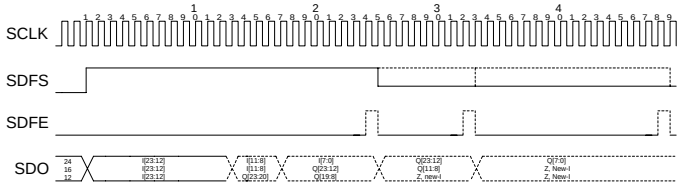


Figure 31. SDFS is High During Data Shift

In the final mode, the SDFS bit goes high as in the first mode one clock cycle prior to the actual data. However, a second SDFS is inserted one clock cycle prior to the shift of the first Q bit. In this manner, each word out of the AD6634 is accompanied by an SDFS.

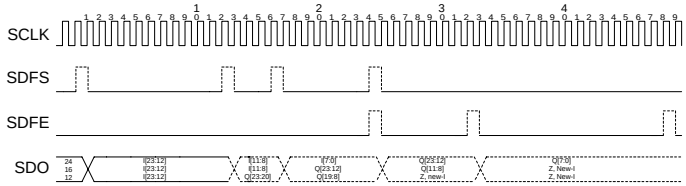


Figure 32. A Second SDFS Inserted Prior to First Q Bit

Regardless of the mode above, the SDFE behaves the same in each. On the last bit of the serial frame (least significant bit of the Q word), the Serial Data Frame End (SDFE) is raised. The SDFE signal can either be used by the DSP to indicate the end of the frame or it can be used as the SDFS (Serial Data Frame Sync) of another AD6634 chip or channel running in Serial Cascade mode.

Serial Data Frame (Serial Cascade)

Any of the AD6634 serial outputs may be operated in the serial cascade mode (serial slave). In this mode, the selected AD6634 channel requires that an external device such as a DSP to issue the serial clock and SDFS.

To operate successfully in the serial cascade mode, the DSP must have some indication that the AD6634 channel's serial buffer is ready to send data. This is indicated by the assertion of the DRx pin where 'x' is the channel number. This pin should be tied to an interrupt or flag pin of the DSP. In this manner, the DSP will know when to service the serial port.

When the DSP begins handling the serial service, the serial port should be configured such that the SDFS pin is asserted

one clock cycle prior to shifting data. As such, the AD6634 channel samples the SFDS pin on the rising edge of the serial clock. On the next rising edge of the serial clock the AD6634 serial port begins shifting data until the specified number of bits have been shifted.

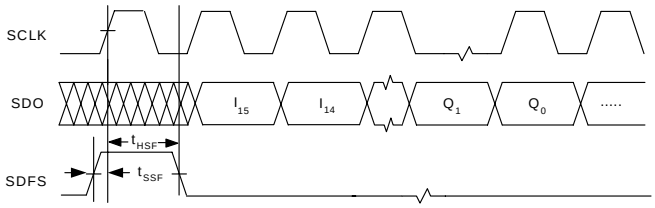


Figure 33. SDO, SDFS Switching Characteristics (SBM=0)

On the last bit of the serial frame (least significant bit of the Q word), the Serial Data Frame End (SDFE) is raised. The SDFE signal can either be used by the DSP to indicate the end of the frame or it can be used as the SDFS (Serial Data Frame Sync) of another AD6634 chip or channel running in Serial Cascade mode.

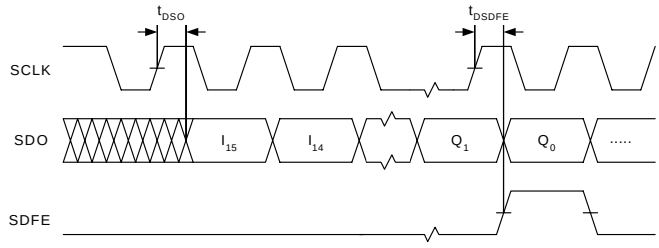


Figure 34. SDO, SDFE Switching Characteristics

Configuring the Serial Ports

Each Serial Output Port may function as either a Master or Slave. A Serial Bus Master will provide SCLK (SCLK0, SCLK1, SCLK2, SCLK3) and SDFS outputs. A Serial Slave will accept these signals as inputs. Upon the lift of /RESET Serial Port 0 will become a Master if the SBM0 pin is high and will be a slave if SBM0 is low. Serial Ports 1, 2 and 3 will always default to serial slaves when /RESET is taken low. They can be programmed as a master by setting the SBM1, SBM2, and SBM3 bits in the 0xA9 Registers high.

Serial Port Data Rate

If a Serial Port is defined as a master then the SCLK frequency is defined by the equation below. F_{CLK} is the frequency of the master clock of the AD6634 channel and SDIVx is the Serial Division word for the channel (1, 2 or 3). The SDIVx for serial port 0 are located directly as pins on the package for easy hardware configuration and are **not** mapped into 0xA9. For serial ports 1, 2 and 3, the internal register 0xA9 bits 3-0 define the SDIV (SDIV0, SDIV1, SDIV2, SDIV3) word.

$$f_{SCLK} = \frac{f_{CLK}}{(SDIV + 1)}$$

AD6634 Serial Port to DSP Interconnection

The AD6634 is very flexible in the manner that the serial ports can be configured and connected to external devices. Each of the channels can be independently configured and processed by different DSPs or all of the channels can be chained together to form a TDM (time division multiplexed) serial chain. This allows one DSP to handle all of the channels. Additionally, the channels can be parceled off in any combination in between.

To configure a channel as a serial bus master, bit 4 of register xA9 should be set high. However, as with the SDIV pins, channel 0 SBM is not mapped to memory and is instead pinned out and must be hard wired as either a master or a slave. Figure 35 shows the typical interconnections between an AD6634 Channel in Serial Bus Master mode and a DSP.

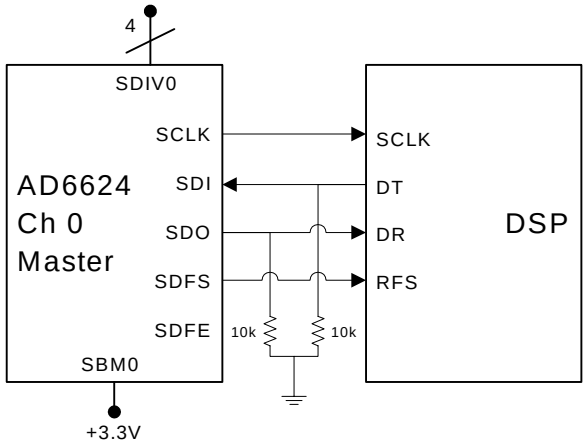


Figure 35. Typical Serial Data Output Interface to DSP (Serial Master Mode, SBM = 1)

Serial Slave Operation

The AD6634 can also be operated as a serial bus slave. In this configuration shown in Figure 36, the serial clock provided by the DSP can be asynchronous with the AD6634 clock and input data. In this mode the clock has a maximum frequency of 80Mhz and must be fast enough to read the entire serial frame prior to the next frame coming available. Since the AD6634 output is derived (via the Decimation/Interpolation Rates) from its input sample rate the output rate can be determined by the user. The output rate of the AD6634 is given below.

$$F_{OUT} = \frac{F_{ADC} * L_{CIC2}}{M_{CIC2} * M_{CIC5} * M_{RCF}}$$

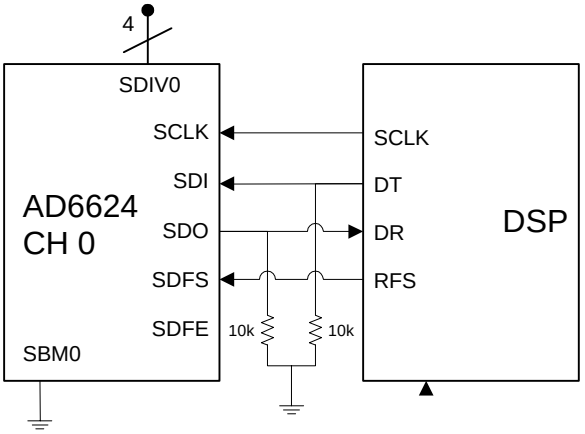


Figure 36. Typical Serial Data Output Interface to DSP (Serial Slave Mode, SBM = 0)

AD6634 Serial Ports Cascaded

Serial output ports may be cascaded on the AD6634 such that the SDOs outputs are shorted together. In this mode the SDO port of the master channel tristates when the SDO port of the slave channel is active. This allows data to be shifted out of a slave channel immediately following the completion of data frame (I/Q pair) shifting out of a master AD6634 channel. To accomplish this, the SDFE signal of the master channel drives the SDFS input of the slave channel. Serial output port cascading can be used with channels on the same AD6634 device, or with channels on two different devices as shown in Figure 37. To satisfy t_{SSF} and t_{HSF} timing requirements of the slave channel, the SDFE signal from the master channel should be delayed using a non-inverting buffer (e.g. 74LVC244A) that provides a minimum of 1.5ns of propagation delay. Figure 37 shows the cascade capability between two AD6634 devices. The first is connected as a serial master (SBM=1), and the second is configured in serial cascade mode (SBM=0).

Using the AD6634 master-slave mode permits a DSP to shift the data from the master AD6634 serial port followed immediately by a frame of data (I and Q words) from the AD6634 slave port. As shown in Figure 37 the Master Port is Serial Port 0. The slave port can be either serial port 1, 2 or 3 or a Serial Port 0 from another AD6634. Other AD6634 Serial Ports can be cascaded to the slave port by using the SDFE and SDFS in the manner shown. The only limit to the number of ports that can be cascaded comes from serial bandwidth and fan-out considerations.

There must be enough Serial Clock cycles available to shift the necessary data into the DSP and the SCLK (common to all channels and DSP) must be closely monitored to ensure that it is a clean signal. For Systems where a single DSP serial port will be connected to many AD6634 Serial Ports it is recommended that the SCLK signal from the Master be buffered to the slaves. See Serial Port Buffering in the applications section.

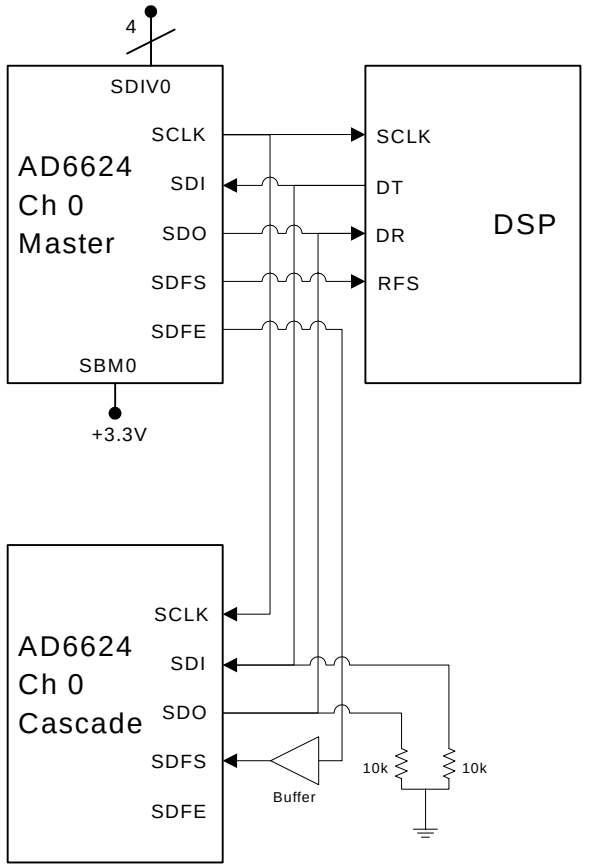


Figure 37. Typical Serial Data Output Interface to DSP (Serial Cascade Mode, SBM = 0)

Serial Output Frame Timing (Master and Slave)

The SDFS signal transitions accordingly depending on whether the part in is Master (SBM=1, Figure 44) or Slave (SBM=0, Figure 33) modes. The next rising edge of SCLK after this occurs will drive the first bit of the serial data on the SDO pin. The falling edge of SCLK or the subsequent rising edge can then be used by the DSP to sample the data until the required number of bits is received (determined by the serial output port word length). If the DSP has the ability to count bits, the DSP will know when the complete frame is received. If not, the DSP can monitor the SDFE pin to determine that the frame is complete.

Serial Port Timing Specifications

Whether the AD6634 serial channel is operated as a Serial Bus Master or as a Serial Slave, the serial port timing is identical. The diagrams below indicated the required timing for each of the specification.

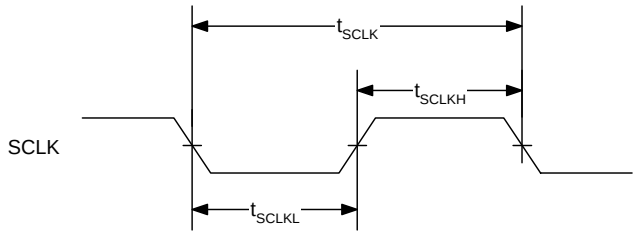


Figure 38. SCLK Timing Requirements

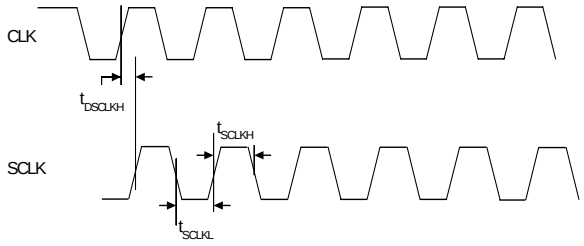


Figure 39. SCLK Switching Characteristics (Divide by 1)

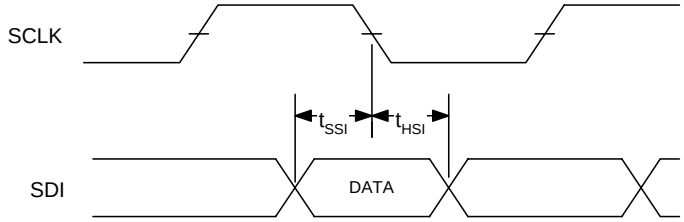


Figure 40. Serial Input Data Timing Requirements

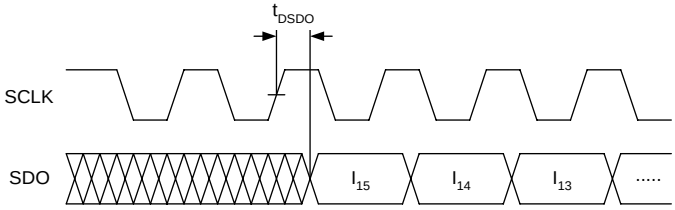


Figure 41. Serial Output Data Switching Characteristics

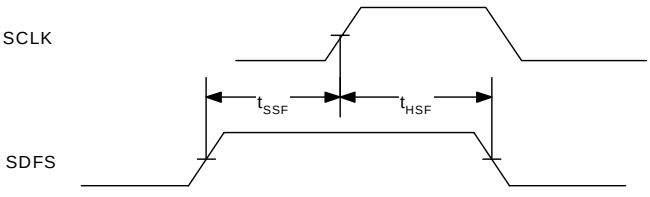


Figure 42. SDFS Timing Requirements (SBM=0)

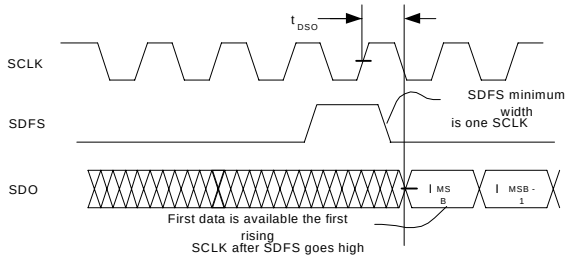


Figure 43. Timing for Serial Output Port (SBM=1)

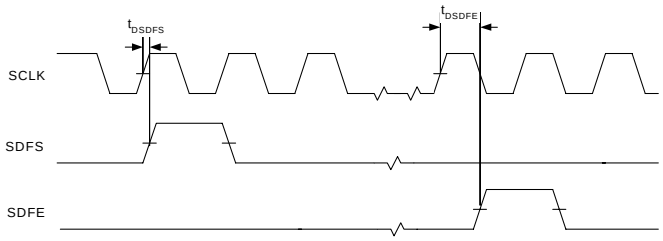


Figure 44. Serial Frame Switching Characteristics (SBM=1)

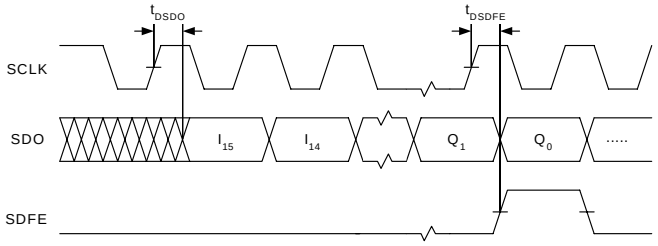


Figure 45. SDO, SDFE Switching Characteristics

SBM0

SBM0 is the Serial Bus Master pin for the Channel 0 Serial Port only. Serial Ports 1, 2 and 3 will always default to serial slave mode but can be programmed as masters in the internal register space. The SBM0 pin gives the user the option to boot the AD6634 through Serial Port 0 as a master. When SBM0 is high (master mode), the AD6634 generates SCLK0 and SDFS0. When SBM0 is low (slave mode), the AD6634 accepts external SCLK0 and SDFS0 signals. When configured as a bus master the SCLK0 signal can be used to strobe data into the DSP interface. When used with another AD6634 in Serial Cascade Mode, SCLK0 can be taken from the master AD6634 and used to shift data out from the cascaded device. In this situation SDFS of the slave AD6634 channel is connected to the SDFE pin of the master AD6634 channel (or the preceding chip in the chain). When an AD6634 is in Serial Slave Mode all of the serial port activities are controlled by the external signals SCLK and SDFS.

Regardless of whether the chip is a Serial Bus Master or is in Serial Slave Mode the AD6634 Serial Port functions are identical except for the source of the SCLK and SDFS pins.

SCLKx
SCLK is an output when SBM (SBM0 or register bit for serial ports 1, 2 and 3) is high; SCLK is an input when SBM (SBM0 or register bit for serial ports 1, 2 and 3) is low in serial slave mode. In either case the SDIN input is sampled on the falling edge of SCLK and all outputs are switched on the rising edge of SCLK. The SDFS pin is sampled on the falling edge of SCLK. This allows the AD6634 to recognize the SDFS in time to initiate a frame on the very next SCLK rising edge. The maximum speed of this port is 80Mhz.

SDINx
SDIN is the Serial Data Input. Serial Data is sampled on the falling edge of SCLK. This pin is used in the serial control mode to write the internal control registers of the AD6634. These activities are described later in the Serial Port Control section. The Serial Input Port is Self Framing and bears no fixed relationship to either SDFS or SDFE.

SDOx
SDO is the Serial Data Output. Serial output data is shifted on the rising edge of SCLK. On the very next SCLK rising edge after an SDFS, the MSB of the I data from the Channel is shifted. On every subsequent SCLK edge a new piece of data is shifted out on the SDO pin until the last bit of data is shifted out. The last bit of data shifted is the LSB of the channels Q data. SDO is tri-stated when the serial port is outside its time-slot. This allows the AD6634 to share the SDIN of a DSP, with other AD6634s or other devices.

SDFSx
SDFS is the Serial Data Frame Sync signal. SDFS is an output when SBMx (SBM0 or register bit for serial ports 1, 2 and 3) is high in the master mode. SDFS is an input when SBMx (SBM0 or register bit for serial ports 1, 2 and 3) is low in the slave mode. SDFS is sampled on the falling edge of SCLK. When SBMx is sampled low, the AD6634 serial port will function as a serial slave. In this mode, the port is silent until the DSP issues a frame sync. When the AD6634 detects an SDFSx on the falling edge of a DSP generated serial clock, on the next rising edge of the serial clock, the AD6634 enables the output driver and shifts the MSB of the I word. Data is shifted until the LSB of the Q word has been sent. On the LSB of the Q word, the AD6634 generates an SDFEx, which can be cascaded to the next SDFSx on a TDM serial chain or to the DSP to indicate that the last bit has been sent.

When SBMx is sampled high, the chip functions as a serial bus master. In this mode, the AD6634 is responsible for generating serial control data. There are three modes of that operation which are set via channel address 0xA9 bits 8-7. Each behaves a little different as detailed below.

In the first mode (0xA9 bits 8-7:00), the SDFSx is valid for one complete clock cycle prior to the data shift. On the next clock cycle the AD6634 begins shifting serial data. In the second mode, (0xA9 bits 8-7:01), the SDFSx is high for the entire time that valid bits are being shifted. The SDFSx bit goes high concurrent with the first bit shifted out of the AD6634 and returns low after the last bit is shifted out of the AD6634. In the third mode, (0xA9 bits 8-7:10), the SDFSx bit goes high as in the first mode one clock cycle prior to the actual data. However, a second SDFSx is inserted one clock cycle prior to the shift of the first Q bit. In this manner, each word out of the AD6634 is accompanied by an SDFSx.

SDFEx

SDFEx is the Serial Data Frame End output. SDFE will go high during the last SCLK cycle (LSB of the Q word) of an active time-slot. The SDFE output of a master AD6634 channel can be tied to the input SDFS of an AD6634 channel in Serial Slave Mode in order to provide a hardwired time-slot scenario. When the Last Bit of SDO data is shifted out of the Master AD6634, the SDFE signal will be driven high by the same SCLK rising edge that this bit is clocked out on. On the falling edge of this SCLK cycle, the slaved serial port will sample its SDFS signal, which is hardwired to the SDFE of the Master. On the very next SCLK rising edge data of the slave will start shifting. There will be no rest between the time-slots of the master and slave.

Serial Word Length
Bits 6-5 of register 0xA9 determine the length of the serial word (I or Q). If these bits are set to ’00’ then each word is 12 bits (12 bits for I and 12 more bits for Q). If set to ‘01’ then the serial words are 16 bits wide and the if set to ‘1x’ (x is don’t care) then the word length is 24 bits.

SDFS Mode
Bits 8-7 of register 0xA9 determine how the SFDS behaves in Serial Bus Master Mode. In serial slave mode, the frame sync must be formatted by programming bits 8-7 to ‘00’.

The first mode is set by programming bits 8-7 to ‘00’. In this mode, the SDFS is valid for one complete clock cycle prior to the data shift. On the next clock cycle the AD6634 begins shifting out the digitally processed data stream. Depending on the bit precision of the serial configuration, either 12, 16, or 24 bits of I data are shifted out followed by 12, 16, or 24 bits of Q data.

The second mode is set by programming bits 8-7 to ‘01’. In this mode, the SDFS is high for the entire time that valid bits are being shifted. The SDFS bit goes high concurrent with the first bit shifted out of the AD6634 and goes low after the last bit has been shifted.

The third mode is set by programming bits 8-7 to ‘1x’ (x is don’t care). In this mode, the SDFS bit goes high as in the first mode one clock cycle prior to the actual data. However, a second SDFS is inserted one clock cycle prior to the shift of the first Q bit. In this manner, each word out of the AD6634 is accompanied by an SDFS.

Mapping RCF Data to the BIST Registers
If bit 9 of 0xA9 is set, then RCF data is routed to the BIST registers. This allows the filter results to be read from the microprocessor port. This can be useful when the data must be accessed via a parallel port and the decimation rate is sufficiently high that throughput does not become an issue.

LINK PORT

The AD6634 has two configurable link ports that provide a seamless data interface with the TigerSHARC DSP. Each link port allows the AD6634 to write output data to the receive DMA channel in the TigerSHARC for transfer to memory. Since they operate independently of each other, each link port can be connected to a different TigerSHARC or different link ports on the same TigerSHARC. The figure below shows how to connect one of the two AD6634 link ports to one of the four TigerSHARC link ports. Link Port A is configured through register 0x19 and Link Port B is configured through register 0x1B. Each is enabled by setting bit 7 of its respective register high and the PAR/SER pin HIGH.

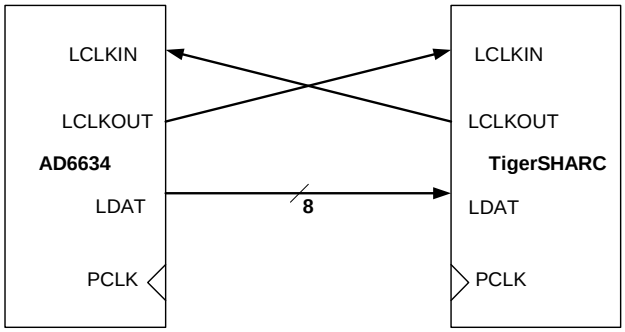


Figure xx: Link Port Connection Between AD6634 and TigerSHARC

Link Port Data Format

Each link port can output data to the TigerSHARC in 5 different formats: 2 channel, 4 channel, dedicated AGC, redundant AGC with gain, and redundant AGC without gain. Each format outputs 2 bytes of I data and 2 bytes of Q data to form a 4 byte IQ pair. Since the TigerSHARC link port transfers data in quad-word (16-byte) blocks, four IQ pair can make up one quad-word. If the channel data is selected (Bit 0 = 1), then 4-byte IQ words of the four channels can be output in succession or alternating channel pair IQ words can be output. The following figures show the quad-word transmitted for each scenario with corresponding register values for configuring each link port.

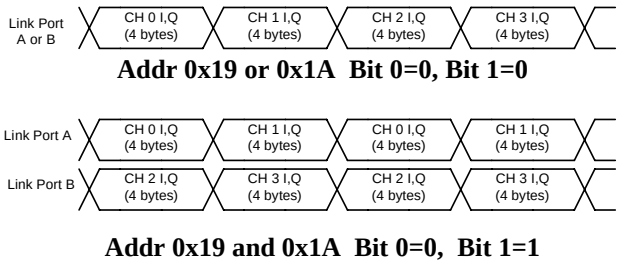


Figure xx: Link Port Data from RCF

If AGC output is selected (Bit 0 = 1), then gain information can be sent with the IQ pair from each AGC. Each link port can be configured to output data from one AGC or both link ports can output data from the same AGC. If both link ports are transmitting the same data, then gain data must be sent with the IQ words (Bit 2 = 0). Note that the actual AGC gain is only 2 bytes, so the link port sends 2 bytes of 0's immediately after each gain word to make a full 16-byte quad-word.

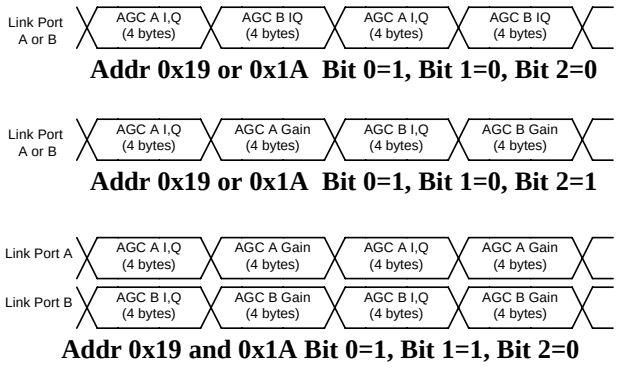


Figure xx: Link Port Data from AGC

Note that Bit 0 =1 Bit 1 = 0, and Bit 2 = 1 is not a valid configuration. Bit 2 must be set to 0, to output AGC A IQ and gain words on link port A and AGC B IQ and gain words on link port B.

Link Port Timing

Both link ports run off of PCLK, which can be externally provided to the chip (Addr 0x1C Bit 0 = 0) or generated from the master clock of the AD6634 (Addr 0x1C Bit 0 = 1). This register boots to 0 (slave mode) and allows the user to control the data rate coming from the AD6634. PCLK can be run as fast as 100 MHz.

The link port provides a 1-byte data words (LA[7:0], LB[7:0] pins) and output clocks (LACLKOUT, LBCLKOUT pins) in response to a ready signals (LACLKIN, LBCLKIN pins) from the receiver. Each link port transmits 8 bits on each edge of LCLKOUT, requiring 8 LCLKOUT cycles to complete transmission of the full 16 bytes of a TigerSHARC quad-word.

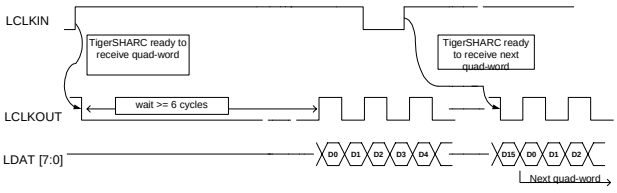


Figure xx: Link Port Data Transfer

Due to the TigerSHARC link port protocol, the AD6634 must wait at least 6 PCLK cycles after the TigerSHARC is ready to receive data, as indicated by the TigerSHARC setting the respective AD6634 LCLKIN pin high. Once the AD6634 link port has waited the appropriate number of PCLK cycles and has begun transmitting data, the TigerSHARC does a connectivity check by sending the AD6634 LCLKIN low and then high while the data is being transmitted. This tells the AD6634 link port that the TigerSHARC's DMA is ready to receive the next quad-word after completion of the current quad-word. Because the connectivity check is done in parallel to the data transmission, the AD6634 is able to stream uninterrupted data to the TigerSHARC.

The length of the wait before data transmission is a 4-bit programmable value in the link port control registers (0x19 and 0x1B bits 6-3). This value allows the AD6634 PCLK and the TigerSHARC PCLK to be run at different rates and out of phase.

$$WAIT \geq ceil\left(6 \cdot \frac{f_{LCLK\_34}}{f_{LCLK\_TSHARC}}\right)$$

WAIT ensures that the amount of time the AD6634 needs to wait to begin data transmission is at least equal to the minimum amount of time the TigerSHARC is expecting it to wait. If the PCLK of the AD6634 is out of phase with the PCLK of the TigerSHARC and the argument to the ceil() function is an integer, then WAIT must be strictly greater than the value given in the above formula. If the LCLKs are in phase, then the maximum output data rate is

$$f_{LCLK\_34} \leq \frac{15}{6} \cdot f_{LCLK\_TSHARC}$$

otherwise it is

$$f_{LCLK\_34} \leq \frac{14}{6} \cdot f_{LCLK\_TSHARC}$$

TigerSHARC Configuration

Since the AD6634 is always the transmitter in this link and the TigerSHARC is always the receiver, the following values can be programmed into the LCTL register for the link port used to receive AD6634 output data. "User" means that the actual register value depends on the user's application.

VERE	**0**
SPD	**User**
LTEN	**0**
PSIZE	**1**
TTOE	**0**
CERE	**0**
LREN	**1**
RTOE	**1**

TigerSHARC LCTLx Register Configuration

AD6634 MEMORY MAP

Ch Address	Register	Bit Width	Comments
00-7F	Coefficient Memory(CMEM)	20	128x20-bit Memory
80	CHANNEL SLEEP	1	0: SLEEP bit from EXT_ADDRESS 3
81	Soft_Sync Control Register	2	1: Hop 0: Start
82	Pin_SYNC Control Register	3	2: First SYNC Only 1: Hop_En 0: Start_En
83	Start Hold-Off Counter	16	Start Hold-Off Value
84	NCO Frequency Hold-Off Counter	16	NCO_FREQ Hold-Off Value
85	NCO Frequency Register 0	16	NCO_FREQ[15:0]
86	NCO Frequency Register 1	16	NCO_FREQ[31:16]
87	NCO Phase Offset Register	16	NCO_PHASE[15:0]
88	NCO Control Register	9	8-7: SYNC Input Select[1:0] 6: WB Input Select B/A 5-4: Input Enable Control 11: Clock on IEN transition to Low 10: Clock on IEN transition to High 01: Clock on IEN high 00: Mask on IEN low 3: Clear Phase Accumulator on HOP 2: Amplitude Dither 1: Phase Dither 0: By-Pass (A-Input -> I-Path, B -> Q)
89-8F	Unused		

Table 8. Channel Address Memory Map

0x00-0x7F: Coefficient Memory(CMEM)
This is the Coefficient Memory(C-MEM) used by the RCF. It is memory mapped as 128 words by 20 bits. A second 128 words of RAM may be accessed via this same location by writing bit 8 of the RCF control register high at channel address 0xA4. The filter calculated will always use the same coefficients for I and Q. By using memory from both of these 128 blocks a filter up to 160 taps can be calculated. Multiple filters can be loaded and selected with a single internal access to the Coefficient Offset Register at channel address 0xA3.

0x80: Channel Sleep Register
This register contains the SLEEP bit for the Channel. When this bit is high then the channel is placed in a low power state. When this bit is low then the channel processes data. Note that in serial slave mode, the /RESET pin needs to be held low for several SCLK cycles to insure that it will program this bit high. This bit can also be set by accessing the SLEEP register at external address 3. When the External SLEEP register is accessed then all four channels are accessed simultaneously and the SLEEP bits of the channels are set appropriately.

0x81: Soft_SYNC Register
This register is used to initiate SYNC events through the micro port. If the Hop bit is written high then the Hop Hold-Off Counter at address 0x84 is loaded and begins to count down. When this value reaches 1 then the NCO Frequency register used by the NCO accumulator, is loaded with the data from channel addresses 0x85 and 0x86. When the Start bit is set high then the Start Hold-Off Counter is loaded with the value at address 0x83 and begins to count down. When this value hits 1 then the Sleep bit in address 0x80 is dropped low and the channel is started.

0x82: Pin_SYNC Register
This register is used to control the functionality of the SYNC pins. Any of the four SYNC pins can be chosen and monitored by the channel. The channel can be configured to initiate either a Start or Hop SYNC event by setting the Hop or Start bit high. These bits function as enables so that when a SYNC pulse occurs then either the Start or Hop Hold-Off Counters are activated in the same manner as with a Soft_SYNC.

0x83: Start Hold-Off Counter
The Start Hold-Off Counter is loaded with the value written to this address when a Start_Sync is initiated. It can be initiated by either a Soft_SYNC or Pin_SYNC. The counter begins decrementing and when it reaches a value of 1 the channel is brought out of SLEEP and begins processing data. If the channel is already running then the phase of the filters are adjusted such that multiple AD6634s can be synchronized. A periodic pulse on the SYNC pin can be used in this way to adjust the timing of the filters with the resolution of the ADC sample clock. If this register is written to a 1 then the Start will occur immediately when the SYNC comes into the channel. If it is written to a 0 then no SYNC will occur.

0x84: NCO Frequency Hold-Off Counter
The NCO Frequency Hold-Off Counter is loaded with the value written to this address when either a Soft_SYNC or Pin_SYNC comes into the channel. The Counter begins counting down so that when it reaches 1 the NCO frequency word is updated with the values of addresses 0x85 and 0x86. This is known as a Hop or Hop_SYNC. If this register is written to a 1 then the NCO Frequency will be updated immediately when the SYNC comes into the channel. If it is written to a 0 then no HOP will occur. NCO HOPs can be either phase continuous or non-phase continuous depending upon the state of bit 3 of the NCO control register at channel address 0x88. When this bit is low then the Phase Accumulator of the NCO is not cleared but starts to add the new NCO Frequency word to the accumulator as soon as the SYNC occurs. If this bit is high then the Phase Accumulator of the NCO is cleared to 0 and the new word is then accumulated.

0x85: NCO Frequency Register 0
This register represents the 16 LSBs of the NCO Frequency word. These bits are shadowed and are not updated to the register used for the processing until the channel is either brought out of SLEEP or a Soft_SYNC or Pin_SYNC has been issued. In the latter two cases the register is updated when the Frequency Hold-Off Counter hits a value of 1. If the Frequency Hold-Off Counter is set to 1 then the register will be updated as soon as the shadow is written.

0x86: NCO Frequency Register 1
This register represents the 16 MSBs of the NCO Frequency word. These bits are shadowed and are not updated to the register used for the processing until the channel is either brought out of SLEEP or a Soft_SYNC or Pin_SYNC has been issued. In the latter two cases the register is updated only when the Frequency Hold-Off Counter hits a value of 1. If the Frequency Hold-Off Counter is set to 1 then the register will be updated as soon as the shadow is written.

0x87: NCO Phase Offset Register
This register represents a 16-bit phase offset to the NCO. It can be interpreted as values ranging from 0 to just under 2π.

0x88: NCO Control Register
This 9-bit Register controls features of the NCO and the channel. The bits are defined below. For more detail the NCO section should be consulted.

Bits 8-7 of this register choose which of the four SYNC pins are used by the channel. The SYNC pin selected can be used to initiate a START, HOP, or timing adjustment to the Channel. The Synchronization Section of the Data-Sheet provides more details on this.

Bit 6 of this register defines whether the A or B input port is used by the channel. If this bit is low then the A Input Port is selected and if this bit is high the B Input Port is selected. Each input port consists of a 14-bit input mantissa(INx[13:0]), a 3-bit exponent(EXPx[2:0]) and a input enable pin IENx. The x represents either A or B.

Bits 5-4 determine how the sample clock for the channel is derived from the high speed CLK signal. There are four possible choices. Each is defined below but for further detail the NCO section of the data sheet should be consulted.

When these bits are 00 then the input sample rate (f_{samp}) of the channel is equal to the rate of the high speed CLK signal. When IEN is low the data going into the channel is masked to 0. This is an appropriate mode for TDD systems where the receiver may wish to mask off the transmitted data yet still remain in the proper phase for the next receive burst. When these bits are 01 then the input sample rate is determined by the fraction of the rising edges of CLK on which the IEN input is high. For Example if IEN toggles on every rising edge of CLK then the IEN signal will only be sampled high on 1 out of every 2 rising edges of CLK. This means that the input sample rate f_{samp} will be ½ the CLK rate.

When these bits are 10 then the input sample rate is determined by the rate at which the IEN pin toggles. The data that is captured on the rising edge of CLK after IEN transitions from low to high is processed. When these bits are 11 then the accumulator and sample CLK are determined by the rate at which the IEN pin toggles. The data that is captured on the rising edge of CLK after IEN transitions from high to low is processed. For example, control modes 10 and 11 can be used to allow interleaved data from either the A or B input ports and then assigned to the respective channel. The IEN pin selects the data such that a channel could be configured in mode 10 and another could be configured in mode 11.

Bit 3 determines whether or not the phase accumulator of the NCO is cleared when a Hop occurs. The Hop can originate

from either the Pin_SYNC or Soft_SYNC. When this bit is set to 0 the Hop is phase continuous and the accumulator is not cleared. When this bit is set to 1 the accumulator is cleared to 0 before it begins accumulating the new frequency word. This is appropriate when multiple channels are hopping from different frequencies to a common frequency.

Bits 2-1 control whether or not the dithers of the NCO are activated. The use of these features is heavily determined by the system constraints. Consult the NCO section of the data sheet for more detailed information on the use of dither.

Bit 0 of this register allows the NCO Frequency translation stage to be bypassed. When this occurs the data from the A Input Port is passed down the I path of the channel and the data from the B Input Port is passed down the Q path of the channel. This allows a real filter to be performed on baseband I and Q data.

AD6634 MEMORY MAP Continued

Ch Address	Register	Bit Width	Comments
90	rCIC2 Decimation – 1	12	M_{rCIC2}-1
91	rCIC2 Interpolation – 1	9	L_{rCIC2}-1
92	rCIC2 Scale	12	11: Exponent Invert 10: Exponent Weight 9-5: rCIC2_QUIET[4:0] 4-0: rCIC2_LOUD[4:0]
93	Reserved	8	Reserved(Must be written low)
94	CIC5 Decimation –1	8	M_{CIC5}-1
95	CIC5 Scale	5	4-0: CIC5_SCALE[4:0]
96	Reserved	8	Reserved(Must be written low)
97-9F	Unused		
A0	RCF Decimation – 1	8	M_{RCF}-1
A1	RCF Decimation Phase	8	P_{RCF}
A2	RCF Number of Taps –1	8	N_{Taps}-1
A3	RCF Coefficient Offset	8	CO_{RCF}
A4	RCF Control Register	11	10: RCF By-pass BIST 9: RCF Input Select (own 0, other 1) 8: Program RAM Bank 1/0 7: Use Common Exponent 6: Force Output Scale 5-4: Output Format 1x: Floating Point 12+4 01: Floating Point 8+4 00: Fixed Point 3-0: Output Scale
A5	BIST Signature for I path	16	BIST-I
A6	BIST Signature for Q path	16	BIST-Q
A7	# of BIST outputs to accumulate	20	19-0: # of outputs(Counter Value Read)
A8	RAM BIST Control Register	3	2: D-RAM Fail/Pass 1: C-RAM Fail/Pass 0: RAM BIST Enable
A9	Serial Port Control Register	10	9: Map RCF Data to BIST registers 8-7: I_SDFS Control 1x: Separate I and Q SDFS pulses 01: SDFS high for entire frame 00: Single SDFS pulse 6-5: SOWLx 1x: 24-bit words 01: 16-bit words 00: 12-bit words 4: SBMx

			3-0: SDIVx[3:0]

Table 8. Channel Address Memory Map

0x90: rCIC2 Decimation – 1 (M_{rCIC2}-1)
This register is used to set the decimation in the rCIC2 filter. The value written to this register is the decimation minus one. The rCIC2 decimation can range from 1 to 4096 depending upon the Interpolation of the channel. The decimation must always be greater than the interpolation. M_{rCIC2} must be chosen larger than L_{rCIC2} and both must be chosen such that a suitable rCIC2 Scalar can be chosen. For more details the rCIC2 section should be consulted

0x91: rCIC2 Interpolation – 1 (L_{rCIC2}-1)
This register is used to set the interpolation in the rCIC2 filter. The value written to this register is the interpolation minus one. The rCIC2 interpolation can range from 1 to 512 depending upon the decimation of the rCIC2. There is no timing error associated with this interpolation. See the rCIC2 section of the data sheet for further details.

0x92: rCIC2 Scale
The rCIC2 Scale register is used to provide attenuation to compensate for the gain of the rCIC2 and to adjust the linearization of the data from the floating-point input. The use of this scale register is influenced both by the rCIC2 growth and Floating Point Input Port Considerations. The rCIC2 section should be consulted for details. The rCIC2 scalar has been combined with the Exponent Offset and will need to be handled appropriately in both the Input Port and rCIC2 sections.

Bit 11 determines the polarity of the exponent. Normally, this bit will be cleared unless and ADC such as the AD6600 is used, in which case this bit will be set.

Bit 10 determines the weight of the Exponent word associated with the input port. When this bit is low then each exponent step is considered to be worth 6.02dB. When this bit is high then each exponent step is considered to be worth 12.02dB.

Bits 9-5 are the actual scale value used when the Level Indicator, LI pin associated with this channel is active.

Bits 4-0 are the actual scale value used when the Level Indicator, LI pin associated with this channel is active.

0x93:
Reserved(Must be written low)

0x94: CIC5 Decimation – 1 (M_{CIC5}-1)
This register is used to set the decimation in the CIC5 filter. The value written to this register is the decimation minus one. Although this is an 8-bit register the decimation is usually limited to between 1 and 32. Decimations higher than 32 would require more scaling than the CIC5 is capable of.

0x95: CIC5 Scale
The CIC5 Scale factor is used to compensate for the growth of the CIC5 filter. Consult the CIC5 section for details.

0x96:
Reserved (Must be written low)

0xA0: RCF Decimation – 1 (M_{RCF}-1)
This register is used to set the decimation of the RCF stage. The value written is the decimation minus one. Although this is an 8-bit register which allows decimation up to 256, for most filtering scenarios the decimation should be limited between 1 and 32. Higher decimations are allowed but the alias protection of the RCF may not be acceptable for some applications.

0xA1: RCF Decimation Phase (P_{RCF})
This register allows any one of the M_{RCF} phases of the filter to be used and can be adjusted dynamically. Each time a filter is started then this phase is updated. When a channel is synchronized then it will retain the phase setting chosen here. This can be used as part of a timing recovery loop with an external processor or can allow multiple RCFs to work together while using a single RCF pair. The RCF section of the data sheet should be consulted for further details.

0xA2: RCF Number of Taps minus one (N_{RCF}-1)
The number of taps for the RCF filter minus one is written here.

0xA3: RCF Coefficient Offset (CO_{RCF})
This register is used to specify which section of the 256-word coefficient memory is used for a filter. It can be used to select between multiple filters that are loaded into memory and referenced by this pointer. This register is shadowed and the filter pointer is updated every time a new filter is started. This allows the Coefficient Offset to be written even while a filter is being computed with disturbing operation. The next sample that comes out of the RCF will be with the new filter.

0xA4: RCF Control Register
The RCF Control Register is an 11-bit register that controls general features of the RCF as well as output formatting. The bits of this register and their functions are described below.

Bit 10 bypasses the RCF filter and sends the CIC5 output data to the BIST-I and BIST-Q registers. The 16 MSBs of the CIC5 data can be accessed from this register if bit 9 of the Serial Control Register at channel address 0xA9 is set.

Bit 9 of this register controls the source of the input data to the RCF. If this bit is 0 then the RCF processes the output data of it's own channel. If this bit is 1 then it processes the

data from the CIC5 of another channel. The CIC5 that the RCF is connected to when this bit is 1 are shown in the table below. These can be used to allow multiple RCFs to be used together to process wider bandwidth channels. See the Multi-Processing section of the data-sheet for further details.

Channel	RCF Input Source When Bit-9 is 1
0	1
1	0
2	1
3	1

Table 9. RCF Input Configurations

Bit 8 is used as an extra address to allow a second block of 128 words of CMEM to be addressed by the channel addresses at 0x00-0x7F. If this bit is 0 then the first 128 words are written and if this bit is 1 then a second 128 words is written. This bit is only used to program the Coefficient Memory. It is not used in any way by the processing and filters longer than 128 taps can be performed.

Bit 7 is used to help control the output formatting of the AD6634s RCF data. This bit is only used when the 8+4 or 12+4 floating-point modes are chosen. These modes are enable by bits 5 and 4 of this register below. When this bit is 0 then the I and Q output exponents are determined separately based on their individual magnitudes. When this bit is 1 then the I and Q data is a Complex Floating-Point number where I and Q use a single exponent that is determined based on the maximum magnitude of I or Q.

Bit 6 is used to force the Output Scale Factor in bits 3-0 of this register to be used to scale the data even when one of the Floating Point Output Modes is used. If the number was too large to represent with the Output Scale chosen then the mantissas of the I and Q data clip and do not overflow.

Bits 5 and 4 choose the output formatting option used by the RCF data. The options are defined in the table below and are discussed further in the output format section of the data sheet.

Bit Values	Output Option
1x	12-bit Mantissa and 4-bit Exponent(12+4)
01	8-bit Mantissa and 4-bit Exponent(8+4)
00	Fixed Point Mode

Table 10. Output Formats

Bits 3-0 of this register represent the Output Scale Factor of the RCF. It is used to scale the data when the output format is in fixed-point mode or when the Force Exponent bit is high.

0xA5: BIST Register for I
This register serves two purposes. The first is to allow the complete functionality of the I data path in the channel to be tested in the system. The BIST section of the data sheet should be consulted for further details. The second function is to provide access to the I output data through the micro-port. To accomplish this the Map RCF data to BIST bit in the Serial Port Control register, 0xA9, should be set high. 16-bits of I data can then be read through the micro port in either the 8+4, 12+4, 12 bit linear or 16-bit linear output modes. This data may come from either the formatted RCF output or the CIC5 output.

0xA6: BIST Register for Q
This register serves two purposes. The first is to allow the complete functionality of Q data path in the channel to be tested in the system. The BIST section of the data sheet should be consulted for further details. The second function is to provide access to the Q output data through the micro-port. To accomplish this the Map RCF data to BIST bit in the Serial Port Control register, 0xA9, should be set high. 16-bits of Q data can then be read through the micro port in either the 8+4, 12+4, 12 bit linear or 16-bit linear output modes. This data may come from either the formatted RCF output or the CIC5 output.

0xA7: BIST Control Register
This register controls the number of outputs of the RCF or CIC filter that are observed when a BIST test is performed. The BIST signature registers at addresses 0xA5 and 0xA6 will observe this number of outputs and then terminate. The loading of this register also starts the BIST engine running. Details of how to utilize the BIST circuitry are defined in the BIST section of the data sheet.

0xA8: RAM BIST Control Register
This register is used to test the memories of the AD6634 should they ever be suspected of a failure. Bit 0 of this register is written with a 1 when the channel is in SLEEP and the user waits for 1600 CLKs and then polls the bits. If bit 1 is high then the CMEM failed the test and if bit 2 is high then the data memory used by the RCF failed the test.

0xA9: Serial Port Control Register
This register controls the serial port of the AD6634 and along with the RCF control register it helps to determine the output format.

Bit 9 of this register allows the RCF or CIC5 data to be mapped to the BIST registers at addresses 0xA5 and 0xA6. When this bit is 0 then the BIST register is in signature mode and ready for a self-test to be run. When this bit is 1 then the output data from the RCF after formatting or the CIC5 data is mapped to these registers and can be read through the micro-port. In addition when this bit is high the DRx pin for the channel delivers a 1 CLK cycle wide pulse that can be used to synchronize the host processor with the AD6634. This signal is a 1 SCLK cycle wide pulse when this bit is 0.

Bits 8 and 7 control the output format of the SDFS pulse. When these bits are 00 then there is a single SCLK cycle wide pulse for the I and Q data. When these bits are 01 then the SDFS signal is high for all of the bits shifted during the serial frame. When these bits are 10 or 11 then there are two SDFS pulses that are each 1 SCLK cycle wide. One pulse precedes the I word of data and the second precedes the Q word of data. When a serial port is configured as a serial slave then it should be in the first mode with these bits set to 00.

Bits 6 and 5 determine the serial word length used by the serial port. If these bits are 00 then the serial ports uses 12 bit words and shifts 12 bits of I followed by 12 bits of Q with each shifted MSB first. . If these bits are 01 then the serial ports uses 16 bit words and shifts 16 bits of I followed by 16 bits of Q with each shifted MSB first. . If these bits are 1x then the serial ports uses 24 bit words and shifts 24 bits of I followed by 24 bits of Q with each shifted MSB first. When the fixed point output option is chosen from the RCF control register then these bits also set the rounding correctly in the output formatter of the RCF.

Bit 4 of this register controls whether the Serial Port is a Master or Slave. This register powers up low so that the serial port is a slave in order to avoid contention problems on the output drivers. The serial port for channel 0 does not use this bit. The Master/Slave status of Serial Port 0 is set by the SBM0 pin.

Bits 3-0 control the rate of the SCLKx signal when the channel is master. This four-bit bus can set the SCLK as a division of the master CLK from 1 to 16 with approximately a 50% duty cycle. The SCLK can be generated and run up to a maximum of 80 MHz. The serial division bits from this register are not used for serial port 0. The external SDIV[3:0] pins are used to determine this for serial port 0.

Memory Map for Input Port Control Registers

Ch Address	Register	Bit Width	Comments
00	Lower Threshold A	10	9-0: Lower Threshold for Input A
01	Upper Threshold A	10	9-0: Upper Threshold for Input A
02	Dwell Time A	20	19-0: Minimum Time below Lower Threshold A
03	Gain Range A Control Register	5	4: Output Polarity LIA-A & LIA-B 3: Interleaved Channels 2-0: Linearization Hold-Off Register
04	Lower Threshold B	10	9-0: Lower Threshold for Input B
05	Upper Threshold B	10	9-0: Upper Threshold for Input B
06	Dwell Time B	20	19-0: Minimum Time below Lower Threshold B
07	Gain Range B Control Register	5	4: Output Polarity LIB-A & LIB-B 3: Interleaved Channels 2-0: Linearization Hold-Off Register

In order to access the Input Port Registers the Program Gain Control bit should be written high. The CAR is then written with the address to the correct Input Port Register.

Memory Map for Output Port Control Registers

Ch Address	Register	Bit Width	Comments
08	HB A Control Register	4	3: Reserved 2-1: HB A Signal Interleaveing 11 All 4 Channels 10 Chs 0, 1, 2 01 Chs 2,3 00 Ch 0 0: ByPass
09	HB-B Control Register	2	1: HB A Signal Interleaveing 1 Chs 2, 3 0 Ch 2 0: ByPass
0A	AGC A Control Register	8	7-1: Reserved 0: Bypass
0B	AGC A Desired Level	16	15-0: Desired Output Power Level or clipping energy
0C	AGC A Signal Gain	16	15-0: Gain set/monitor register
0D	AGC A Loop Gain 1	16	15-0: Loop Gain Set Register 1
0E	AGC A Loop Gain 2	16	15-0: Loop Gain Set Register 2
0F	AGC A r Value	8	7-0: Sets the Loss of an integrator
10	AGC A Clipping Error	16	For monitoring the Clipping Level
11	AGC B Control Register	8	7-1: Reserved 0: Bypass
12	AGC B Desired Level	16	15-0: Desired Output Power Level or clipping energy
13	AGC B Signal Gain	16	15-0: Gain set/monitor register
14	AGC B Loop Gain 1	16	15-0: Loop Gain Set Register 1
15	AGC B Loop Gain 2	16	15-0: Loop Gain Set Register 2
16	AGC B r Value	8	7-0: Sets the Loss of an integrator
17	AGC B Clipping Error	16	For monitoring the Clipping Level
18	Parallel A Control	8	7-6: Reserved 5: Parallel Port Data Format 1: 8-bit Parallel I, Q 0: 16-bit Interleaved I, Q 4: Channel 3 3: Channel 2 2: Channel 1 / AGC B Enable 1: Channel 0 / AGC A Enable 0: AGC_CH Select 1: Data comes from AGCs 0: Data comes from Channels
19	Link A Control	8	7: Link Port A Enable 6-3: Wait 2: No Gain Word 1: Don't output gain word

			0: Output gain word 1: Channel Data Interleaved 1: 2 channel mode/separate AB 0: 4 channel mode/AB same port 0: AGC_CH Select 1: Data comes from AGCs 0: Data comes from Channels
1A	Parallel B Control	8	7-6: Reserved 5: Parallel Port Data Format 1: 8-bit Parallel I, Q 0: 16-bit Interleaved I, Q 4: Channel 3 3: Channel 2 2: Channel 1 / AGC B Enable 1: Channel 0 / AGC A Enable 0: AGC_CH Select 1: Data comes from AGCs 0: Data comes from Channels
1B	Link B Control	8	7: Link Port B Enable 6-3: Wait 2: No Gain Word 1: Don't output gain word 0: Output gain word 1: Channel Data Interleaved 1: 2 channel mode/separate AB 0: 4 channel mode/AB same port 0: AGC_CH Select 1: Data comes from AGCs 0: Data comes from Channels
1C	Port Clock Control	3	2-1: PCLK divisor 0: PCLK Master/Slave[1] 0: Slave 1: Master

1: PCLK boots as slave

0x08 Half band A Control Register
Half band A can be used to interleave the data streams of multiple channels and interpolate by two providing a maximum output data rate of 4x the chip rate. It can be configured to listen to all four channels; channels 0, 1, 2 and 3; channels 0 and 1; or only channel 0. Half band A is bypassed when bit 0 = 1, in which case the outputs of the RCFs are directly sent to the AGC. The channel data streams still get interleaved with the half band bypassed, but they are not filtered and interpolated. The maximum data rate from this configuration would be 2x the chip rate.

0x09 Half band B Control Register
Half band B can be used to interleave the data streams of multiple channels and interpolate by two providing a maximum output data rate of 4x the chip rate. It can be configured to listen to channels 2 and 3; or only channel 2. Half band B is bypassed when bit 0 = 1, in which case the outputs of the RCFs are directly sent to the AGC. The channel data streams still get interleaved with the half band bypassed, but they are not filtered and interpolated. The maximum data rate from this configuration would be 2x the chip rate.

0x0A AGC A Control Register

Flexibility of AGC control is still being determined, so most of these values are still reserved.

Bit 0 = 1 bypasses AGC A.

0x0B AGC A Desired Level
This 16-bit value determines what the desired level of the gain-data product. The difference is fed through the AGC feedback loop to adjust the gain. This can either be the desired signal level or the desired clipping level. This status will be determined by the AGC A control register at address 0x0A.

0x0C AGC A Signal Gain
To be determined

0x0D AGC A Loop Gain 1
This 16-bit programmable value sets the K value of AGC A. This is the amount by which the error signal (whether clipping error or signal level error) is scaled before it is input to the loop filter.

0x0E AGC A Loop Gain 2
To be determined.

0x0F AGC A r Value

This 8-bit programmable value adjusts the loop filter's time constant of AGC A, which determines the window for calculating the peak-to-average ratio of the input signal.

0x10 AGC A Clipping Error
This 16-bit programmable value determines how much clipping overhead is provided when calculating the error due to clipping. This is useful only when the AGC A is configured to adjust the gain based on clipping level.

0x11 AGC B Control Register
Flexibility of AGC control is still being determined, so most of these values are still reserved.

Bit 0 = 1 bypasses AGC B.

0x12 AGC B Desired Level
This 16-bit value determines what the desired level of the gain-data product. The difference is fed through the AGC B feedback loop to adjust the gain. This can either be the desired signal level or the desired clipping level. This status will be determined by the AGC B control register at address 0x11.

0x13 AGC B Signal Gain
To be determined.

0x14 AGC B Loop Gain 1
This 16-bit programmable value sets the K value of AGC B. This is the amount by which the error signal (whether clipping error or signal level error) is scaled before it is input to the loop filter.

0x15 AGC B Loop Gain 2
To be determined.

0x16 AGC B r Value
This 8-bit programmable value adjusts the loop filter's time constant of AGC B, which determines the window for calculating the peak-to-average ratio of the input signal.

0x17 AGC B Clipping Error
This 16-bit programmable value determines how much clipping overhead is provided when calculating the error due to clipping. This is useful only when the AGC B is configured to adjust the gain based on clipping level.

0x18 Parallel Port Control A
When the serial data port is disabled, data is output through either a parallel port interface or a link port interface. When 0x19 bit 7 = 0, the use of link port A is disabled and the use of parallel port A is enabled. The parallel port provides different data modes for interfacing with DSPs or FPGAs.

Bit 0 selects which data is output on parallel port A. When bit 0 = 0, parallel port A outputs data from the RCF according to the format specified by bits 1 through 4. When bit 0 = 1, parallel port A outputs the data from the AGCs according to the format specified by bits 1 and 2.

In AGC mode, bit 0 = 1 and bit 1 determines if parallel port A is able to output data from AGC A and bit 2 determines if parallel port A is able to output data from AGC B. The order of output depends on the rate of triggers from each AGC, which in turn is determined by the decimation rate of the channels feeding it. In channel mode, bit 0 = 0 and bits 1 through 4 determine which combination of the four processing channels is output. The output order depends on the rate of triggers received from each channel, which is determined by the decimation rate of each channel. The channel output indicator pins can be used to determine which data came from which channel.

Bit 5 determines the format of the output data words. When bit 5 = 0, parallel port A outputs 16-bit words on its 16-bit bus. This means that I and Q data are interleaved and the IQ indicator pin determines whether data on the port is I data or Q data. When bit 5 = 1, parallel port A is outputting an 8-bit I word and an 8-bit Q word at the same time, and the IQ indicator pins will be HIGH.

0x19 Link Port Control A
When the serial data port is disabled, data is output through either a parallel port interface or a link port interface. The link port provides an efficient data link between the AD6634 and a TigerSHARC DSP and can be enabled by setting bit 7 = 1.

Bit 0 selects which data is output on link port A. When bit 0 =0, link port A outputs data from the RCF according to the format specified by bit 1. When bit 0 = 1, link port A outputs the data from the AGCs according to the format specified by bits 1 and 2.

Bit 1 has two different meanings that depend on whether data is coming from the AGCs or from the RCFs. When data is coming from the RCFs (bit 0 = 0), bit 1 selects between two and four channel data mode. Bit 1 = 1 indicates link port A transmits RCF IQ words alternately from channels 0 and 1. When bit 1 = 1, link port A outputs RCF IQ words from each of the four channels in succession: 0, 1, 2, then 3. However, when AGC data is selected (bit 0 = 1), bit 1 selects the AGC data output mode. In this mode, when bit 1 = 1, link port A outputs AGC A IQ and gain words. With this mode, gain words must be included by setting bit 2 = 0. However, if bit 0 = bit 1 = 0, then AGC A and B are alternately output on link port A and the inclusion or exclusion of the gain words is determined by bit 2.

Bit 2 selects if gain words are included or not in the data output. If bit 1 = 1, bit 2 =0. Since the gain words are only two bytes long and the IQ words are four bytes long, the gain words are padded with zeros to give a full 16-byte

TigerSHARC quad-word. If AGC output is not selected (bit 0 = 0) then this bit can be any value.

Bits 6 through 3 specify the programmable delay value for link port A between the time the link port receives a data ready from the receiver and the time it transmits the first data word. The link port must wait at least 6 cycles of the receiver's clock, so this value allows the user to use clocks of differing frequency and phase for the AD6634 link port and the TigerSHARC link port. There is more information on the limitations and relationship of these clocks in the section on Link Ports.

0x1A Parallel Port Control B

When the serial data port is disabled, data is output through either a parallel port interface or a link port interface. When 0x1B bit 7 = 0, the use of link port B is disabled and the use of parallel port B is enabled. The parallel port provides different data modes for interfacing with DSPs or FPGAs.

Bit 0 selects which data is output on parallel port B. When bit 0 = 0, parallel port B outputs data from the RCF according to the format specified by bits 1 through 4. When bit 0 = 1, parallel port B outputs the data from the AGCs according to the format specified by bits 1 and 2.

In AGC mode, bit 0 = 1 and bit 1 determines if parallel port B is able to output data from AGC A and bit 2 determines if parallel port B is able to output data from AGC B. The order of output depends on the rate of triggers from each AGC, which in turn is determined by the decimation rate of the channels feeding it. In channel mode, bit 0 = 0 and bits 1 through 4 determine which combination of the four processing channels is output. The output order depends on the rate of triggers received from each channel, which is determined by the decimation rate of each channel. The channel output indicator pins can be used to determine which data came from which channel.

Bit 5 determines the format of the output data words. When bit 5 = 0, parallel port B outputs 16-bit words on its 16-bit bus. This means that I and Q data are interleaved and the IQ indicator pin determines whether data on the port is I data or Q data. When bit 5 = 1, parallel port B is outputting an 8-bit I word and an 8-bit Q word at the same time, and the IQ indicator pins will be HIGH.

0x1B Link Port Control B

When the serial data port is disabled, data is output through either a parallel port interface or a link port interface. The link port provides an efficient data link between the AD6634 and a TigerSHARC DSP and can be enabled by setting bit 7 = 1.

Bit 0 selects which data is output on link port B. When bit 0 =0, link port B outputs data from the RCF according to the format specified by bit 1. When bit 0 = 1, link port B outputs the data from the AGCs according to the format specified by bits 1 and 2.

Bit 1 has two different meanings that depend on whether data is coming from the AGCs or from the RCFs. When data is coming from the RCFs (bit 0 = 0), bit 1 selects between two and four channel data mode. Bit 1 = 1 indicates link port A transmits RCF IQ words alternately from channels 0 and 1. When bit 1 = 1, link port B outputs RCF IQ words from each of the four channels in succession: 0, 1, 2, then 3. However, when AGC data is selected (bit 0 = 1), bit 1 selects the AGC data output mode. In this mode, when bit 1 = 1, link port B outputs AGC B IQ and gain words. With this mode, gain words must be included by setting bit 2 = 0. However, if bit 0 = bit 1 = 0, then AGC A and B are alternately output on link port B and the inclusion or exclusion of the gain words is determined by bit 2.

Bit 2 selects if gain words are included or not in the data output. If bit 1 = 1, bit 2 =0. Since the gain words are only two bytes long and the IQ words are four bytes long, the gain words are padded with zeros to give a full 16-byte TigerSHARC quad-word. If AGC output is not selected (bit 0 = 0) then this bit can be any value.

Bits 6 through 3 specify the programmable delay value for link port B between the time the link port receives a data ready from the receiver and the time it transmits the first data word. The link port must wait at least 6 cycles of the receiver's clock, so this value allows the user to use clocks of differing frequency and phase for the AD6634 link port and the TigerSHARC link port. There is more information on the limitations and relationship of these clocks in the section on Link Ports.

0x1C Port Clock Control

Bit 0 determines whether PCLK is supplied externally by the user or derived internally in the AD6634. If PCLK is derived internally from CLK (Bit 0 = 1), it is output through the PCLK pin as a master clock. For most applications, PCLK will be provided by the user as an input to the AD6634 via the PCLK pin.

Bits 2 and 1 allow the user to divide CLK by an integer value to generate PCLK (00 = 1, 01 = 2, 10 = 3, 11 = 4).

MICROPORT CONTROL

The AD6634 has an 8-bit microprocessor port and 4 serial input ports. The use of each of these ports is described separately below. The interaction of the ports is then described. The Microport interface is a multi-mode interface that is designed to give flexibility when dealing with the host processor. There are two modes of bus operation: Intel non-multiplexed mode (INM), and Motorola non-multiplexed mode (MNM). The mode is selected based on host processor and which mode is best suited to that processor. The micro-port has an 8-bit data bus(D[7:0]), 3-bit address bus(A[2:0]), 3 control pins lines (/CS, /DS or /RD, RW or /WR), and one status pin(DTACK or RDY). The functionality of the control signals and status line changes slightly depending upon the mode that is chosen. Refer to the timing diagrams and the following descriptions for details on the operation of both modes.

External Memory Map

The External Memory Map is used to gain access to the Channel Address Space described previously. The 8-bit data and address buses are used to this set of 8 registers that can be seen in the following table. These registers are collectively referred to as the External Interface Registers since they control all accesses to the Channel Address space as well as global chip functions. The use of each of these individual registers is described below in detail. It should be noted that the Serial Control interface to Channel 0 has the same memory map as the micro-port interface and can carry out the EXACT same functions, although at a slower rate.

Access Control Register(ACR)

The Access Control Register serves to define the channel or channels that receive an access from the micro-port or serial port 0.

Bit 7 of this register is the Auto-Increment bit. If this bit is a 1 then the CAR register described below will increment its value after every access to the channel. This allows blocks of address space such as Coefficient Memory to be initialized more efficiently.

Bit 6 of the register is the Broadcast bit and determines how bits 5-2 are interpreted. If Broadcast is 0 then bits 5-2, which are refereed to as Instruction bits (Instruction[3:0]), are compared with the CHIP_ID[3:0] pins. The instruction which matches the CHIP_ID[3:0] pins will determine the access. This allows up to 16 chips to be connected to the same port and memory mapped without external logic. This also allows the same serial port of a host processor to configure up to 16 chips. If the Broadcast bit is high the Instruction[3:0] word allows multiple AD6634 channels and/or chips to be configured simultaneously independent of the CHIP_ID[3:0] pins. There are 10 possible instructions that are defined in the table below. This is useful for smart antenna systems where multiple channels listing to a single antenna or carrier can be configured simultaneously. The x's in the table represent don't cares in the digital decoding.

External Memory Map

A[2:0]	Name	Comment
111	Access Control Register (ACR)	7: Auto Increment 6: Broadcast 5-2: Instruction[3:0] 1-0: A[9:8]
110	Channel Address Register (CAR)	7-0: A[7:0]
101	SOFT_SYNC Control Register **(Write Only)**	7: PN_EN 6: Test_MUX_Select 5: Hop 4: Start 3: SYNC 3 2: SYNC 2 1: SYNC 1 0: SYNC 0
100	PIN_SYNC Control Register **(Write Only)**	7: Toggle IEN for BIST 6: First SYNC Only 5: Hop_En 4: Start_En 3: SYNC_EN 3 2: SYNC_EN 2 1: SYNC_EN 1 0: SYNC_EN 0
011	SLEEP **(Write Only)**	7-6: Reserved 5: Access Input Port Control Registers 4: Serial Read 0 3: SLEEP 3 2: SLEEP 2 1: SLEEP 1 0: SLEEP 0
010	Data Register 2 (DR2)	7-4: Reserved 3-0: D[19:16]
001	Data Register 1 (DR1)	15-8: D[15:8]
000	Data Register 0 (DR0)	7-0: D[7:0]

Table 11. External Memory Map

Microport Instructions

Instruction	Comment:
0000	All Chips and all Channels will get the access.
0001	Channel 0,1,2 of all Chips will get the access.
0010	Channel 1,2,3 of all Chips will get the access.
0100	All Chips will get the access.[1]
1000	All Chips with Chip_ID[3:0] = xxx0 will get the access.[1]
1001	All Chips with Chip_ID[3:0] = xxx1 will get the access.[1]
1100	All Chips with Chip_ID[3:0] = xx00 will get the access.[1]
1101	All Chips with Chip_ID[3:0] = xx01 will get the access.[1]
1110	All Chips with Chip_ID[3:0] = xx10 will get the access.[1]
1111	All Chips with Chip_ID[3:0] = xx11 will get the access.[1]

[1]A[9:8] bits control which channel is decoded for the access.

Table 12. Microport Instructions

When broadcast is enabled (bit 6 set high) read back is not valid because of the potential for internal bus contention.

Therefore, if read back is subsequently desired, the broadcast bit should be set low.

Bits 1-0 of this register are address bits that decode which of the four channels are being accessed. If the Instruction bits decode an access to multiple channels then these bits are ignored. If the Instruction decodes an access to a subset of chips then the A[9:8] bits will otherwise determine the channel being accessed.

Channel Address Register (CAR)
This register represents the 8-bit internal address of each channel. If the Auto-Increment bit of the ACR is 1 then this value will be incremented after every access to the DR0 register, which will in turn access the location pointed to by this address. The Channel Address register cannot be read back while the Broadcast bit is set high.

SOFT_SYNC Control Register
External Address [5] is the SOFT_SYNC control register and is write only.

Bit 0-3 of this register are the SOFT_SYNC control bits. These pins may be written to by the controller to initiate the synchronization of a selected channel. Although there are 4 inputs, these do not necessarily go to the channel of the same number. This is fully configurable at the channel level as to which bit to look at. All 4 channels may be configured to synchronize from a single position, or they may be paired or all independent.

Bit 4 determines if the synchronization is to apply to a chip start. If this bit is set, a chip start will be initiated.

Bit 5 determines if the synchronization is to apply to a chip hop. If this bit is set, the NCO frequency will be updated when the when the SOFT_SYNC occurs.

Bit 6 configures how the internal data bus is configured. If this bit is set low, then the internal ADC data buses are configured normally. If this bit is set, then the internal test signals are selected. The internal test signals are configured in Bit 7 of this register.

Bit 7 if set clear, a negative full scale signal is generated and made available to the internal data bus. If this bit is high, then internal pseudorandom sequence generator is enabled and this data is available to the internal data bus. The combined functions of bit 6 and 7 facilitate verification of a given filter design. Also, in conjunction with the MISR registers allows for detailed in-system chip testing. In conjunction with the JTAG test board, very high levels of chip verification can be done during system test, both in the factory and field.

PIN_SYNC Control Register

External Address [4] is the PIN_SYNC control register and is write only.

Bit 0-3 of this register are the SYNC_EN control bits. These pins may be written to by the controller to allow pin synchronization of a selected channel. Although there are 4 inputs, these do not necessarily go to the channel of the same number. This is fully configurable at the channel level as to which bit to look at. All 4 channels may be configured to synchronize from a single position, or they may be paired or all independent.

Bit 4 determines if the synchronization is to apply to a chip start. If this bit is set, a chip start will be initiated when the when the PIN_SYNC occurs.

Bit 5 determines if the synchronization is to apply to a chip hop. If this bit is set, the NCO frequency will be updated when the when the PIN_SYNC occurs.

Bit 6 is used to ignore repetitive synchronization signals. In some applications, this signal may occur periodically. If this bit is clear, each PIN_SYNC will restart/hop the channel. If this bit is set, then only the first occurrence will cause the chip to take action.

Bit 7 is used with bit 6 and 7 of external address 5. When this bit is cleared, the data supplied to the internal data bus simulates a normal ADC. When this bit is set, the data supplied is in the form of a time multiplexed ADC such as the AD6600 (this allows the equivalent of testing in the 4 channel input mode). Internally, when set, this bit forces the IEN pin to toggle as if it were driven by the A/B signal of the AD6600.

SLEEP Control Register
External Address [3] is the sleep register.

Bits 3-0 control the state of each of the channels. Each bit corresponds to one of the possible RSP channels within the device. If this bit is cleared, the channel operates normally. However, when this bit is set, the indicated channel enters a low power sleep mode.

Bit 4 causes the normal RSP data on serial channel 0 to be replaced with read access data. This allows reading the internal registers over the serial bus. It should be noted that in the mode, any RSP data will be superceded by internal access data.

Bit 5 allows access to the Input Control Port Registers at channel addresses 00-07. When this bit is set low, the normal memory map is accessed. However, when this bit is set, it allows access to the Input Port Control Registers. Access to these registers allows the lower and upper thresholds to be set along with dwell time and other features.

When this bit is set, the value in external address 6 (CAR) points to the memory map for the Input Port Control Registers instead of the normal memory map. See Input Port Control Registers Below.

Bit 6-7 are reserved and should be set low.

Data Address Registers
External Address [2-0] form the data registers DR2, DR1 and DR0 respectively. All internal data words have widths that are less than or equal to 20 bits. Accesses to External Address [0] DR0 trigger an internal access to the AD6634 based on the address indicated in the ACR and CAR. Thus during writes to the internal registers, External Address [0] DR0 must be written last. At this point data is transferred to the internal memory indicated in A[9:0]. Reads are performed in the opposite direction. Once the address is set, External Address [0] DR0must be the first data register read to initiate an internal access. DR2 is only 4 bits wide. Data written to the upper 4 bits of this register will be ignored. Likewise reading from this register will produce only 4 LSBs.

Write Sequencing
Writing to an internal location is achieved by first writing the upper two bits of the address to bits 1 through 0 of the ACR. Bits 7:2 may be set to select the channel as indicated above. The CAR is then written with the lower eight bits of the internal address (it doesn't matter if the CAR is written before the ACR as long as both are written before the internal access). Data register 2,(DR2) and register 1 (DR1) must be written first because the write to data register DR0 triggers the internal access. Data register DR0 must always be the last register written to initiate the internal write.

Read Sequencing
Reading from the micro port is accomplished in the same manner. The internal address is set up the same way as the write. A read from data register DR0 activates the internal read, thus register DR0 must always be read first to initiate an internal read followed by DR1and DR2. This provides the 8 LSBs of the internal read through the micro port (D[7:0]). Additional data registers can be read to read the balance of the internal memory.

Read/Write Chaining
The micro port of the AD6634 allows for multiple accesses while /CS is held low (/CS can be tied permanently low if the micro port is not shared with additional devices). The user can access multiple locations by pulsing the /WR or /RD line and changing the contents of the external three bit address bus. External access to the external registers of Table 2 is accomplished in one of two modes using the /CS, /RD, /WR, and MODE inputs. The access modes are Intel Non-Multiplexed mode and Motorola Non-Multiplexed mode. These modes are controlled by the MODE input (MODE=0 for INM, MODE=1 for MNM). /CS, /RD, and /WR control the access type for each mode.

Intel Non-Multiplexed Mode (INM)
MODE must be tied low to operate the AD6634 microprocessor in INM mode. The access type is controlled by the user with the /CS, /RD (/DS), and /WR (RW) inputs. The RDY (/DTACK) signal is produced by the micro port to communicate to the user that an access has been completed. RDY (/DTACK) goes low at the start of the access and is released when the internal cycle is complete. See the timing diagrams for both the read and write modes in the Specifications.

Motorola Non-Multiplexed Mode (MNM)
MODE must be tied high to operate the AD6634 microprocessor in MNM mode. The access type is controlled by the user with the /CS, /DS (/RD), and RW (/WR) inputs. The /DTACK (RDY) signal is produced by the micro port to communicate to the user that an access has been completed. /DTACK (RDY) goes low when an internal access is complete and then will return high after /DS (/RD) is de-asserted. See the timing diagrams for both the read and write modes in the Specifications.

Memory Map for Input Port Control Registers

Ch Address	Register	Bit Width	Comments
00	Lower Threshold A	10	9-0: Lower Threshold for Input A
01	Upper Threshold A	10	9-0: Upper Threshold for Input A
02	Dwell Time A	20	19-0: Minimum Time below Lower Threshold A
03	Gain Range A Control Register	5	4: Output Polarity LIA-A & LIA-B 3: Interleaved Channels 2-0: Linearization Hold-Off Register
04	Lower Threshold B	10	9-0: Lower Threshold for Input B
05	Upper Threshold B	10	9-0: Upper Threshold for Input B
06	Dwell Time B	20	19-0: Minimum Time below Lower Threshold B
07	Gain Range B Control Register	5	4: Output Polarity LIB-A & LIB-B 3: Interleaved Channels 2-0: Linearization Hold-Off Register

Table 13. Input Port Control Registers

Input Port Control Registers

The Input Port control register enables various input related features used primarily for input detection and level control. Depending on the mode of operation, up to 4 different signal paths can be monitored with these registers. These features are accessed by setting bit 5 of external address 3 (Sleep Register) and then using the CAR (external address 6) to address the 8 locations available.

Response to these settings is directed to the LIA-A, LIA-B, LIB-A and LIB-B pins.

Address 00 is the lower threshold for input channel A. This word is 10 bits wide and maps to the 10 most significant bits of the mantissa. If the upper 10 bits are less than or equal to this value, then the lower threshold has been met. In normal chip operation, this starts the Dwell time counter. If the input signal increases above this value, then the counter is reloaded and await the input to drop back to this level.

Address 01 is the upper threshold for input channel A. This word is 10 bits wide and maps to the 10 most significant bits of the mantissa. If the upper 10 bits are greater than or equal to this value, then the upper threshold has been met. In normal chip operation, this will cause the appropriate LI pin (LIA-A or LIA-B) to become active.

Address 02 is the dwell time for input channel A. This sets the time that the input signal must be at or below the lower threshold before the LI pin is de-activated. For the input level detector to work, the Dwell time must be set to at least 1. If set to 0, the LI functions are disabled.

Address 02 has a 20 bit register. When the lower threshold is met following an excursion into the upper threshold, the dwell time counter is loaded and begins to count high speed clock cycles as long as the input is at or below the lower threshold. If the signal increases above the lower threshold, the counter is reloaded and waits for the signal to fall below the lower threshold again.

Address 03 configures input channel A.
Bit 4 determines the polarity of LIA-A and LIA-B. If this bit is clear then the LI signal is high when the upper threshold has been exceeded. However, if this bit is set, the LI pin is low when active. This allows maximum flexibility when using this function.

Bit 3 determines if the input consists of a single channel or TDM channels such as when using the AD6600. If this bit is cleared, then a single ADC is assumed. In this mode, LIA-A functions as the active output indicator. LIA-B provides the compliment of LIA-A. However, if this bit is set, then the input is determined to be dual channel and determined by the state of the IENA pin. If the IENA pin is low, then the input detection is directed to LIA-A. If the IENA pin is high, the input is directed to LIA-B. In either case, bit 4 determines the actual polarity of these signals.

Bit 2-0 determines the internal latency of the gain detect function. When the LIA-A,B pins are made active, they are typically used to change an attenuator or gain stage. Since this is prior to the ADC, there is a latency associated with the ADC and with the settling of the gain change. This register allows the internal delay of the LIA-A,B signal to be programmed.

Addresses 4-7 duplicates address 00-03 for input port B (INB[13:0]).

SERIAL PORT CONTROL

The AD6634 will have 4 serial ports serving as primary data output interfaces. In addition to output data, these ports will provide control paths to the internal functions of the AD6634. Serial Port 0 (SDIN0) can access all of the internal registers for all of the channels while ports 1, 2 and 3 (SDIN1-3) are limited to their local registers only. In this manner, a single DSP could be used to control the AD6634 over the serial port 0 interface. The option is present to use a DSP per channel if needed. In addition to the global access of serial port 0, it has preemptive access over the other serial ports and the micro port.

The Serial Output and Input functions use mainly separate hardware and can largely be considered separate ports that use a common Serial Clock (SCLK). The Serial Input Port is self-framing as described below and allows more efficient use of the Serial Input Bandwidth for Programming. Hence, the state of the SDFS signal has no direct impact on the Serial Input Port. Since the serial input port is self-framing, it is not necessary to wait for an SDFS to perform a serial write. The beginning of a Serial Input Frame is signaled by a Frame bit that appears on the SDI pin. This is the MSB of the Serial Input Frame. After the FRAME bit has been sampled high on the Falling Edge of SCLK a State Counter will start and enable an 11 bit Serial Shifter 4 Serial Clock Cycles later. These 4 SCLK cycles represent the "Don't Care" bits of the Serial Frame that are ignored. After all of the bits are shifted then the Serial Input Port will pass along the 8-bit data and 3-bit address to the arbitration block.

The Serial Word Structure for the SDI input is illustrated in the table below. Only 15 bits are listed so that the second bit in a standard 16-bit serial word is considered the FRAME bit. This is done for compatibility with the AD6620 Serial Input Port. The Shifting order begins with FRAME and shifts the Address MSB first and then the data MSB first.

Frame	x	x	x	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

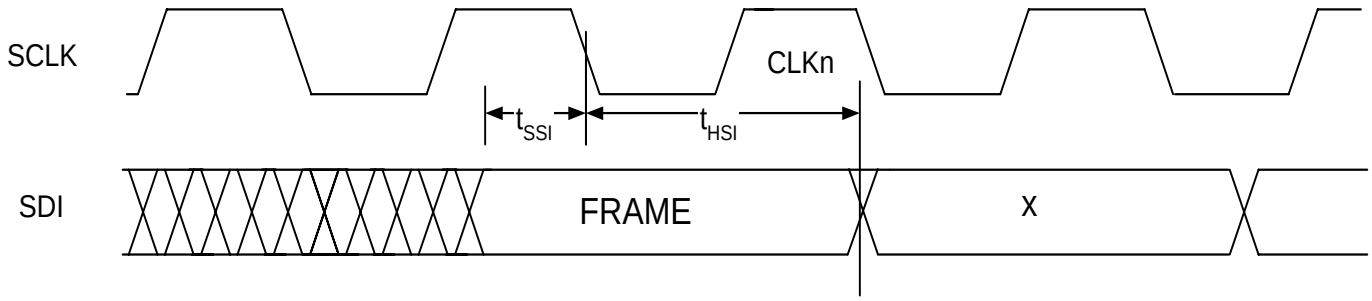


Figure 46. Serial Port Control Timing

JTAG BOUNDARY SCAN

The AD6634 supports a subset of IEEE Standard 1149.1 specification. For additional details of the standard, please see "IEEE Standard Test Access Port and Boundary-Scan Architecture," IEEE-1149 publication from IEEE.

The AD6634 has five pins associated with the JTAG interface. These pins are used to access the on-chip Test Access Port and are listed in the table below.

Name	Pin Number	Description
/TRST	67	Test Access Port Reset
TCLK	68	Test Clock
TMS	69	Test Access Port Mode Select
TDI	72	Test Data Input
TDO	70	Test Data Output

Table 14. Boundary Scan Test Pins

The AD6634 supports four op codes as shown below. These instructions set the mode of the JTAG interface.

Instruction	Op Code
IDCODE	001
BYPASS	111
SAMPLE/PRELOAD	010
EXTEST	000
HIGHZ	011
CLAMP	100

Table 15. Boundary Scan Op Codes

The Vendor Identification Code can be accessed through the IDCODE instruction and has the following format.

MSB Version	Part Number	Manufacturing ID #	LSB Mandatory
0000	0010 0111 1000 1100	000 1110 0101	1

Table 16. Vendor ID Code

A BSDL file for this device is available, please contact Analog Devices Inc. for more information.

EXTEST (3'b000) -> Places the IC into an external boundary-test mode and selects the boundary-scan register to be connected between tdi and tdo. During this, the boundary-scan register is accessed to drive test data off-chip via boundary outputs and receive test data off-chip from boundary inputs.

IDCODE (3'b001) -> Allows the IC to remain in its functional mode and selects device id register to be connected between tdi and tdo. Accessing the id register does not interfere with the operation of the IC.

SAMPLE/PRELOAD (3'b010) -> Allows the IC to remain in normal functional mode and selects the boundary-scan register to be connected between tdi and tdo. The boundary-scan register can be accessed by a scan operation to take a sample of the functional data entering and leaving the IC. Also, test data can be preloaded into the boundary scan register before an EXTEST instruction.

HIGHZ (3'b011) -> Sets all outputs to high impedance state. Selects one-bit bypass register to be connected between tdi and tdo.

CLAMP (3'b100) -> Sets the outputs of the IC to logic levels determined by the boundary-scan register and selects one-bit bypass register to be connected between tdi and tdo. Before this instruction, boundary-scan data can be preloaded with the SAMPLE/PRELOAD instruction.

BYPASS (3'b111) -> Allows the IC to remain in normal functional mode and selects one-bit bypass register between tdi and tdo. During this instruction, serial data is transferred from tdi to tdo without affecting operation of the IC.

INTERNAL WRITE ACCESS

Up to 20-bits of data (as needed) can be written by the process described below. Any high order bytes that are needed are written to the corresponding data registers defined in the external 3-bit address space. The least significant byte is then written to DR0 at address (000). When a write to DR0 is detected, the internal microprocessor port state machine then moves the data in DR2-DR0 to the internal address pointed to by the address in the LAR and AMR.

Write Pseudocode

```
void write_micro(ext_address, int data);

main();
{
/* This code shows the programming of the NCO phase
offset register using the write_micro function as defined
above. The variable address is the External Address
A[2:0] and data is the value to be placed in the external
interface register.

Internal Address = 0x087
 */

// holding registers for NCO phase byte wide access data
int d1, d0;

// NCO frequency word (16-bits wide)
NCO_PHASE = 0xCBEF;

// write ACR
write_micro(7, 0x03 );

// write CAR
write_micro(6, 0x03);

// write DR1 with D[15:8]
d1 = (NCO_PHASE & 0xFF00) >> 8;
write_micro(1, d1);

// write DR0 with D[7:0]
// On this write all data is transferred to the internal address
d0 = NCO_FREQ & 0xFF;
write_micro(0, d0);

}  // end of main
```

INTERNAL READ ACCESS

A read is performed by first writing the CAR and AMR as with a write. The data registers (DR2-DR0) are then read in the reverse order that they were written. First, the Least Significant Byte of the data (D[7:0]) is read from DR0. On this transaction the high bytes of the data are moved from the internal address pointed to by the CAR and AMR into the remaining data registers (DR2-DR1). This data can then be read from the data registers using the appropriate 3 bit addresses. The number of data registers used depends solely on the amount of data to be read or written. Any unused bit in a data register should be masked out for a read.

Read Pseudocode

```
int read_micro(ext_address);

main();
{
/* This code shows the reading of  the first RCF coefficient
using the read_micro function as defined above.  The
variable address is the External Address A[2..0].

Internal Address = 0x000
 */

// holding registers for the coefficient
int d2, d1, d0;

// coefficient  (20-bits wide)
long coefficient;

// write AMR
write_micro(7, 0x00 );

// write LAR
write_micro(6, 0x00);

/* read D[7:0] from DR0,  All data is moved from the
Internal Registers to the interface registers on this access
*/
d0 = read_micro(0) & 0xFF;

// read D[15:8] from DR1
d1 = read_micro(1) & 0xFF;

// read D[23:16] from DR2
d2 = read_micro(2) & 0x0F;

coefficient = d0 + (d1 << 8) + (d2 << 16);

}  // end of main
```