

## Quad 12-Bit Microprocessor-Compatible D/A Converter

AD390\*

### **FEATURES**

Four Complete 12-Bit DACs in One IC Package Linearity Error ± 1/2LSB T<sub>min</sub> – T<sub>max</sub> (AD390K, T) Factory-Trimmed Gain and Offset Buffered Voltage Output Monotonicity Guaranteed Over Full Temperature Range Double-Buffered Data Latches Includes Reference and Buffer Fast Settling: 8µs max to ± 1/2LSB

### PRODUCT DESCRIPTION

The AD390 contains four 12-bit high speed voltage-output digital-to-analog converters in a compact 28-pin hybrid package. The design is based on a proprietary latched 12-bit DAC chip which reduces chip count and provides high reliability. The AD390 is ideal for systems requiring digital control of many analog voltages where board space is at a premium. Such applications include automatic test equipment, process controllers, and vector-scan displays.

The AD390 is laser-trimmed to  $\pm 1/2$ LSB max nonlinearity (AD390KD, TD) and absolute accuracy of  $\pm 0.05$  percent of full scale. The high initial accuracy is made possible by the use of thin-film scaling resistors on the monolithic DAC chips. The internal buried Zener voltage reference provides excellent temperature drift characteristics (20ppm/°C) and an initial tolerance of  $\pm 0.03\%$  maximum. The internal reference buffer allows a single common reference to be used for multiple AD390 devices in large systems.

The individual DACs are accessed by the  $\overline{CS1}$  through  $\overline{CS4}$  control inputs and the  $\overline{A0}$  and  $\overline{A1}$  lines. These control signals permit the registers of the four DACs to be loaded sequentially and the outputs to be simultaneously updated.

The AD390 outputs are calibrated for a  $\pm 10V$  output range with positive-true offset binary input coding. A 0 to + 10V version is available on special order.

The AD390 is packaged in a 28-lead ceramic package and is specified for operation over the 0 to  $+70^{\circ}$ C and  $-55^{\circ}$ C to  $+125^{\circ}$ C temperature range.

\*Protected by patent numbers 3,803,590; 3,890,611; 3,932,863; 3,978,473; 4,020,486 and other patents pending.

# TUNCTIONAL BLOCK DIAGRAM V, DOING AGNO 12 BT LATCH DACI 13 BT LATCH DACI 14 BT LATCH DACI 15 BT LATCH DACI 17 BF IN DACI 18 BT LATCH DACI 19 Vouri

### PRODUCT HIGHLIGHTS

- The AD390 offers a dramatic reduction in printed circuit board space requirements in systems using multiple DACs.
- Each DAC is independently addressable, providing a versatile control architecture for simple interface to microprocessors.
   All latch enable signals are level-triggered.
- The output voltage is trimmed to a full scale accuracy of ±0.05%. Settling time to ±1/2LSB is 8 microseconds maximum.
- An internal 10 volt reference is available or an external reference can be used. With an external reference, the AD390 gain TC is ±5ppm/°C maximum.
- The proprietary smonolithic DAC chips provide excellent linearity and guaranteed monotonicity over the full operating temperature range.
- The 28-pin double-width hybrid package provides extremely high functional density. No external components or adjustments are required to provide the complete function.
- The AD390SD and AD390TD feature guaranteed accuracy and linearity over the -55°C to +125°C temperature range.

# AD390—SPECIFICATIONS $(T_A = +25^{\circ}C, V_S = \pm 15V)$ unless otherwise indicated, specifications guaranteed after 10 minute warmup)

Model	AD390JD/SD		AD390KD/TD				
	Min	Тур	Max	Min	Тур	Max	Units
DATA INPUTS (Pins 1-12 and 23-28) <sup>1</sup>							
TTL or 5 Volt CMOS							
Input Voltage	1						1
Bit ON (Logic "1")	+ 2.0		+5.5	+2.0		+ 5.5	V
Bit OFF (Logic "0")	i		+0.8			+0.8	V
Input Current (Pin 24 is 3 × Larger)							
Bit ON (Logic "1")	•	500	1200	}	500	1200	μΑ
Bit OFF (Logic "0")	i	150	400		150	409	μΛ
· •	<del>                                     </del>		12			12	Bits
RESOLUTION	<del> </del>			<del>                                     </del>		14	Dita
OUTPUT <sup>2</sup>						. 10	1,,
Voltage Range <sup>3</sup>	1 _		± 10	_ ا		± 10	V.
Current	5		_	5			mA.
Settling Time (to ± ½LSB)		4	8		4	8	μs
ACCURACY							ar crop4
Gain Error (w/ext. 10.000V reference)	ļ	$\pm 0.05$	±0.1		±0.025	±0.05	% of FSR <sup>4</sup>
Offset	1	$\pm 0.025$	$\pm 0.05$		$\pm 0.012$	±0.025	% of FSR
Linearity Error	1	± 1/4	± 3/4	1	± 1/8	± 1/2	LSB
Differential Linearity Error		$\pm 1/2$	± 3/4		± 1/4	± 1/2	LSB
TEMPERATURE DRIFT							
Gain (internal reference)			± 40	}		± 20	ppm/°C
(external reference)			± 10			±5	ppm/°C
Zero			± 10			± 5	ppm/°C
Linearity Error T <sub>min</sub> -T <sub>max</sub>	1	$\pm 1/2$	$\pm 3/4$		± 1/4	± 1/2	LSB
Differential Linearity MONO	TONICITY	GUARANT	EED OVER	FULL TEM	PERATURE	RANGE	
CROSSTALK <sup>5</sup>		0.1			0.1		LSB
				<u> </u>			
REFERENCE OUTPUT				1	10.000	10.000	1 47
	9.997	10.000	10.003	9.997	10.000	10.003	V
Voltage (without load)	9.997 2.5	10.000 3.5	10.003	9.997 2.5	3.5	10.003	mA
Current (available for external use)	1		10.003			10.003	II
Voltage (without load) Current (available for external use) REFERENCE INPUT	1	3.5	10.003		3.5		mA
Voltage (without load) Current (available for external use) REFERENCE INPUT Input Resistance	2.5			2.5			mA
Voltage (without load) Current (available for external use) REFERENCE INPUT Input Resistance Voltage Range	1	3.5	10.003		3.5	11	mA
Voltage (without load) Current (available for external use)  REFERENCE INPUT Input Resistance Voltage Range  POWER REQUIREMENTS	5	3.5 10 <sup>10</sup>	11	5	3.5 10 <sup>10</sup>	11	mA Ω V
Voltage (without load) Current (available for external use)  REFERENCE INPUT Input Resistance Voltage Range  POWER REQUIREMENTS Voltage <sup>6</sup>	2.5	3.5		2.5	3.5		mA
Voltage (without load) Current (available for external use)  REFERENCE INPUT Input Resistance Voltage Range  POWER REQUIREMENTS Voltage <sup>6</sup> Current	5	3.5 10 <sup>10</sup> ± 15	11 ± 16.5	5	3.5 10 <sup>10</sup> ± 15	11 ± 16.5	mA Ω V
Voltage (without load) Current (available for external use)  REFERENCE INPUT Input Resistance Voltage Range  POWER REQUIREMENTS Voltage <sup>6</sup> Current + V <sub>S</sub>	5	3.5 10 <sup>10</sup> ± 15 20	11 ±16.5	5	3.5 10 <sup>10</sup> ± 15 20	11 ± 16.5	mA Ω V V mA
Voltage (without load) Current (available for external use)  REFERENCE INPUT Input Resistance Voltage Range  POWER REQUIREMENTS Voltage <sup>6</sup> Current + V <sub>S</sub> - V <sub>S</sub>	2.5 5 ±13.5	3.5 10 <sup>10</sup> ± 15	11 ± 16.5	5	3.5 10 <sup>10</sup> ± 15	11 ± 16.5	mA Ω V
Voltage (without load) Current (available for external use)  REFERENCE INPUT Input Resistance Voltage Range  POWER REQUIREMENTS Voltage <sup>6</sup> Current + V <sub>S</sub> - V <sub>S</sub> POWER SUPPLY GAIN SENSITIVITY	2.5 5 ±13.5	3.5 10 <sup>10</sup> ± 15 20 - 85	11 ± 16.5 35 - 100	5	3.5 10 <sup>10</sup> ± 15 20 - 85	11 ± 16.5 35 - 100	mA Ω V V mA mA
Voltage (without load) Current (available for external use)  REFERENCE INPUT Input Resistance Voltage Range  POWER REQUIREMENTS Voltage <sup>6</sup> Current + V <sub>S</sub> - V <sub>S</sub> POWER SUPPLY GAIN SENSITIVITY + V <sub>S</sub>	2.5 5 ±13.5	3.5  10 <sup>10</sup> ± 15  20  - 85  0.002	11 ± 16.5 35 -100	5	3.5  10 <sup>10</sup> ± 15  20  - 85  0.002	11 ± 16.5 35 - 100	mA Ω V V mA mA %FS/%
Voltage (without load) Current (available for external use)  REFERENCE INPUT Input Resistance Voltage Range  POWER REQUIREMENTS Voltage <sup>6</sup> Current + V <sub>S</sub> - V <sub>S</sub> POWER SUPPLY GAIN SENSITIVITY	2.5 5 ±13.5	3.5 10 <sup>10</sup> ± 15 20 - 85	11 ± 16.5 35 - 100	5	3.5 10 <sup>10</sup> ± 15 20 - 85	11 ± 16.5 35 - 100	mA Ω V V mA mA
Voltage (without load) Current (available for external use)  REFERENCE INPUT Input Resistance Voltage Range  POWER REQUIREMENTS Voltage <sup>6</sup> Current + V <sub>S</sub> - V <sub>S</sub> POWER SUPPLY GAIN SENSITIVITY + V <sub>S</sub>	2.5 5 ±13.5	3.5  10 <sup>10</sup> ± 15  20  - 85  0.002	11 ± 16.5 35 -100	2.5 5 ±13.5	3.5  10 <sup>10</sup> ± 15  20  - 85  0.002	11 ± 16.5 35 - 100 0.006 0.006	mA Ω V V mA mA %FS/%
Voltage (without load) Current (available for external use)  REFERENCE INPUT Input Resistance Voltage Range  POWER REQUIREMENTS Voltage <sup>6</sup> Current + V <sub>S</sub> - V <sub>S</sub> POWER SUPPLY GAIN SENSITIVITY + V <sub>S</sub> - V <sub>S</sub>	2.5 5 ±13.5	3.5  10 <sup>10</sup> ± 15  20  - 85  0.002	11 ± 16.5 35 -100	5	3.5  10 <sup>10</sup> ± 15  20  - 85  0.002	11 ± 16.5 35 - 100	mA Ω V  V  mA mA %FS/% %FS/%
Voltage (without load) Current (available for external use)  REFERENCE INPUT Input Resistance Voltage Range  POWER REQUIREMENTS Voltage <sup>6</sup> Current + V <sub>S</sub> - V <sub>S</sub> POWER SUPPLY GAIN SENSITIVITY + V <sub>S</sub> - V <sub>S</sub> TEMPERATURE RANGE	2.5 5 ±13.5	3.5  10 <sup>10</sup> ± 15  20  - 85  0.002	11 ±16.5 35 -100 0.006 0.006	2.5 5 ±13.5	3.5  10 <sup>10</sup> ± 15  20  - 85  0.002	11 ± 16.5 35 - 100 0.006 0.006	mA Ω V V mA mA %FS/%

### NOTES

<sup>1</sup>Timing specifications appear in Table 2.

AD50207-1 J Grade AD50207-2 K Grade AD50207-3 S Grade AD50207-4 T Grade AD50207-7 S/883B Grade AD50207-8

T/883B Grade

<sup>&</sup>lt;sup>2</sup>The AD390 outputs are guaranteed stable for load capacitances up to 300pF.

<sup>3</sup> ± 10V range is standard. A 0 to 10V version is also available. To order, use the following part numbers:

<sup>&</sup>lt;sup>4</sup>FSR means Full Scale Range and is equal to 20V for a ± 10V range.

 $<sup>^{5}</sup>$ Crosstalk is defined as the change in any one output as a result of any other output being driven from -10V to +10V into a  $2k\Omega$  load.

The AD390 can be used with supply voltage as low as  $\pm 11.4$ V, Figure 10.

Specifications subject to change without notice.

	AD390
ABSOLUTE MAXIMUM RATINGS  + V <sub>S</sub> to DGND 0 to +18V  − V <sub>S</sub> to DGND 0 to −18V  Digital Inputs (Pins 1-12, 23-28) to DGND +7V  Ref In to DGND	Analog Outputs (Pins 16, 18-21)

### **ORDERING GUIDE**

Model	Temperature Range	Gain Error 25°C	Linearity Error T <sub>min</sub> - T <sub>max</sub>	Package Option*
AD390JD	0 to +70°C	±4LSB	± 3/4LSB	DH-28
AD390KD	0 to +70°C	±2LSB	± 1/2LSB	DH-28
AD390SD	-55°C to +125°C	±4LSB	± 3/4LSB	DH-28
AD390TD	-55°C to +125°C	±2LSB	± 1/2LSB	DH-28

<sup>\*</sup>DH-28 = Side Brazed Ceramic DIP for Hybrid. For outline information see Package Information section.

### PIN CONFIGURATION

