Complete, High Speed 16-Bit A/D Converters

AD1376/AD1377

FEATURES

Complete 16-Bit Converters with Reference and Clock
±0.003% Maximum Nonlinearity
No Missing Codes to 14 Bits over Temperature
Fast Conversion
17 μs to 16 Bits (AD1376)
10 μs to 16 Bits (AD1377)
Short Cycle Capability
Adjustable Clock Rate
Parallel and Serial Outputs
Low Power: 645 mW Typical (AD1376)
585 mW Typical (AD1377)
Industry Standard Pinout

PRODUCT DESCRIPTION

The AD1376/AD1377 are high resolution, 16-bit analog-to-digital converters with internal reference, clock and laser-trimmed thin-film applications resistors. They are packaged in a compact 32-pin, ceramic scam sealed (hermetic) dual-in-line packages (DIP). Thin-film scaling resistors provide bipolar input ranges of ±2.5 V, ±5 V, ±10 V and unipolar input ranges of 0 V to +5 V, 0 V to +10 V and 0 V to +20 V.

Digital output data is provided in parallel and serial form with corresponding *clock* and *status* outputs. All digital inputs and outputs are TTL compatible.

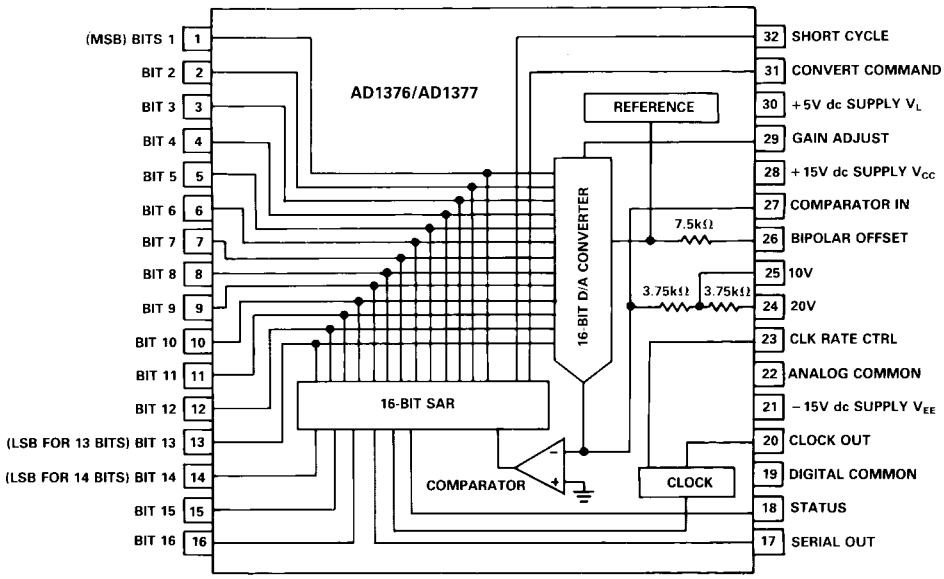
APPLICATIONS

The AD1376/AD1377 are excellent for use in high resolution applications requiring moderate speed and high accuracy or stability over commercial (0°C to +70°C) temperature ranges (for extended temperature ranges, the pin compatible AD1378 is recommended.) Typical applications include medical and analytic instrumentation, precision measurement for industrial robotics, automatic test equipment (ATE), and multichannel data acquisition systems, servo control systems or anywhere wide dynamic range is required A proprietary monolithic DAC and laser-trimmed thin-film resistors guarantee a maximum nonlinearity of ±0 003% (1/2 LSB_{14}.) The converters may be short cycled to achieve faster conversion times – 15 μs to 14 bits for the AD1376, or 8 μs to 14 bits for the AD1377.

PRODUCT HIGHLIGHTS

1. The AD1376/AD1377 provides 16-bit resolution with a maximum linearity error of ±0.003% (1/2 LSB_{14}) at +25°C.
2. AD1376 conversion time is 14 μs (typical) short cycled to 14 bits, and 16 μs to 16 bits.
3. AD1377 conversion time is 8 μs (typical) short cycled to 14 bits, and 9 μs to 16 bits.
4. Two binary codes are available on the digital output. They are CSB (Complementary Straight Binary) for unipolar input voltage ranges and COB (Complementary Offset Binary) for bipolar input ranges. Complementary Twos Complement (CTC) coding may be obtained by inverting Pin 1 (MSB).
5. The AD1376 and AD1377 include internal reference and clock, with external clock rate adjust pin, and serial and parallel digital outputs.

FUNCTIONAL BLOCK DIAGRAM



REV. B

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AD1376/AD1377–SPECIFICATIONS (typical at T_A = +25°C, V_S = ±15, +5 V unless otherwise noted)

Model	AD1376JD/AD1377JD	AD1376KD/AD1377KD	Units
RESOLUTION	16 (max)	16 (max)	Bits
ANALOG INPUTS			
Voltage Ranges			
Bipolar	±2.5, ±5, ±10	±2.5, ±5, ±10	Volts
Unipolar	0 to +5, 0 to +10, 0 to +20	0 to +5, 0 to +10, 0 to +20	Volts
Impedance (Direct Input)			
0 V to +5 V, ±2.5 V	1.88	1.88	kΩ
0 V to +10 V, ±5.0 V	3.75	3.75	kΩ
0 V to +20 V, ±10 V	7.50	7.50	kΩ
DIGITAL INPUTS[1]			
Convert command	Positive Pulse 50 ns Wide (min) Trailing Edge Initiates Conversion		
Logic Loading	1	1	LS TTL Load
TRANSFER CHARACTERISTICS[2]			
ACCURACY			
Gain Error	±0.05[3] (±0.2 max)	±0.05[3] (±0.2 max)	%
Offset Error			
Unipolar	±0.05[3] (±0.1 max)	±0.05[3] (±0.1 max)	% of FSR[4]
Bipolar	±0.05[3] (±0.2 max)	±0.05[3] (±0.2 max)	% of FSR
Linearity Error (max)	±0.006	±0.003	% of FSR
Inherent Quantization Error	±1/2	±1/2	LSB
Differential Linearity Error	±0.003	±0.003	% of FSR
POWER SUPPLY SENSITIVITY			
±15 V dc (±0.75 V)	0.0015	0.0015	% of FSR/% ΔV_S
+5 V dc (±0.25 V)	0.001	0.001	% of FSR/% ΔV_S
CONVERSION TIME[5]			
12 Bits (AD1376)	11.5 (13 max)	11.5 (13 max)	µs
14 Bits (AD1376)	13.5 (15 max)	13.5 (15 max)	µs
16 Bits (AD1376)	15.5 (17 max)	15.5 (17 max)	µs
14 Bits (AD1377)	8.75 max	8.75 max	µs
16 Bits (AD1377)	10 max	10 max	µs
POWER SUPPLY REQUIREMENTS			
Rated Voltage, Analog	±15, ±0.5 (max)	±15, ±0.5 (max)	V dc
Rated Voltage, Digital	+5, ±0.25 (max)	+5, ±0.25 (max)	V dc
AD1376 Power Consumption	645 (850 max)	645 (850 max)	mW
+15 V Supply Drain	+16	+16	mA
–15 V Supply Drain	–21	–21	mA
+5 V Supply Drain	+18	+18	mA
AD1377 Power Consumption	600 (800 max)	600 (800 max)	mW
+15 V Supply Drain	+10	+10	mA
–15 V Supply Drain	–23	–23	mA
+5 V Supply Drain	+18	+18	mA
WARM-UP TIME	1	1	minutes
DRIFT[6]			
Gain	±15 (max)	±5 (±15 max)	ppm/°C
Offset			
Unipolar	±2 (±4 max)	±2 (±4 max)	ppm of FSR/°C
Bipolar	±10 (max)	±3 (±10 max)	ppm of FSR/°C
Linearity	±2 (±3 max)	±0.3 (±2 max)	ppm of FSR/°C
Guaranteed No Missing Code			
Temperature Range	0 to 70 (13 Bits)	0 to 70 (14 Bits)	°C
DIGITAL OUTPUT[1]			
(All Codes Complementary)			
Parallel & Serial			
Output Codes[7]			
Unipolar	CSB	CSB	
Bipolar	COB, CTC[8]	COB, CTC[8]	
Output Drive	5	5	LSTTL Loads

Model	AD1376JD/AD1377JD	AD1376KD/AD1377KD	Units
Status		Logic "1" During Conversion	
Status Output Drive	5 (max)	5 (max)	LSTTL Loads
Internal Clock[9]			
Clock Output Drive	5 (max)	5 (max)	LSTTL Loads
Frequency	1040/1750	1040/1750	kHz
TEMPERATURE RANGE			
Specification	0 to –70	0 to –70	°C
Operating	–25 to +85	–25 to +85	°C
Storage	–55 to +125	–55 to +125	°C

NOTES
[1]Logic "0" = 0.8 V, max. Logic "1" = 2.0 V, min for inputs. For digital outputs Logic "0" = +0.4 V max. Logic "1" = 2.4 V min.
[2]Tested on ±10 V and 0 V to +10 V ranges.
[3]Adjustable to zero.
[4]Full-Scale Range.
[5]Guaranteed but not 100% production tested.
[6]Conversion time may be shortened with "Short Cycle" set for lower resolution.
[7]CSB–Complementary Straight Binary. COB–Complementary Offset Binary. CTC–Complementary Twos Complement.
[8]CTC coding obtained by inverting MSB (Pin 1).
[9]With Pin 23, clock rate controls tied to digital ground.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . ±18 V
Logic Supply Voltage . . . . . +7 V
Analog Inputs (Pins 24 and 25) . . . . . ±25 V
Analog Ground-to-Digital Ground . . . . . ±0.3 V
Digital Inputs . . . . . –0.3 V to V_{DD} + 0.3 V
Junction Temperature . . . . . +175°C
Storage . . . . . +15°C
Lead Temperature (10 seconds) . . . . . +300°C

*Absolute maximum ratings are limiting values to be applied individually, and beyond which the service ability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Maximum Linearity Error	Conversion Time (16 Bits)	Package Option*
AD1376JD	0°C to +70°C	±0.006%	17 µs	DH-32E
AD1376KD	0°C to +70°C	±0.003%	17 µs	DH-32E
AD1377JD	0°C to -70°C	±0.006%	10 µs	DH-32E
AD1377KD	0°C to +70°C	±0.003%	10 µs	DH-32E

*DH-32E = Ceramic DIP.

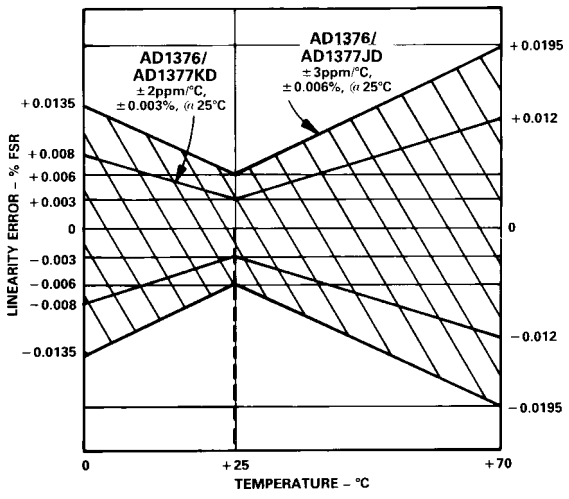


Figure 1. Linearity Error vs. Temperature

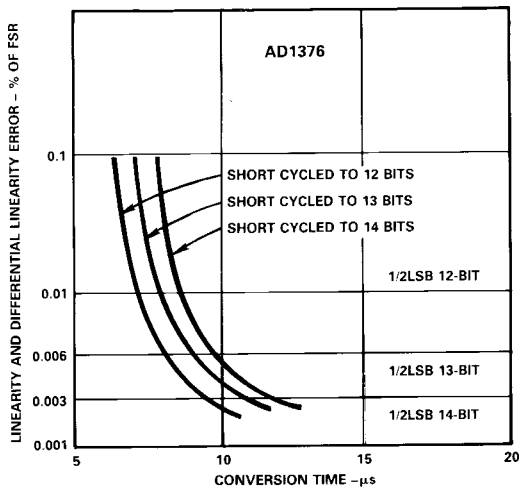


Figure 2. AD1376 Nonlinearity vs. Conversion Time

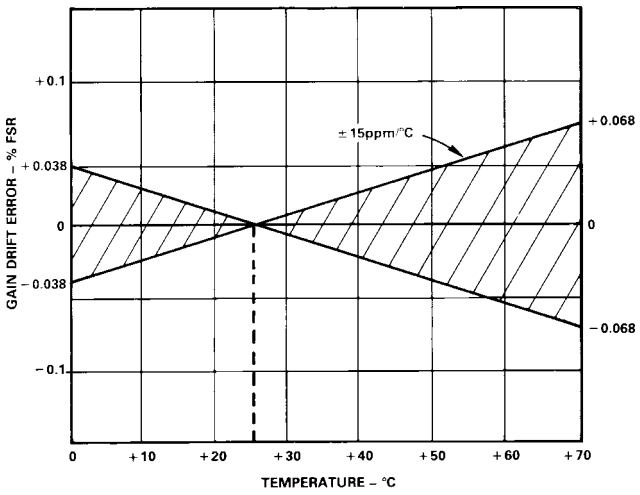


Figure 3. Gain Drift Error vs. Temperature

DESCRIPTION OF OPERATION

On receipt of a CONVERT START command, the AD1376/AD1377 converts the voltage at its analog input into an equivalent 16-bit binary number. This conversion is accomplished as follows: the 16-bit successive-approximation register (SAR) has its 16-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one hit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

GAIN ADJUSTMENT

The gain adjust circuit consists of a 100 ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 300 kΩ resistor to the gain adjust Pin 29 as shown in Figure 4.

If no external trim adjustment is desired, Pin 27 (offset adj) and Pin 29 (gain adj) may be left open.

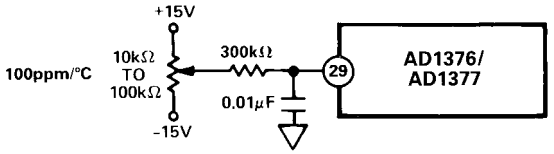


Figure 4. Gain Adjustment Circuit (±0.2% FSR)

OFFSET ADJUSTMENT

The zero adjust circuit consists of a 100 ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 1.8 MΩ resistor to Comparator Input Pin 27 for all ranges. As shown in Figure 5, the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a –1200 ppm/°C tempco contributes a worst-case offset tempco of 32 LSB_{14} × 61 ppm/LSB_{14} × 1200 ppm/°C = 2.3 ppm/°C of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±16 LSB_{14}, use of a carbon composition offset summing resistor typically contributes no more than 1 ppm/°C of FSR offset tempco.

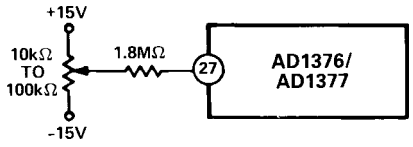


Figure 5. Offset Adjustment Circuit (±0.3% FSR)

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100 ppm/°C) are used, is shown in Figure 6.

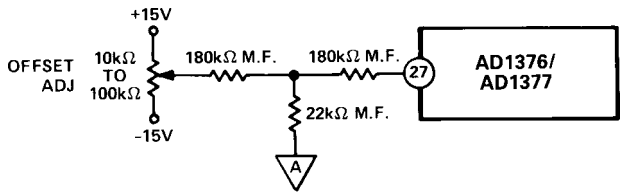


Figure 6. Low Tempco Zero Adjustment Circuit

In either adjust circuit, the fixed resistor connected to Pin 27 should be located close to this pin to keep the pin connection runs short. Comparator Input Pin 27 is quite sensitive to external noise pick-up and should be guarded by analog common.

TIMING

The timing diagram is shown in Figure 7. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 17 cycles. All the SAR parallel bits, STATUS flip-flops, and the gated clock inhibit signal are initialized on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and B_2–B_{16} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is reset unconditionally. This sequence continues until the Bit 16 (LSB) decision (keep) is made at t_{16}. The STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the low Logic "0" state. Note that the clock remains low until the next conversion.

Corresponding parallel data bits become valid on the same positive-going clock edge.

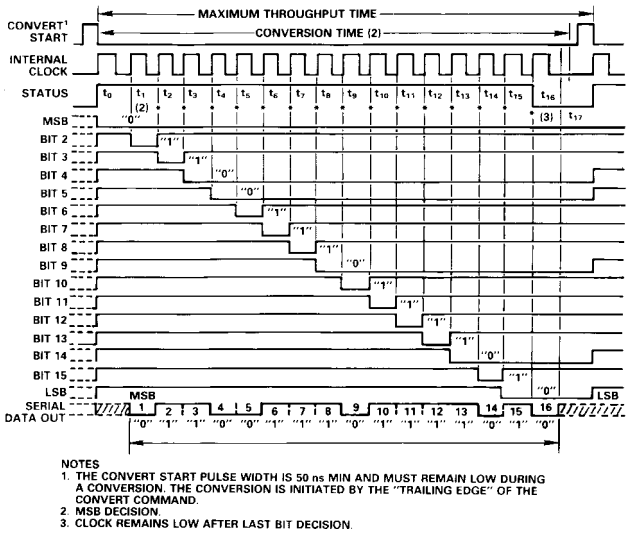


Figure 7. Timing Diagram (Binary Code 0110011101111010)

DIGITAL OUTPUT DATA

Both parallel and serial data from TTL storage registers is in negative true form (Logic "1" = 0 V and Logic "0" = 2.4 V). Parallel data output coding is complementary binary for unipolar ranges and complementary offset binary for bipolar ranges. Parallel data becomes valid at least 20 ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag (see Figure 8).

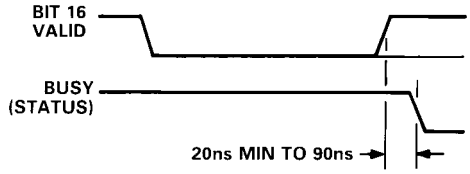


Figure 8. LSB Valid to Status Low

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (1M4SB first, LSB last) in NRZ (nonreturn-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 120 ns after the rising clock edges, permitting serial data to he clocked directly into a receiving register on the negative-going clock edges as shown in Figure 9. There are 17 negative-going clock edges in the complete 16-bit conversion cycle. The first negative edge shifts an invalid bit into the register, which is shifted out on the last negative-going clock edge.

All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

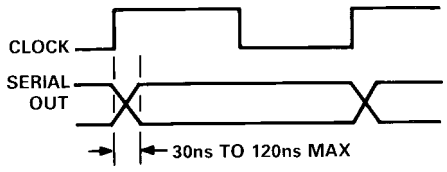


Figure 9. Clock High to Serial Out Valid

Short Cycle Input

A Short Cycle Input, Pin 32, permits the timing cycle shown in Figure 7 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 16-bit resolution. When 10-bit resolution is desired, Pin 32 is connected to Bit 11 output Pin 11. The conversion cycle then terminates and the STATUS flag resets after the Bit 10 decision (timing diagram of Figure 7). Short cycle connections and associated 8-, 10-, 12-, 13-, 14- and 15-bit conversion times are summarized in Table I, for a 1.6 MHz clock (AD1377) or 933 kHz (AD1376).

INPUT SCALING

The ADC (ADC) inputs should he scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 10 for circuit details.

Table II. Input Scaling Connections

Input Signal Line	Output Code	Connect Pin 26 to Pin	Connect Pin 24 to	Connect Input Signal to
±10 V	COB	27	Input Signal	24
±5 V	COB	27	Open	25
±2.5 V	COB	27	Pin 27	25
0 V to +5 V	CSB	22	Pin 27	25
0 V to +10 V	CSB	22	Open	25
0 V to +20 V	CSB	22	Input Signal	24

Note
Pin 27 is extremely sensitive to noise and should be guarded by Analog Common.

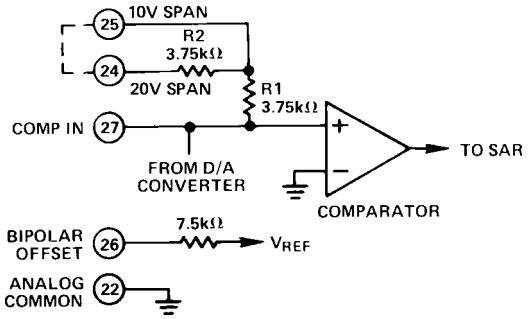


Figure 10. Input Scaling Circuit

Table I. Short Cycle Connections

Resolution Bits	Resolution (% FSR)	Maximum Conversion Time–µs (AD1377)	Maximum Conversion Time–µs (AD1378)	Status Flag Reset	Connect Short Cycle Pin 32 to Pin:
16	0.0015	10	17.1	t_{16}	NC (Open)
15	0.003	9.4	16.1	t_{15}	16
14	0.006	8.7	15.0	t_{14}	15
13	0.012	8.1	13.9	t_{13}	14
12	0.024	7.5	12.9	t_{12}	13
10	0.100	6.3	10.7	t_{10}	11
8	0.390	5.0	8.6	t_{8}	9

Table III. Transition Values vs. Calibration Codes

Code Under Test MSB	LSB	Range	Low Side Transition Values ±10 V	±5 V	±2.5 V	0 V to +10 V	0 V to +5 V
000	000*	+Full Scale	+10 V –3/2 LSB	+5 V –3/2 LSB	+2.5 V –3/2 LSB	+10 V –3/2 LSB	+5 V –3/2 LSB
011.....	111	Mid Scale	0–1/2 LSB	0–1/2 LSB	0–1/2 LSB	+5 V–1/2 LSB	+2.5 V–1/2 LSB
111.....	110	–Full Scale	–10 V +1/2 LSB	–5 V +1/2 LSB	–2.5 V +1/2 LSB	0 V +1/2 LSB	0 V +1/2 LSB

*Voltages given are the nominal value for Transition to the code specified.
Note: For LSB value for range and resolution used, see Table IV.

Table IV. Input Voltage Range and LSB Values

Analog Input Voltage Range	±10 V	±5 V	±2.5 V	0 V to +10 V	0 V to +5 V	
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20\ V}{2^n}$	$\frac{10\ V}{2^n}$	$\frac{5\ V}{2^n}$	$\frac{10\ V}{2^n}$	$\frac{5\ V}{2^n}$
	n = 8	78.13 mV	39.06 mV	19.53 mV	39.06 mV	19.53 mV
	n = 10	19.53 mV	9.77 mV	4.88 mV	9.77 mV	4.88 mV
	n = 12	4.88 mV	2.44 mV	1.22 mV	2.44 mV	1.22 mV
	n = 13	2.44 mV	1.22 mV	0.61 mV	1.22 mV	0.61 mV
	n = 14	1.22 mV	0.61 mV	0.31 mV	0.61 mV	0.31 mV
	n = 15	0.61 mV	0.31 mV	0.15 mV	0.31 mV	0.15 mV

NOTES
*COB = Complementary Offset Binary.
**CTC = Complementary Twos Complementary—achieved by using an inverter to complement the most significant bit to product ($\overline{MSB}$).
***CSB = Complementary Straight Binary.

CALIBRATION
(14-Bit Resolution Examples)

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 4 and 5, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and –FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 V to + 10 V Range

Set analog input to +1 LSB_{14} = 0.00061 V. Adjust Zero for digital output = 11111111111110.

Zero is now calibrated. Set analog input to +FSR – 2 LSB = +9.99878 V. Adjust Gain for 00000000000001 digital output code; full scale (Gain) is now calibrated. Half scale calibration check: set analog input to +5.00000 V; digital output code should be 01111111111111.

–10 V to + 10 V Range

Set analog input to 9.99878 V; adjust zero for 1111111111110 digital output (complementary offset binary) code. Set analog input to 9.99756 V; adjust Gain for 00000000000001 digital output (complementary offset binary) code. Half scale calibration check set analog input to 0.00000 V; digital output (complementary offset binary) code should be 01111111111111.

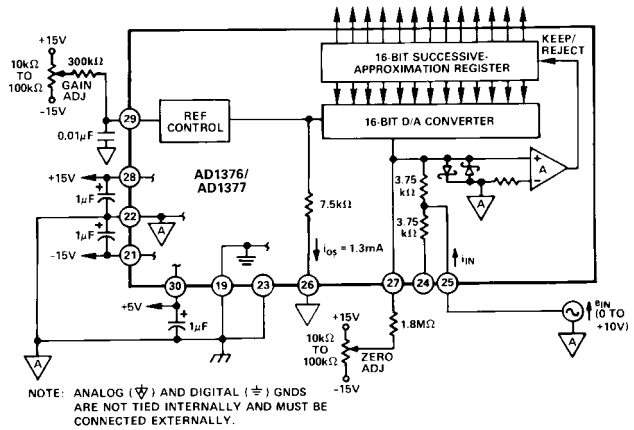


Figure 11. Analog and Power Connections for Unipolar 0 V to +10 V Input Range

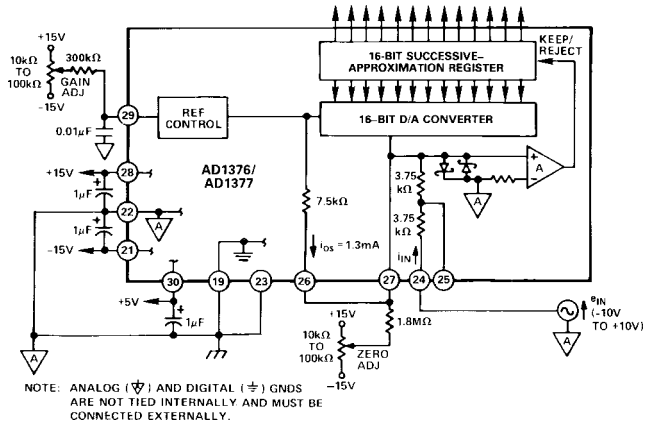


Figure 12. Analog and Power Connections for Bipolar +10 V to +10 V Input Range

Other Ranges

Representative digital coding for 0 V to +10 V and –10 V to +10 V ranges is given above. Coding relationships and calibration points for 0 V to +5 V, –2.5 V to +2.5 V and –5 V to +5 V ranges can be found by halving proportionally the corresponding code equivalents listed for the 0 V to +10 V and –10 V to +10 V ranges, respectively, as indicated in Table III.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/2 LSB using the static adjustment procedure described above. By summing a small sine or triangular wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in *Analog-Digital Conversion Handbook*, edited by D. H. Sheingold, Prentice Hall, Inc., 1986.

GROUNDING, DECOUPLING AND LAYOUT CONSIDERATIONS

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return) and Analog Signal Ground. These grounds (Pins 19 and 22) must be tied together at one point for the ADC as close as possible to the converter. Ideally, a single solid analog ground plane under the converter would be desirable. Current flows through the wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system analog ground point and the ground pins of the ADC. Separate wide conductor stripe ground returns should be provided for high resolution converters to minimize noise and IR losses from the current flow in the path from the converter to the system ground point. In this way ADC supply currents and other digital logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the ADC supply terminals should be capacitively decoupled as close to the ADC as possible. A large value capacitor such as 1 μF in parallel with a 0.1 μF capacitor is usually sufficient. Analog supplies are to be bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.

The metal cover is internally grounded with respect to the power supplies, grounds and electrical signals. Do not externally ground the cover.

CLOCK RATE CONTROL

The AD1376/AD1377 may be operated at faster conversion times by connecting the Clock Rate Control (Pin 23) to an external multiturn trim potentiometer (TCR <100 ppm/°C) as shown in Figure 13.

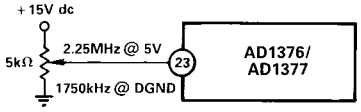


Figure 13. Clock Rate Control Circuit

HIGH RESOLUTION DATA ACQUISITION SYSTEM

The essential details of a high resolution data acquisition system using the AD386 and AD1376 or AD1377 are shown in Figure 14. Conversion is initiated by the falling edge of the CONVERT START pulse. This edge drives the AD1376's or AD1377's STATUS line high. The inverter then drives the AD386 into hold mode. STATUS remains high throughout the conversion and returns low once the conversion is completed. This allows the AD386 to reenter track mode.

This circuit can exhibit nonlinearities arising from transients produced at the A/D's input by the falling edge of CONVERT START. This edge resets the A/D's internal DAC; the resulting transient depends on the SHA's present output voltage and the A/D's prior conversion result. In the circuit of Figure 14 the falling edge of CONVERT START also places the SHA into hold mode (via the A/D's STATUS output), causing the reset transient to occur at the same moment as the SHA's track-and-hold transition. Timing skews and capacitive coupling can cause some of the transient signal to add to the signal being acquired by the SHA, introducing nonlinearity.

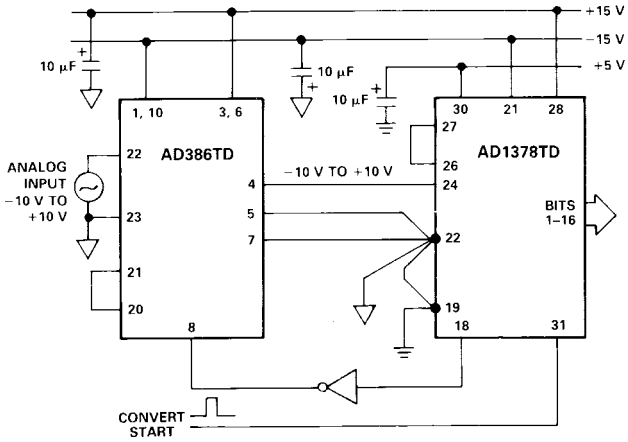


Figure 14. Basic Data Acquisition System Interconnections

A much safer approach is to add a flip flop as shown in Figure 15. The rising edge of CONVERT START places the T/H into hold mode before the A/D reset transients begin. The falling

edge of STATUS places the AD386 back into track mode. System throughput will be reduced if a long CONVERT START pulse is used. Throughput can be calculated from

$$Throughput = \frac{1}{T_{ACQ} + T_{CONV} + T_{CS}}$$

where T_{ACQ} is the T/H acquisition time, T_{CONV} is the time required for the A/D conversion, and T_{CS} is the duration of CONVERT START. The combination of the AD1376 and AD386 will provide greater than 50 kHz throughput. No significant T/H droop error will be introduced provided the width of CONVERT START is small compared with the A/D's conversion time.

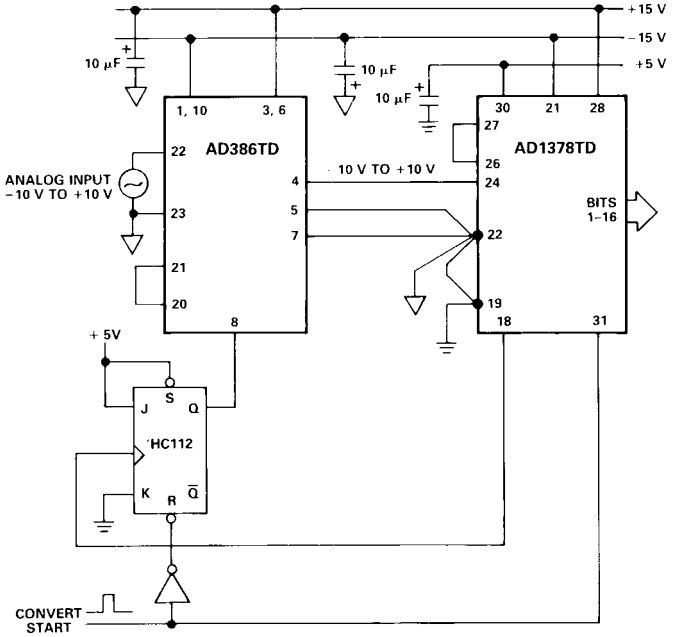


Figure 15. Improved Data Acquisition System

Using the AD1376 or AD1377 at Slower Conversion Times

The user may wish to run the ADC at slower conversion times in order to synchronize the A/D with an external clock. This is accomplished by running a slower clock than the internal clock into the START CONVERT input. This clock must consist of narrow negative-going clock pulses, as seen in Figure 16. The pulse must be a minimum of 100 ns wide but not greater than 700 ns. Having a rising edge immediately after a falling edge inhibits the internal clock pulse. This enables the ADC to function normally and complete a conversion after 17 clock pulses.

The STATUS command will function normally and switch high after the first clock pulse and will fall low after the 17th clock pulse. In this way an external clock can be used to control the ADC at slower conversion times.

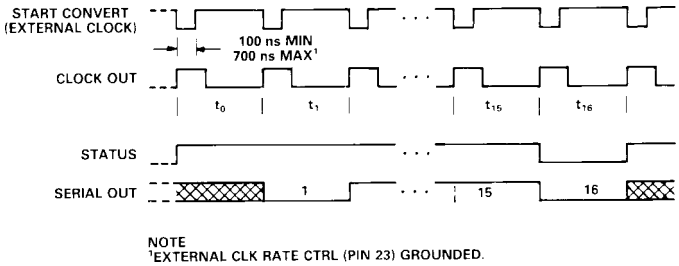
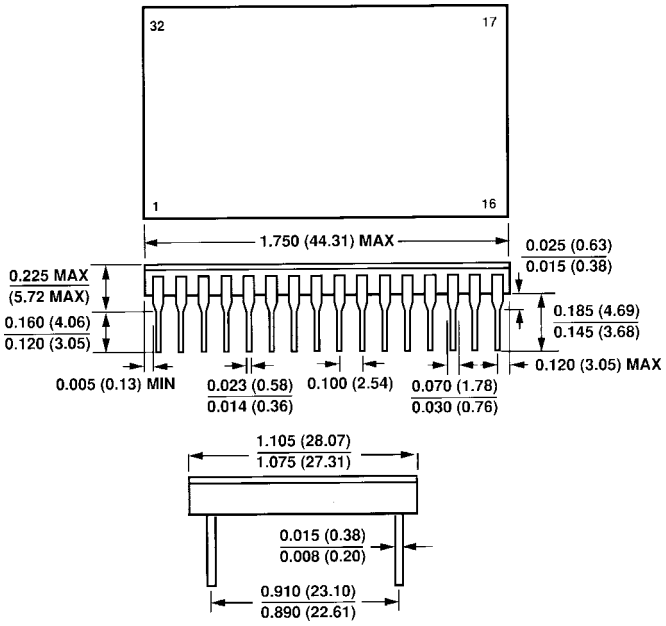


Figure 16. Timing Diagram for Use with an External Clock

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

32-Pin Ceramic DIP
(DH-32E)



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