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8XL51FA/FB/FC
LOW VOLTAGE
CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLERS
Commercial/Express

87L51FA/83L51FA/80L51FA/87L51FB/83L51FB/87L51FC/83L51FC

■ High Performance CHMOS OTP ROM/ ROM/CPU

■ Low Voltage Operation

■ 20 MHz Commercial/16 MHz Express Operation

■ Three 16-Bit Timer/Counters

■ Programmable Counter Array with:
— High Speed Output,
— Compare/Capture,
— Pulse Width Modulator,
— Watchdog Timer Capabilities

■ Up/Down Timer/Counter

■ Three Level Program Lock System

■ 8K/16K/32K On-Chip Program Memory

■ 256 Bytes of On-Chip Data RAM

■ Improved Quick Pulse Programming Algorithm

■ Boolean Processor

■ 32 Programmable I/O Lines

■ 7 Interrupt Sources

■ Four Level Interrupt Priority

■ Programmable Serial Channel with:
— Framing Error Detection
— Automatic Address Recognition

■ 64K External Program Memory Space

■ 64K External Data Memory Space

■ MCS® 51 Microcontroller Compatible Instruction Set

■ Power Saving Idle and Power Down Modes

■ ONCE (On-Circuit Emulation) Mode

■ Extended Temperature Range ($-40°C$ to $+85°C$)

MEMORY ORGANIZATION

ROM Device	OTP ROM Version	ROMLESS Version	ROM/ OTP ROM Bytes	RAM Bytes
83L51FA	87L51FA	80L51FA	8K	256
83L51FB	87L51FB	80L51FA	16K	256
83L51FC	87L51FC	80L51FA	32K	256

These devices can address up to 64 Kbytes of external program/data memory.

The Intel 8XL51FA/8XL51FB/8XL51FC is a single-chip control oriented microcontroller which is fabricated on Intel's reliable CHMOS III-E technology. Being a member of the MCS® 51 microcontroller family, the 8XL51FA/8XL51FB/8XL51FC uses the same powerful instruction set, has the same architecture, and is pin-for-pin compatible with the existing MCS 51 microcontroller products.

The 8XL51FX is a 3V version of current 8XC51FX and will operate from 2.7V to 3.6V at a frequency range of 3.5 MHz to 16 MHz (Express)/20 MHz (Commercial).

For the remainder of this document, the 8XL51FA, 8XL51FB, 8XL51FC will be referred to as the 8XL51FX, unless information applies to a specific device.

November 1994   **Order Number: 272356-003**

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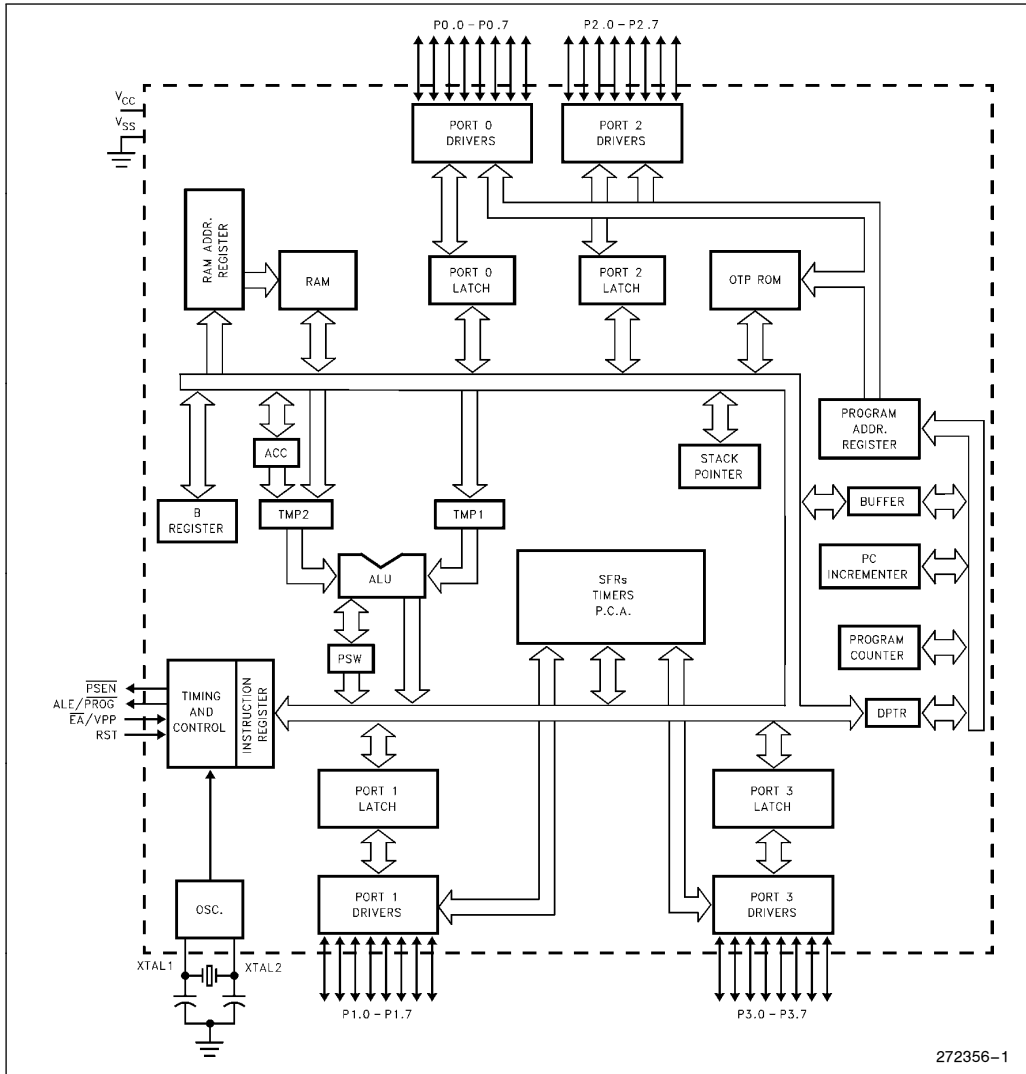|	Standard	−1	−20*
80L51FA	X	X	X
83L51FA	X	X	X
87L51FA	X	X	X
83L51FB	X	X	X
87L51FB	X	X	X
83L51FC	X	X	X
87L51FC	X	X	X

NOTE:
Standard   3.5 MHz to 12 MHz; 2.7V to 3.6V
−1   3.5 MHz to 16 MHz; 2.7V to 3.6V
−20*   3.5 MHz to 20 MHz; 2.7V to 3.6V
*Only available for commercial standard temperature range, not available at express temperature range.

Figure 1. 8XL51FX Block Diagram

ADVANCE INFORMATION

PROCESS INFORMATION

The 8XL51FA/8XL51FB/8XL51FC is manufactured on P629.5, a CHMOS III-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order Number 210997.

PACKAGES

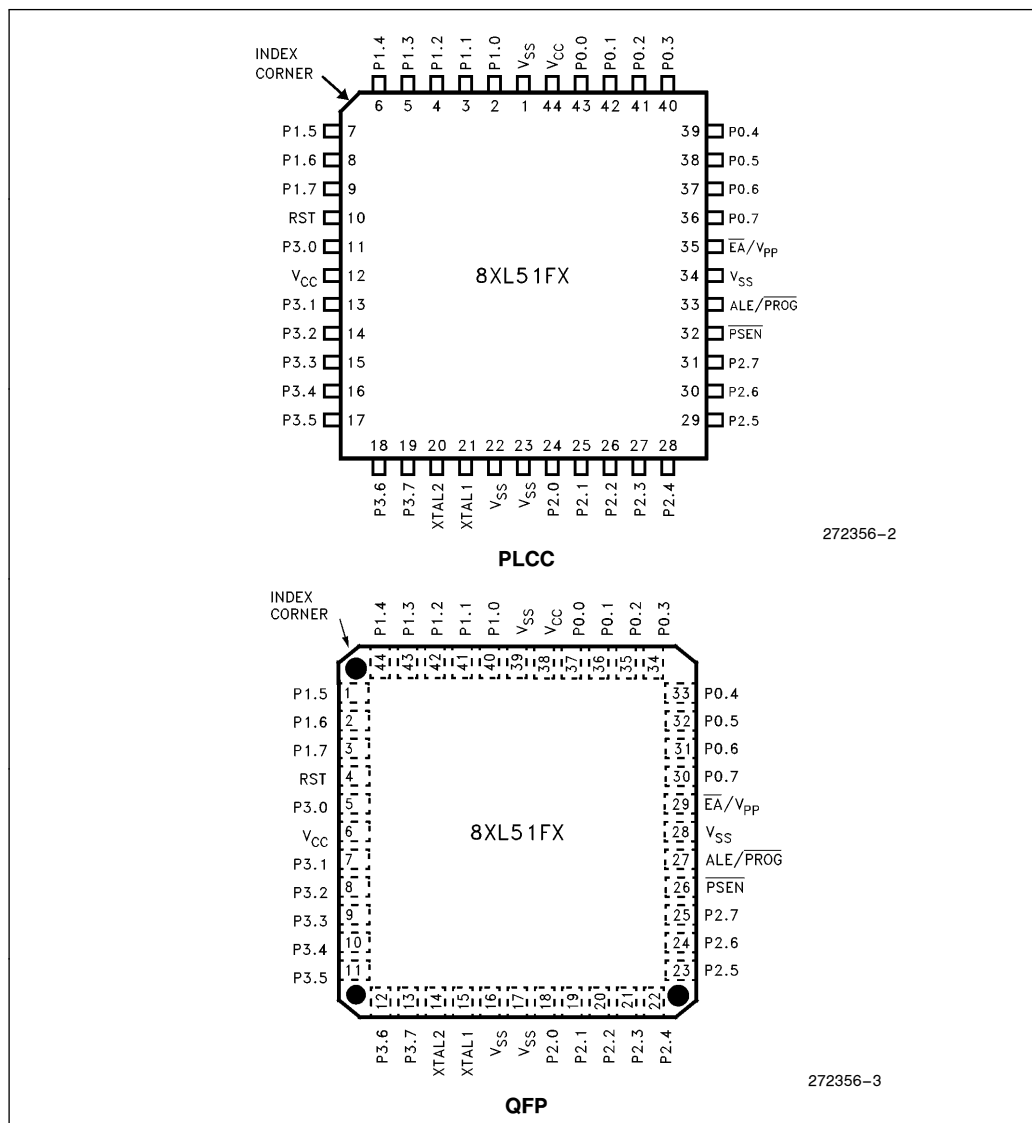| Part	Prefix	Package Type
8XL51FX	N	44-Pin PLCC (OTP)
	S	44-Pin QFP (OTP)

Figure 2. Pin Connections

PIN DESCRIPTIONS

V_{CC}: Supply voltage.

V_{SS}: Circuit ground.

Port 0: Port 0 is an 8-bit, open drain, bidirectional I/O port. As an output port each pin can sink several inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's, and can source and sink several inputs.

Port 0 also receives the code bytes during OTP ROM programming, and outputs the code bytes during program verification. External pullup resistors are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can drive several inputs. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pull-ups.

In addition, Port 1 serves the functions of the following special features of the 8XL51FX:

Port Pin	Alternate Function
P1.0	T2 (External Count Input to Timer/Counter 2), Clock Out
P1.1	T2EX (Timer/Counter 2 Capture/Reload Trigger and Direction Control)
P1.2	ECI (External Count Input to the PCA)
P1.3	CEX0 (External I/O for Compare/Capture Module 0)
P1.4	CEX1 (External I/O for Compare/Capture Module 1)
P1.5	CEX2 (External I/O for Compare/Capture Module 2)
P1.6	CEX3 (External I/O for Compare/Capture Module 3)
P1.7	CEX4 (External I/O for Compare/Capture Module 4)

Port 1 receives the low-order address bytes during OTP ROM programming and verifying.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can drive several inputs. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Some Port 2 pins receive the high-order address bits during OTP ROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can drive several inputs. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the MCS 51 microcontroller family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a minimum V_{IH2} voltage is applied whether the oscillator is running or not. An internal pull-down resistor permits a power-on reset with only a capacitor connected to V_{CC}.

ADVANCE INFORMATION

ALE: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin (ALE/$\overline{PROG}$) is also the program pulse input during OTP ROM programming for the 87L51FX.

In normal operation ALE is emitted at a constant rate of $\frac{1}{6}$ the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With this bit set, the pin is weakly pulled high. However, the ALE disable feature will be suspended during a MOVX or MOVC instruction, idle mode, power down mode and ICE mode. The ALE disable feature will be terminated by reset. When the ALE disable feature is suspended or terminated, the ALE pin will no longer be pulled up weakly. Setting the ALE-disable bit has no affect if the microcontroller is in external execution mode.

Throughout the remainder of this data sheet, ALE will refer to the signal coming out of the ALE/$\overline{PROG}$ pin, and the pin will be referred to as the ALE/$\overline{PROG}$ pin.

$\overline{PSEN}$: Program Store Enable is the read strobe to external Program Memory.

When the 8XL51FX is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory.

$\overline{EA}$/V_{PP}: External Access enable. $\overline{EA}$ must be strapped to VSS in order to enable the device to fetch code from external Program Memory locations 0000H to 0FFFH. Note, however, that if either of the Program Lock bits are programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ must be strapped to V_{CC} for internal program executions.

This pin also receives the programming supply voltage (V_{PP}) during OTP ROM programming.

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of a inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator

may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers."

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 floats, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.
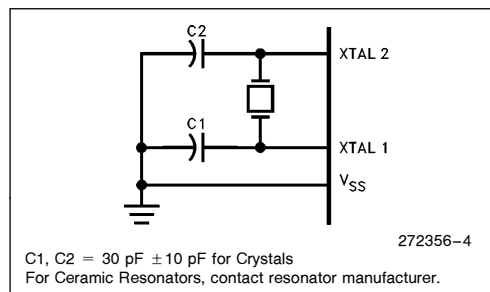

C1, C2 = 30 pF ± 10 pF for Crystals
For Ceramic Resonators, contact resonator manufacturer.

272356–4

Figure 3. Oscillator Connections

272356–5
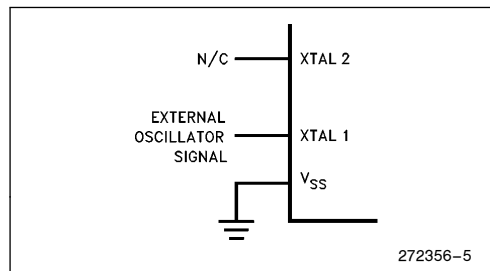
Figure 4. External Clock Drive Configuration

IDLE MODE

The user's software can invoke the Idle Mode. When the microcontroller is in this mode, power consumption is reduced. The Special Function Registers and the onboard RAM retain their values during Idle, but the processor stops executing instructions. Idle Mode will be exited if the chip is reset or if an enabled interrupt occurs. The PCA timer/counter can optionally be left running or paused during Idle Mode.

POWER DOWN MODE

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 8XL51FX either hardware reset or external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

To properly terminate Power Down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 or INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

DESIGN CONSIDERATION

- The 8XL51FX will operate from 2.7V to 3.6V with a frequency range of 3.5 MHz to 16 MHz (Express)/20 MHz (Commercial). Operating beyond these specifications could cause improper device functionality.

- All V_{CC} and V_{SS} pins must be connected. Please refer to Figure 2, Pin Connections, for the specific pins.

- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE MODE

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 8XL51FX without the 8XL51FX having to be removed from the circuit. The ONCE Mode is invoked by:

1) Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;

2) Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins float, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 8XL51FX is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Table 1. Status of the External Pins during Idle and Power Down

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Microcontrollers and Processors Handbook Volume I, #270646, and Application Note AP-252 (Embedded Applications Handbook), #270648, "Designing with the 80C51BH."

ADVANCE INFORMATION

8XL51FX EXPRESS

The Intel EXPRESS system offers enhancements to the operational specifications of the MCS-51 family of microcontrollers. These EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The EXPRESS program includes the commercial standard temperature range with burn-in and an extended temperature range with or without burn-in.

With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to 70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

Package types and EXPRESS versions are identified by a one- or two-letter prefix to the part number. The prefixes are listed in Table 2.

For the extended temperature range option, this data sheet specifies the parameters which deviate from their commercial temperature range limits.

Table 2. Prefix Identification

Prefix	Package Type	Temperature Range
N	PLCC	Commercial
S	QFP	Commercial
TN	PLCC	Extended
TS	QFP	Extended

NOTE:
Contact your distributor or local sales office to match the EXPRESS prefix with the proper device.

EXAMPLES:
N87L51FC indicates 87L51FC in a PLCC package and specified for commercial temperature range, without burn-in.

TN87L51FC indicates 87L51FC in a PLCC package and specified for extended temperature range with burn-in.

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ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . $-40°C$ to $+85°C$

Storage Temperature . . . . $-65°C$ to $+150°C$

Voltage on EA/V_{PP} Pin to V_{SS} . . . . . . .0V to $+13.0V$

Voltage on Any Other Pin to V_{SS} . . $-0.5V$ to $+6.5V$

I_{OL} per I/O Pin . . . . .15 mA

Power Dissipation. 1.5W
   (based on PACKAGE heat transfer limitations, not
   device power consumption)

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias Commercial Express	 0 -40	 $+70$ $+85$	 °C °C
V_{CC}	Supply Voltage	2.7	3.6	V

DC CHARACTERISTICS (Over Operating Conditions)

All parameter values apply to all devices unless otherwise indicated.

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (except XTAL1, RST)	-0.5	0.8	V	
V_{IL1}	Input Low Voltage (XTAL1, RST)	-0.5	$0.2 V_{CC} - 0.1$	V	
V_{IH}	Input High Voltage (Except XTAL1, RST, $\overline{EA}$)	2.0	$V_{CC} + 0.5$	V	
V_{IH1}	Input High Voltage ($\overline{EA}$)	$V_{CC} - 1.0$	$V_{CC} + 0.5$	V	
V_{IH2}	Input High Voltage (XTAL1, RST)	$0.7 V_{CC}$	$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage (Note 4) (Ports 1, 2 and 3)		0.4	V	$I_{OL} = 1.6$ mA (Note 1)
V_{OL1}	Output Low Voltage (Note 4) (Port 0, ALE/$\overline{PSEN}$)		0.4	V	$I_{OL} = 3.2$ mA (Note 1)
V_{OH}	Output High Voltage (Ports 1, 2 and 3, ALE, $\overline{PSEN}$	$V_{CC} - 0.7$		V	$I_{OH} = -30 \mu A$ (Note 2)
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	2.4		V	$I_{OH} = -1.0$ mA (Note 2)
I_{IL}	Logical 0 Input Current (Ports 1, 2 and 3)		-50	μA	$V_{IN} = 0.4V$
I_{LI}	Input Leakage Current (Port 0)		± 10	μA	$0 < V_{IN} < V_{CC}$

ADVANCE INFORMATION

DC CHARACTERISTICS (Over Operating Conditions)

All parameter values apply to all devices unless otherwise indicated. (Continued)

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)		-350	μA	$V_{IN} = 1.4V$
RRST	RST Pulldown Resistor	40	225	$K\Omega$	
I_{CC}	Power Supply Current Active Mode at 16 MHz Idle Mode at 16 MHz Power-Down Mode		25 8 30	mA mA μA	(Note 3)

NOTES:
1. Capacitive loading on Ports 0 and 2 may cause noise pulses above 0.4V to be superimposed on the V_{OL}s of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitance loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger, or CMOS-level input logic.
2. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
3. See Figures 6–9 for test conditions. Minimum V_{CC} for power down is 2V.
4. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin:　　　　　 10 mA
   Maximum I_{OL} per 8-bit port -
   　　　　　　　　Port 0:　　26 mA
   　　　　Ports 1, 2, and 3:　　15 mA
   Maximum total I_{OL} for all output pins:　　71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
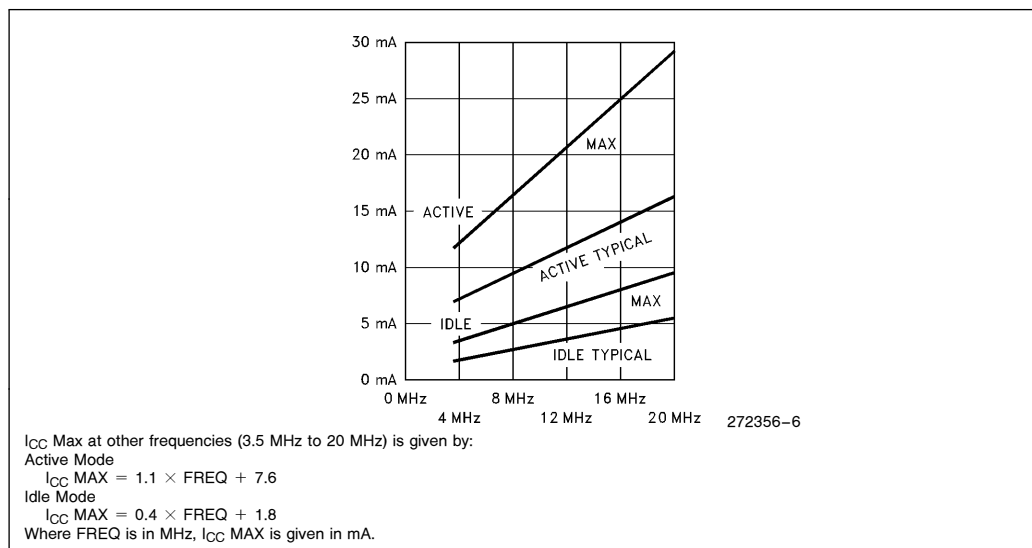Running the device with $\overline{EA}$ at a higher voltage than V_{CC} sinks additional currrent.

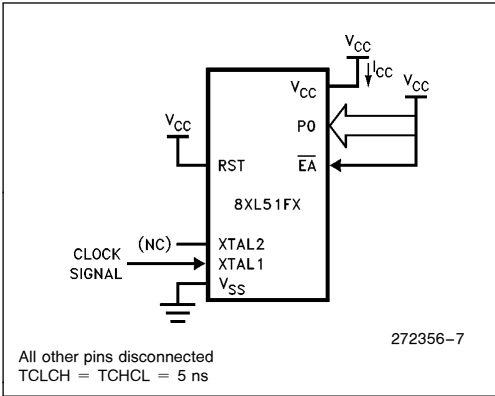I_{CC} Max at other frequencies (3.5 MHz to 20 MHz) is given by:
Active Mode
　I_{CC} MAX $= 1.1 \times$ FREQ $+ 7.6$
Idle Mode
　I_{CC} MAX $= 0.4 \times$ FREQ $+ 1.8$
Where FREQ is in MHz, I_{CC} MAX is given in mA.

272356–6

Figure 5. I_{CC} vs Frequency

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9

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All other pins disconnected
TCLCH = TCHCL = 5 ns

272356–7

Figure 6. I$_{CC}$ Test Condition, Active Mode

All other pins disconnected
TCLCH = TCHCL = 5 ns

272356–8
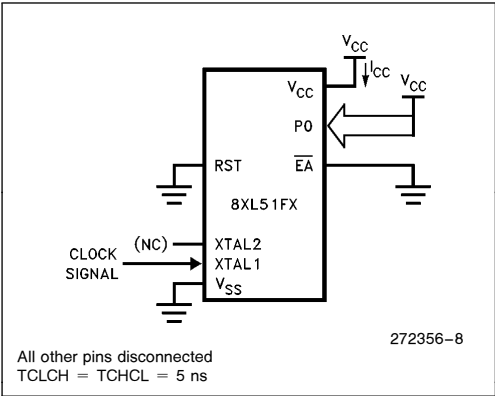
Figure 7. I$_{CC}$ Test Condition Idle Mode

All other pins disconnected
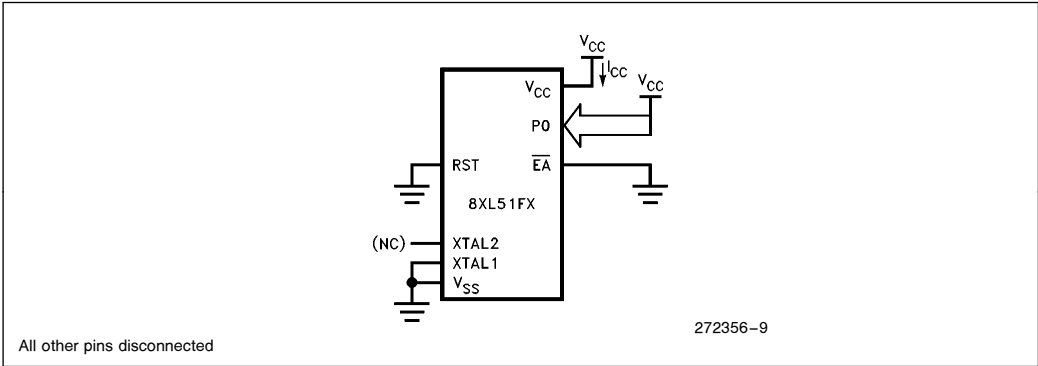
272356–9

**Figure 8. I$_{CC}$ Test Condition, Power Down Mode.
V$_{CC}$ = 2.7V to 3.6V.**

272356–10
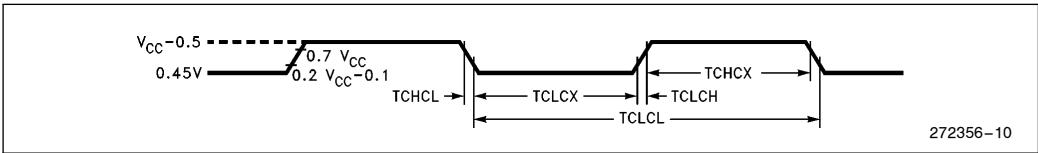
Figure 9. Clock Signal Waveform for I$_{CC}$ Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns.

ADVANCE INFORMATION

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address

C: Clock

D: Input Data

H: Logic level HIGH

I: Instruction (program memory contents)

L: Logic level LOW, or ALE

P: $\overline{PSEN}$

Q: Output Data

R: $\overline{RD}$ signal

T: Time

V: Valid

W: $\overline{WR}$ signal

X: No longer a valid logic level

Z: Float

For example,

TAVLL = Time from Address Valid to ALE Low

TLLPL = Time from ALE Low to $\overline{PSEN}$ Low

AC CHARACTERISTICS (Over Operating Conditions, Load Capacitance for Port 0, ALE/$\overline{PROG}$ and $\overline{PSEN}$ = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

EXTERNAL MEMORY CHARACTERISTICS

All parameter values apply to all devices unless otherwise indicated. In this table, 8XL51FX refers to 8XL51FX and 8XL51FX-1.
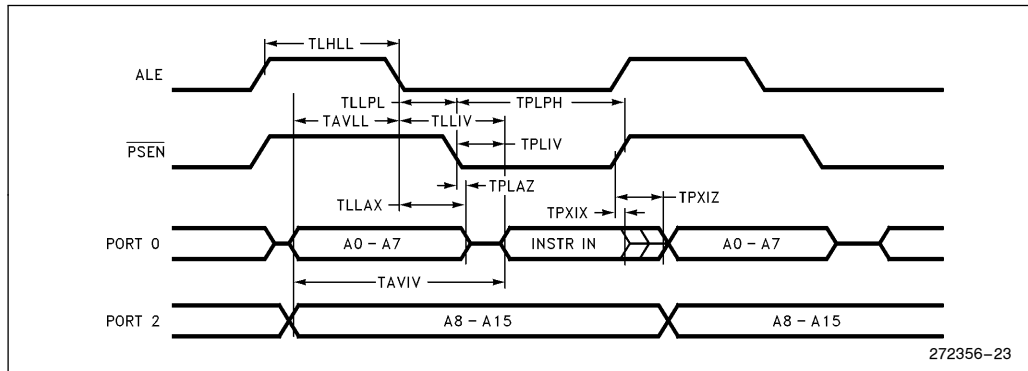
Symbol	Parameter	12 MHz Oscillator		20 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency 8XL51FX 8XL51FX-1 8XL51FX-20					3.5 3.5 3.5	12 16 20	MHz MHz MHz
TLHLL	ALE Pulse Width	127		60		2 TCLCL − 40		ns
TAVLL	Address Valid to ALE Low	43		10		TCLCL − 40		ns
TLLAX	Address Hold After ALE Low	53		20		TCLCL − 30		ns
TLLIV	ALE Low to Valid Instruction In 8XL51FX 8XL51FX-20		234		125		4 TCLCL − 100 4 TCLCL − 75	ns ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	53		20		TCLCL − 30		ns
TPLPH	$\overline{PSEN}$ Pulse Width	205		105		3 TCLCL − 45		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instruction In 8XL51FX 8XL51FX-20		145		60		3 TCLCL − 105 3 TCLCL − 90	ns ns
TPXIX	Input Instruction Hold After $\overline{PSEN}$	0		0		0		ns

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## EXTERNAL MEMORY CHARACTERISTICS (Continued)

All parameter values apply to all devices unless otherwise indicated.

Symbol	Parameter	12 MHz Oscillator		20 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	Min	Max	
TPXIZ	Input Instruction Float After $\overline{PSEN}$ 8XL51FX 8XL51FX-20		59		30		TCLCL − 25 TCLCL − 20	ns ns
TAVIV	Address to Valid Instruction In		312		145		5 TCLCL − 105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	400		200		6 TCLCL − 100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		200		6 TCLCL − 100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In 8XL51FX 8XL51FX-20		252		155		5 TCLCL − 165 5 TCLCL − 95	ns ns
TRHDX	Data Hold After $\overline{RD}$	0		0		0		ns
TRHDZ	Data Float After $\overline{RD}$		107		40		2 TCLCL − 60	ns
TLLDV	ALE Low to Valid Data In 8XL51FX 8XL51FX-20		517		310		8 TCLCL − 150 8 TCLCL − 90	ns ns
TAVDV	Address to Valid Data In 8XL51FX 8XL51FX-20		585		360		9 TCLCL − 165 9 TCLCL − 90	ns ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	100	200	3 TCLCL − 50	3 TCLCL + 50	ns
TAVWL	Address Valid to $\overline{WR}$ Low 8XL51FX 8XL51FX-20	203		110		4 TCLCL − 130 4 TCLCL − 90		ns ns
TQVWX	Data Valid before $\overline{WR}$ 8XL51FX 8XL51FX-20	33		15		TCLCL − 50 TCLCL − 35		ns ns
TWHQX	Data Hold after $\overline{WR}$ 8XL51FX 8XL51FX-20	33		10		TCLCL − 50 TCLCL − 40		ns ns
TQVWH	Data Valid to $\overline{WR}$ High 8XL51FX 8XL51FX-20	433		280		7 TCLCL − 150 7 TCLCL − 70		ns ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	10	90	TCLCL − 40	TCLCL + 40	ns

ADVANCE INFORMATION

EXTERNAL PROGRAM MEMORY READ CYCLE

272356-23

EXTERNAL DATA MEMORY READ CYCLE

272356-24
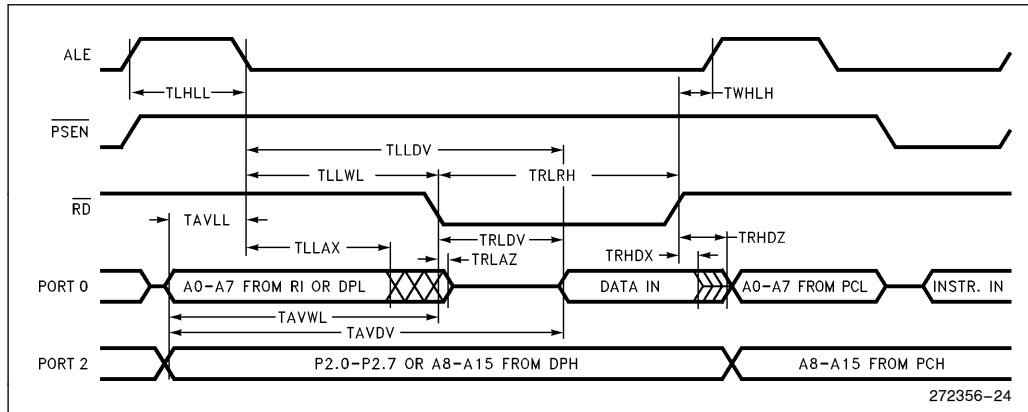
## EXTERNAL DATA MEMORY WRITE CYCLE

272356-25
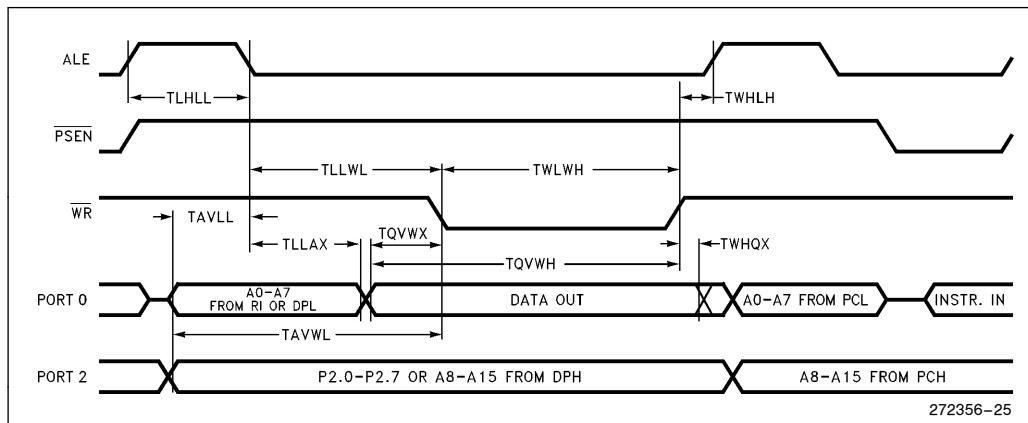
SERIAL PORT TIMING - SHIFT REGISTER MODE

Test Conditions: Over Operating Conditions; Load Capacitance = 80 pF

Symbol	Parameter	12 MHz Oscillator		20 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1		0.600		12 TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		367		10 TCLCL − 133		ns
TXHQX	Output Data Hold after Clock Rising Edge 8XC5X 8XC5X-20	50		50		2 TCLCL − 117 2 TCLCL − 50		ns ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		367		10 TCLCL − 133	ns

SHIFT REGISTER MODE TIMING WAVEFORMS

272356−26

ADVANCE INFORMATION
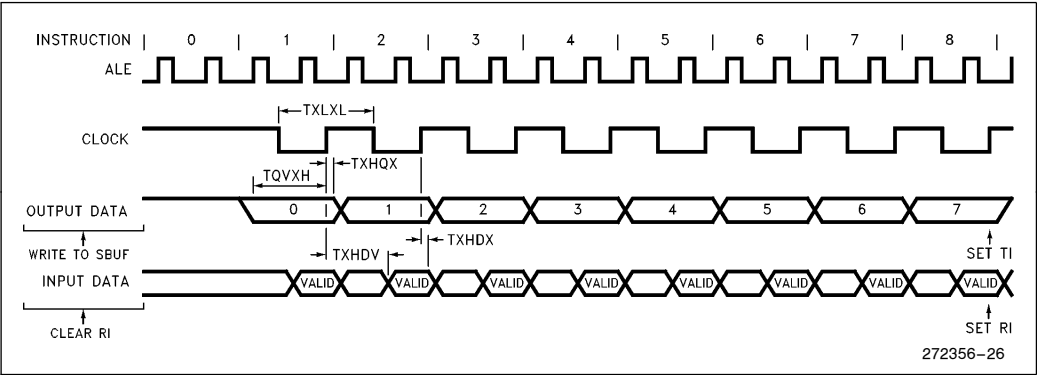
EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency 8XL51FX 8XL51FX-1 8XL51FX-20	 3.5 3.5 3.5	 12 16 20	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM

272356-27
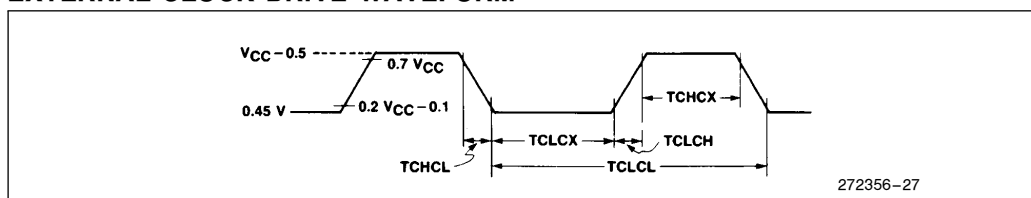
AC TESTING INPUT, OUTPUT WAVEFORMS

272356-28

AC Inputs during testing are driven at $V_{CC}-0.5V$ for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} min for a Logic "1" and V_{IL} max for a Logic "0".

FLOAT WAVEFORMS

272356-29

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} = \pm 20$ mA (-L, $I_{OL}/I_{OH} = \pm 10$ mA).

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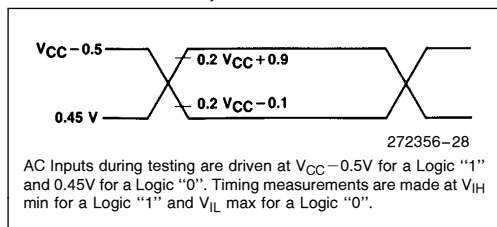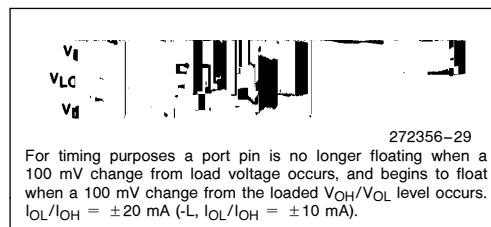
PROGRAMMING THE OTP ROM

To be programmed, the part must be running with a 4 to 6 MHz oscillator. (The reason the oscillator needs to be running is that the internal bus is being used to transfer address and program data to appropriate internal OTP ROM locations.) The address of an OTP ROM location to be programmed is applied to Port 1 and pins P2.0 - P2.4 of Port 2, while the code byte to be programmed into that location is applied to Port 0. The other Port 2 and 3 pins, RST PSEN, and EA/V$_{PP}$ should be held at the "Program" levels indicated in Table 3. ALE/PROG is pulsed low to program the code byte into the addressed OTP ROM location. The setup is shown in Figure 10.

Normally EA/V$_{PP}$ is held at logic high until just before ALE/PROG is to be pulsed. Then EA/V$_{PP}$ is raised to V$_{PP}$, ALE/PROG is pulsed low, and then EA/V$_{PP}$ is returned to a valid high voltage. The voltage on the EA/V$_{PP}$ pin must be at the valid EA/V$_{PP}$ high level before a verify is attempted. Waveforms and detailed timing specifications are shown in later sections of this data sheet.

NOTE:

- EA/V$_{PP}$ pin must not be allowed to go above the maximum specified V$_{PP}$ level for any amount of time. Even a narrow glitch above that voltage level can cause permanent damage to the device. The V$_{PP}$ source should be well regulated and free of glitches.

Table 3. OTP ROM Programming Modes

(H = 2.7V to 3.6V; H1 = 5V ±10%)

Mode		RST	PSEN	ALE/ PROG	EA/ V$_{PP}$	P2.6	P2.7	P3.3	P3.6	P3.7	V$_{CC}$
Program Code Data		H1	L	⊔	12.75V	L	H1	H1	H1	H1	H1
Verify Code Data		H	L	H	H	L	L	L	H	H	H
Program Encryption Array Address 0–3FH		H1	L	⊔	12.75V	L	H1	H1	L	H1	H1
Program Lock Bits	Bit 1	H1	L	⊔	12.75V	H1	H1	H1	H1	H1	H1
	Bit 2	H1	L	⊔	12.75V	H1	H1	H1	L	L	H1
	Bit 3	H1	L	⊔	12.75V	H1	L	H1	H1	L	H1
Read Signature Byte		H	L	H	H	L	L	L	L	L	H

*See Table 2 for proper input on these pins

272356–18

Figure 10. Programming the OTP ROM

ADVANCE INFORMATION

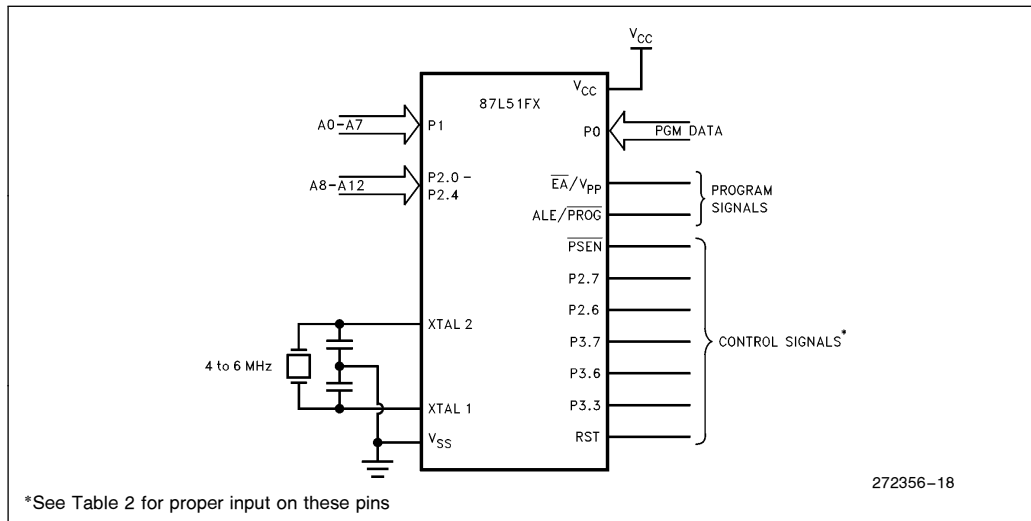## intel

PROGRAMMING ALGORITHM

Refer to Table 3 and Figures 10 and 11 for address, data, and control signals set up. To program the 87L51FX the following sequence must be exercised.

1. Input the valid address on the address lines.

2. Input the appropriate data byte on the data lines.

3. Activate the correct combination of control signals.

4. Raise $\overline{EA}$/V$_{PP}$ from V$_{CC}$ to 12.75V $\pm$0.25V.

5. Pulse, ALE/$\overline{PROG}$ 5 times for the OTP ROM array, and 25 times for the encryption table and the lock bits.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

PROGRAM VERIFY

Program verify may be done after each byte or block of bytes is programmed. In either case a complete verify of the programmed array will ensure reliable programming of the 87L51FX.

The lock bits cannot be directly verified. Verification of the lock bits is done by observing that their features are enabled.
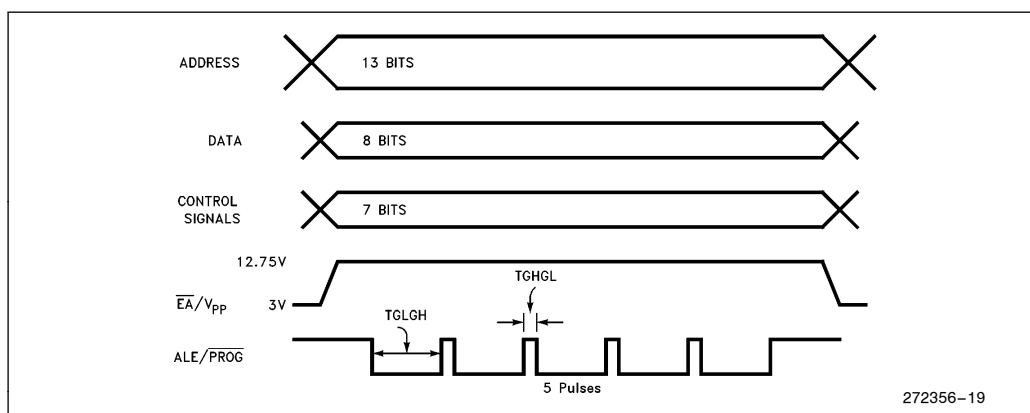

Figure 11. Programming Signals Waveforms

ROM and OTP ROM Lock System

The 87L51FX program lock system, when programmed, protects the onboard program against software piracy.

The 83L51FX has a one-level program lock system and a 64-byte encryption table. See line 2 of Table 4. If program protection is desired, the user submits the encryption table with their code, and both the lock-bit and encryption array are programmed by the factory. The encryption array is not available without the lock bit. For the lock bit to be programmed, the user must submit an encryption table.

The 87L51FX has a 3-level program lock system and a 64-byte encryption array. Since this is an OTP ROM device, all locations are user-programmable. See Table 4.

Encryption Array

Within the OTP ROM array are 64 bytes of Encryption Array that are initially unprogrammed (all 1's). Every time that a byte is addressed during a verify, 6 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an Encryption Verify byte. The algorithm, with the array in the unprogrammed state (all 1's), will return the code in its original, unmodified form. For programming the Encryption Array, refer to Table 3 (Programming the OTP ROM).

When using the encryption array, one important factor needs to be considered. If a code byte has the value 0FFH, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the contents of the encryption array. For this reason all unused code bytes should be programmed with some value other than 0FFH, and not all of them the same value. This will ensure maximum program protection.

Table 4. Program Lock Bits and the Features

Program Lock Bits			Protection Type
	LB1	LB2	LB3	

	LB1	LB2	LB3	Protection Type
1	U	U	U	No Program Lock features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on Reset, and further programming of the OTP ROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, also external execution is disabled.

Any other combination of the lock bits is not defined.

Program Lock Bits

The 87L51FX has 3 programmable lock bits that when programmed according to Table 4 will provide different levels of protection for the on-chip code and data.

Reading the Signature Bytes

The 87L51FX/83L51FX has 3 signature bytes in locations 30H, 31H, and 60H. To read these bytes follow the procedure for OTP ROM verify, but activate the control lines provided in Table 3 for Read Signature Byte.
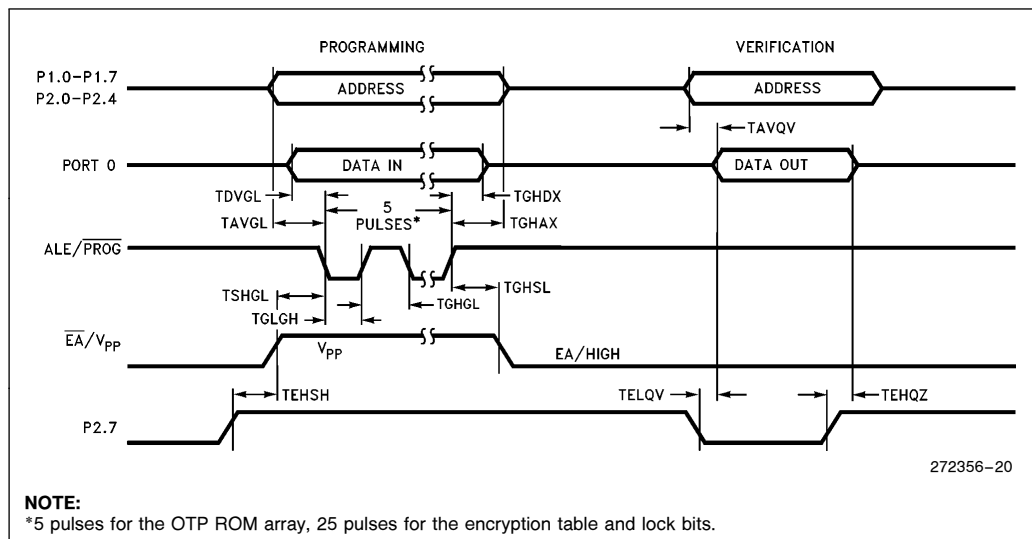
Location	Device	Contents
30H	All	89H
31H	All	58H
60H	83L51FA	70H
	87L51FA	F0H
	83L51FB	71H
	87L51FB	F1H
	83L51FC	72H
	87L51FC	F2H

ADVANCE INFORMATION

OTP ROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C; V_{CC} = 2.7V to 3.6V; V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	P2.7 (ENABLE) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		μs
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		μs
TGLGH	$\overline{PROG}$ Width	90	100	μs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	ENABLE Low to Data Valid		48TCLCL	
TEHQZ	Data Float after ENABLE	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		μs

OTP ROM PROGRAMMING AND VERIFICATION WAVEFORMS

272356–20

NOTE:
*5 pulses for the OTP ROM array, 25 pulses for the encryption table and lock bits.

Thermal Impedance

The thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditionis and applications. See the Intel Packaging Handbook (Order Number 240800) for a description of Intel's thermal impedance test methodology.

Package	θ_{JA}	θ_{JC}	Device
N	46°C/W	16°C/W	All
S	87°CW	18°C/W	52
	96°C/W	24°C/W	54
	90°C/W	22°C/W	58

Data Sheet Revision History

This 8XL51FA/FB/FC data sheet (Advanced Information) replaces 272356-001 (Product Preview).

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