83C51KB
Hardware Description

Addendum to the MCS® 51 Microcontroller Family User's Manual

Order Number: 272801-001
January, 1996

1.0 INTRODUCTION TO THE 83C51KB

The 83C51KB is an application specific read-only-memory (ROM) microcontroller. The 83C51KB is designed as a keyboard scanner and is architecturally similar but not identical to the 80C51BH. Certain features not on the 80C51 have been added to support keyboard scanning. In order to streamline 83C51KB cost/performance factors, 80C51 peripherals not applicable to keyboard scanning are no longer present.

Refer to the *MCS® 51 Microcontroller Family User's Manual* (order number 272383) for a complete description of the 80C51. Figure 1 contains a basic memory map of the architecture. 83C51KB electrical information is contained in the datasheet (order number 272800).

1.1 Comparing the 80C51BH and 83C51KB

The differences between the 83C51KB and the 80C51 are briefly described here.

- The 83C51KB contains circuitry to support use of an RC clock oscillator. The 80C51 has a crystal clock oscillator.
- The 83C51KB has one 16-bit timer/counter (TH0, TL0). This timer is identical with Timer 0 on the 80C51. Other 80C51 timers are not present on the 83C51KB.
- The 83C51KB is designed to communicate with the keyboard controller on a personal computer (PC) through the CLK and DATA signals. The 80C51 has a serial port that is not present in the 83C51KB.
- 80C51 ROM security features are not present on the 83C51KB.
- The 80C51 reset operation is retained but the 83C51KB device also provides an automatic internal reset during power-up.
- Two new bits are implemented in the 83C51KB PCON register. One bit selects an interrupt for the KSI port, and the other controls the enhanced pullups for CLK and DATA signals.
- The 83C51KB has the same idle and power down modes as the 80C51. However, the 83C51KB differs in one respect. In the 83C51KB, either a hardware reset or an external interrupt can terminate the power down operation. The 80C51 is limited to a hardware reset termination of this mode.
- With the exception of port 2, some 80C51 port signals on the 83C51KB have been modified to facilitate keyboard scanning operation.
  - — All 83C51KB ports are now quasi-bidirectional outputs and require no external pullups. The 80C51 had an open-drain design on the port 0 outputs and needed external pullups.
  - — The 83C51KB port 1 circuitry contains new logic to generate an interrupt when enabled and any port 1 pin is pulled to V_{IL}. This feature supports the key-scan input (KSI) operation.
  - — Some 83C51KB port 3 signals are new. Enhanced pullups are available on two Port 3 signals to support the new CLK and DATA functions. Four port 3 outputs now allow direct LED connection.

This document presents a thorough description of the on-chip hardware features of the 83C51KB. It begins with a discussion of the individual signals and on-chip memory and then discusses each peripheral.

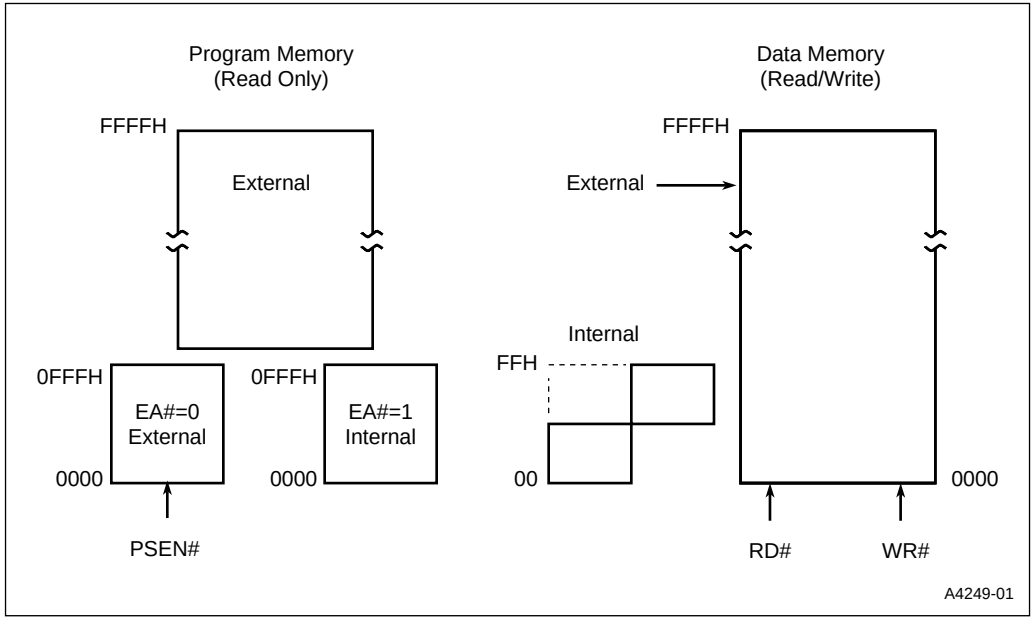


Figure 1. 83C51KB Memory Map

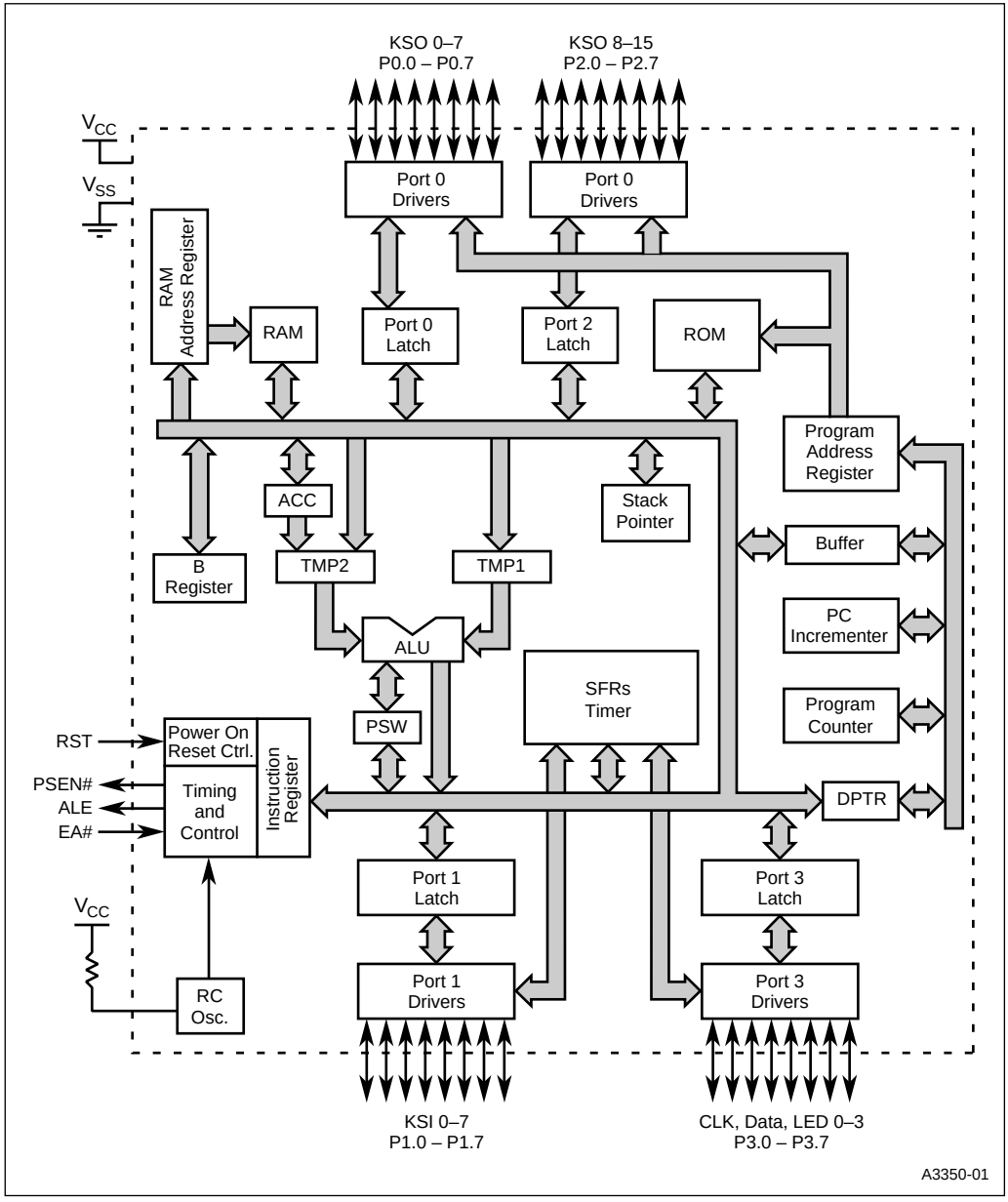


Figure 2. 83C51KB Block Diagram

2.0 SIGNAL SUMMARY

There are forty primary pin functions on the 83C51KB with some alternate functions.

The following tables provide a summary of these signals.

Table 1. 40-pin DIP Signals Arranged by Name

Keyboard	
Name	**Pin**
P0.7/KSO7/AD7	32
P0.6/KSO6/AD6	33
P0.5/KSO5/AD5	34
P0.4/KSO4/AD4	35
P0.3/KSO3/AD3	36
P0.2/KSO2/AD2	37
P0.1/KSO1/AD1	38
P0.0/KSO0/AD0	39
P2.7/KSO15/A15	28
P2.6/KSO14/A14	27
P2.5/KSO13/A13	26
P2.4/KSO12/A12	25
P2.3/KSO11/A11	24
P2.2KSO10/A10	23
P2.1/KSO9/A9	22
P2.0/KSO8/A8	21

Keyboard	
Name	**Pin**
P 1.0/KSI0	1
P1.1/KSI1	2
P1.2/KSI2	3
P1.3/KSI3	4
P1.4/KSI4	5
P1.5/KSI5	6
P1.6/KSI6	7
P1.7/KSI7	8
P3.0/DATA	10
P3.1	11
P3.2/CLK0/INT0#	12
P3.3/CLK1/INT1#	13
P3.4/LED0/T0	14
P3.5/LED1	15
P3.6/LED2/WR#	16
P3.7/LED3/RD#	17

Chip Control	
Name	**Pin**
RCIN	19
RST	9
ALE	30
PSEN#	29
EA#	31

Power & Ground	
Name	**Pin**
V_{CC}	40
V_{SS}	20

Table 2. 40-pin DIP Signals Arranged by Pin Number

Pin	Name	Pin	Name
1	P 1.0/KSI0	21	P2.0/KSO8/A8
2	P1.1/KSI1	22	P2.1/KSO9/A9
3	P1.2/KSI2	23	P2.2KSO10/A10
4	P1.3/KSI3	24	P2.3/KSO11/A11
5	P1.4/KSI4	25	P2.4/KSO12/A12
6	P1.5/KSI5	26	P2.5/KSO13/A13
7	P1.6/KSI6	27	P2.6/KSO14/A14
8	P1.7/KSI7	28	P2.7/KSO15/A15
9	RST	29	PSEN#
10	P3.0/DATA	30	ALE
11	P3.1	31	EA#
12	P3.2/CLK0/INT0#	32	P0.7/KSO7/AD7
13	P3.3/CLK1/INT1#	33	P0.6/KSO6/AD6
14	P3.4/LED0/T0	34	P0.5/KSO5/AD5
15	P3.5/LED1	35	P0.4/KSO4/AD4
16	P3.6/LED2/WR#	36	P0.3/KSO3/AD3
17	P3.7/LED3/RD#	37	P0.2/KSO2/AD2
18	NC	38	P0.1/KSO1/AD1
19	RCIN	39	P0.0/KSO0/AD0
20	V_{SS}	40	V_{CC}

Table 3. Signal Descriptions

Signal Name	Type	Description	Alternate Function
A15:8†	O	**Address Signals**. Upper address lines for the external bus. These signals are normally used for the KSO15:8 scan function and are not available for external memory access in a keyboard application. (See KSO signals).	KSO.15:8 P2.15:8
AD7:0†	I/O	**Address/Data Signals**. Multiplexed lower address and data signals for external memory. These signals are normally used for the KSO7:0 scan function and are not available for external memory access in a keyboard application. (See KSO)	KSO.7:0 P0.7:0
ALE†	O	**Address Latch Enable**. ALE signals the start of an external bus cycle and indicates that valid address information is available on lines A15:8 and AD7:0. Since these external address signals are normally used for the KSO scan function, the ALE should not be used for external memory access in a keyboard application. ALE can be disabled when not used for external memory access by setting bit 0 of SFR AUXR at address 8EH.	
CLK1:0 P3.3:2	I/O	**Clock signal**. Either P3.2 or P3.3 is configurable with a 1.8KΩ pullup and with external interrupt INT0# or INT1# and used as keyboard CLK signal.	INT1:0#
DATA P3.0	I/O	**DATA signal**. P3.0 is configurable with a 1.8KΩ pullup and used as a keyboard Data signal..	
EA#	I	**External Access**. Directs program memory accesses to on-chip or off-chip code memory. For EA# = 0, all program memory accesses are off-chip. EA# should always be strapped to V_{CC} for keyboard applications using the 83C51KB.	
INT1:0#†	I	**External Interrupts 0 and 1**. These inputs set bits IE1:0 in the TCON register. If bits IT1:0 in the TCON register are set, bits IE1:0 are set by a falling edge on INT1#/INT0#. If bits INT1:0 are clear, bits IE1:0 are set by a low level on INT1:0#. For keyboard applications, these signals are normally used for the CLK signals. (See KSIINT and CDPU bits in the PCON register)	CLK1:0 P3.3:2
KSI7:0 P1.7:0	I/O	**Keyboard Scan Inputs**. Application specific keyboard signals.	
KSO15:0 P2.15:8 P0.7:0	I/O	**Keyboard Scan Outputs**. The KSO signals are application specific to keyboard scan functions.	
LED3:0 P3.7:4	I/O	**Light Emitting Diode Drivers**. The LED signals are specifically designed to drive LEDs connected to Vcc directly (see D.C. Characteristics). The alternate functions are not available for keyboard applications.	RD#, WR#, T0
N/C	—	**No Connection Signal**. This signal is to be unconnected.	
P0.7:0†	I/O	**Port 0**. This is an 8-bit quasi-bidirectional I/O port (see KSO signals, see also AD7:0).	AD7:0
P1.7:0	I/O	**Port 1**. This is an 8-bit quasi-bidirectional I/O port (see KSI signals).	
P2.7:0	I/O	**Port 2.** This is an 8-bit quasi-bidirectional I/O port (see also A15:8).	A15:8
P3.7:0	I/O	**Port 3**. This is an 8-bit quasi-bidirectional I/O port (see CLK1:0, DATA, LED3:0).	

† The descriptions of RD#, WR#, ALE, PSEN#, A15:8/P2.7:0 and AD7:0/P0.7:0 are documented for the standard MCS 51 microcontrollers. They are not used for these functions in keyboard applications.

Table 3. Signal Descriptions (Continued)

Signal Name	Type	Description	Alternate Function
PSEN#†	O	**Program Store Enable**. This output is asserted for external program memory fetch operations. It is not available for keyboard applications.	—
RCIN	I	**Resonant Clock Input.** The internal RC signal is generated by connecting a resistor to V_{CC} or provide an external clock input from an external clock device (see Figure).	
RD#†	O	**Read.** Read signal output for external data memory fetch operations. It is not available for keyboard applications.	LED3
RST	I	**Reset**. Asserting RST when the chip is in idle mode or powerdown mode returns the chip to normal operation. This signal is input only.	—
V_{CC}	PWR	**Supply Voltage**. Connect this pin to the +5V supply voltage.	—
V_{SS}	GND	**Circuit Ground**. Connect this pin to ground.	—
WR#†	O	**Write**. Write signal output for external memory write operations. It is not available for keyboard applications.	LED2

† The descriptions of RD#, WR#, ALE, PSEN#, A15:8/P2.7:0 and AD7:0/P0.7:0 are documented for the standard MCS 51 microcontrollers. They are not used for these functions in keyboard applications.

3.0 MEMORY ORGANIZATION

All MCS-51 devices have two primary memory types; program (instruction code) and data memory. Up to 64 Kbytes each of program and data memory may be addressed. Each memory type is a combination of on-chip and off-chip memory. The 83C51KB contains 4 Kbytes of on-chip program memory. In addition to external data memory, the 83C51KB also consists of 128 bytes of on-chip data RAM and 128 bytes of special function registers (SFRs).

3.1 Program Memory

If the EA# pin is connected to VSS, all program (instruction code) fetches are directed to an external 64K-byte memory system (0000H to FFFFH). During external instruction fetch cycles the PSEN# signal is activated to enable program code output from the external memory system. If the EA# pin is connected to VCC, then program fetches to addresses 0000H through 0FFFH are directed to internal ROM and fetches to addresses 1000H through FFFFH are to the external memory system. After the reset operation completes, the 83C51KB execution unit fetches and executes the instruction code located at the reset vector address (0000H).

3.2 Data Memory

Up to 64K bytes of data RAM may be designed into the external memory system. The external data memory is accessed with indirect address instructrions (i.e. MOVX). Using these indirect instructions activates the RD# or WR# signal for external data transfer operations.

3.3 Using External Memory

When the 83C51KB execution unit needs external program or data memory, all port 0 pins are used for low-order address signals. The bus interface unit contains an address/data multiplexer and also uses port 0 for data transfer. All port 2 pins are used for high-order address output (except when MOVX @Ri is used). These signals may not be used for general purpose input/output under these conditions.

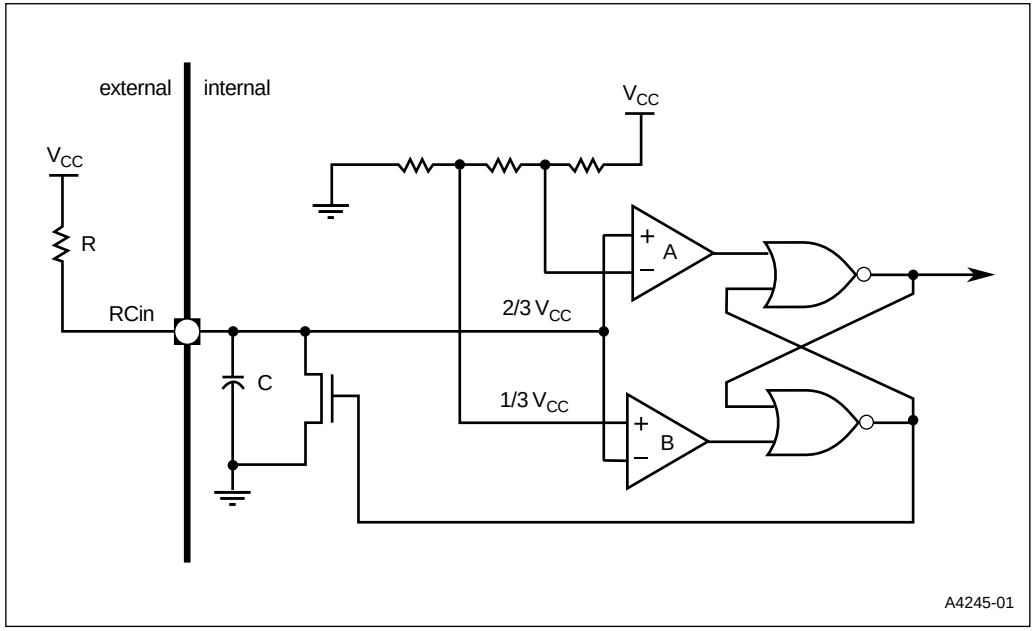
3.4 On-Chip Special Function Registers (SFRs) and RAM

The 83C51KB implements 128 bytes of on-chip RAM (00H to 7FH). This is accessible using direct or indirect addressing. There are four 8-byte general purpose register banks (address 00H to 1FH) and 16 bytes of bit addressable data memory

(address 20H to 2FH). Special function registers are located from 80H to FFH. SFRs can only be accessed with direct address instructions. The shaded SFR addresses in Table 4 are reserved.

Table 4. Special Function Register Map

	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8									FF
F0	B 00000000								F7
E8									EF
E0	ACC 00000000								E7
D8									DF
D0	PSW 00000000								D7
C8									CF
C0									C7
B8	IP xxxx0000								BF
B0	P3 11111111							IPH xxxx0000	B7
A8	IE 0xxx0000								AF
A0	P2 11111111								A7
98									9F
90	P1 11111111								97
88	TCON 00000000	TMOD xxxx0000	TL0 00000000		TH0 00000000		AUXR xxxxxxx0		8F
80	P0 11111111	SP 00000111	DPL 00000000	DPH 00000000				PCON 00x00000	87
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	



RC Oscillator

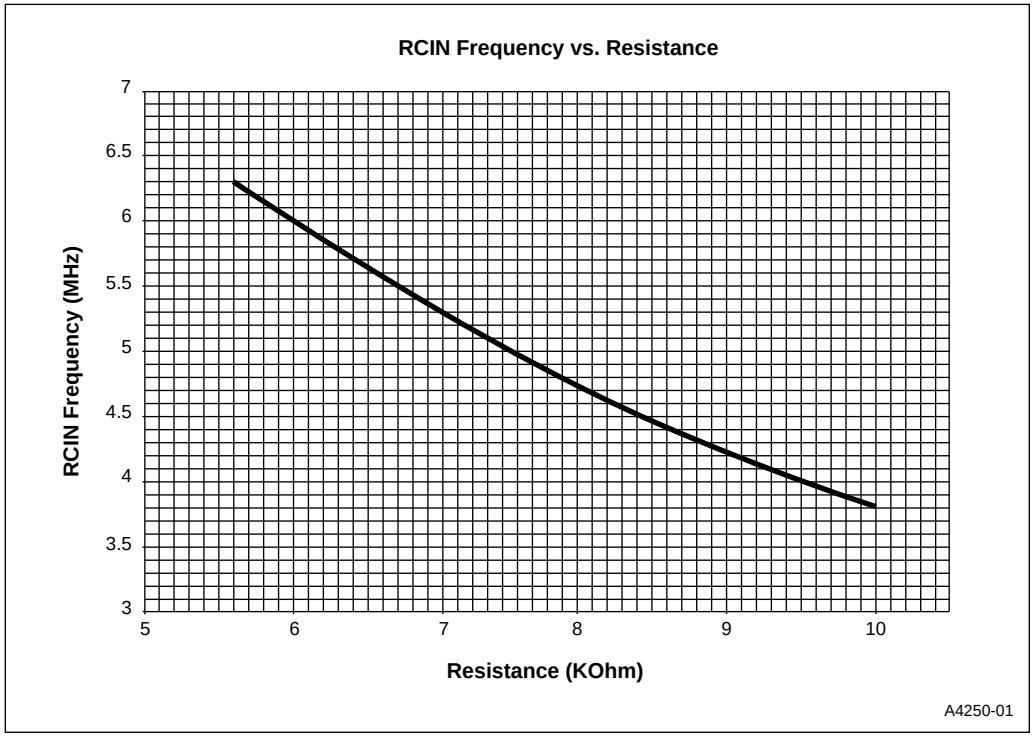
4.0 RC OSCILLATOR

The 83C51KB contains an RC oscillator. The timing is set by a single external resistor connected between the RCIN pin and V_{CC}. The charge time of the circuit is illustrated in formula. The oscillator circuit is shown in Figure .

The circuit operates as follows. Capacitor C charges through the external resistor R, until its voltage reaches 2/3 V_{CC}. At that point comparator A switches the NOR-gate latch, turning on the pulldown transistor.

Then C discharges through this transistor until its voltage falls to 1/3 V_{CC}. At that point comparator B switches the NOR-gate latch, turning off the pulldown transistor, and the cycle repeats. The time it takes the capacitor to charge from 1/3 V_{CC} to 2/3 V_{CC} is:

$$T\ (Charge) = RC \times \ln 2$$



RCIN Frequency (5VDC at Room Temperature)

The circuit is designed to discharge the capacitor very quickly and therefore the corresponding charge time is the primary parameter in the oscillation period. Charge time is controlled with an external resistor. A ±5% variation of the RC resonator frequency is achievable with a 1% precision external resistor (assuming stable VCC and temperature). Reduced resistor precision results in a wider variation of frequency. Detailed specifications of oscillation frequency as a function of external resistance values are presented in the datasheet. A generalized chart is presented in Figure .

The RCIN pin can also be driven with an external oscillator. The external circuit will have to meet the I_{IH} spec for this pin. The I_{IH} spec for this pin is higher than for others, because when the RCIN pin is at a logic high the pulldown FET is on.

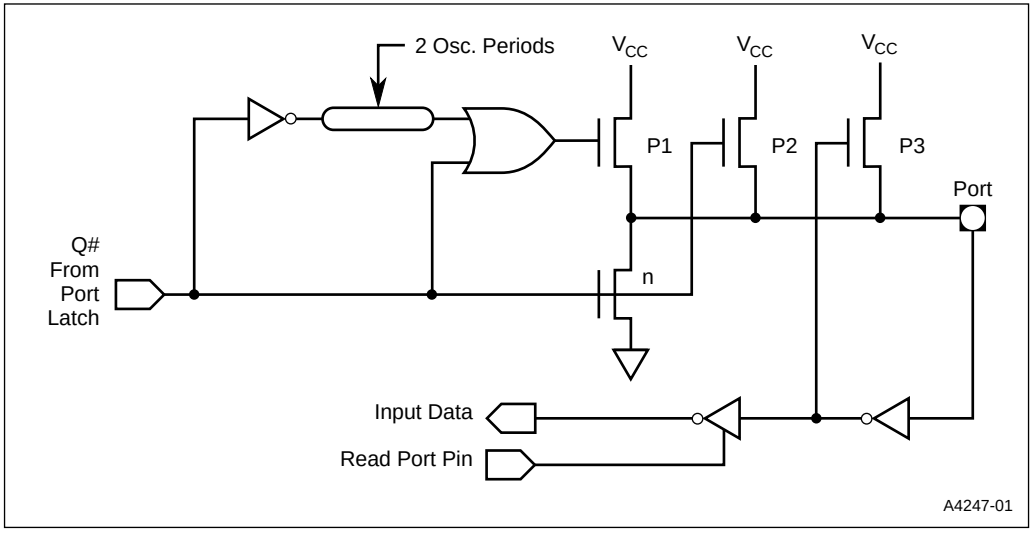
5.0 83C51KB PORT DESIGN

All four input/output ports are quasi-bidirectional structures. If the data change on a port requires a 0-to-1 transition, an additional pullup is turned on. This is done to increase the transition speed. The extra pullup can source about 100 times normal current levels. The internal pullups are field-effect transistors, not linear resistors. The pull-up arrangement is shown in Figure 5.1 and described in the following paragraphs.

The pullup consists of three p-channel (pFET) transistor devices and the pulldown consists of one n-channel (nFET) device. Note that the nFET is turned on when a logical 1 is applied to its gate, and is turned off when a logical 0 is applied to its gate. Conversely the pFET is on when the gate sees a 0, and off when the gate is at 1. The device labeled P1 in Figure 5.1 is the transistor that is turned on for 2 oscillator periods after a 0-to-1 transition in the port latch. A 1 at the port pin turns on P3 (a weak pull-

up), through the inverter. This inverter and pFET form a latch which hold the 1.

If the pin is emitting a 1, a negative glitch on the pin from some external source can turn off P3, causing the pin to go into a float state. P2 is a very weak pullup which is on whenever the nFET is off, in traditional CMOS style. It's only about 1/10 the strength of P3. Its function is to restore a 1 to the pin in the event the pin had a 1 and lost it to a glitch. P1 is turned on for 2 oscillator periods after Q makes a 0-to-1 transition. During this time, P1 also turns on P3 through the inverter to form a latch which holds the 1. P2 is also on. Port 2 is similar except that it holds the strong pullup on while emitting 1s that are address bits.The output buffers may each sink 3.2 mA at 0.45 VDC. These port pins can be driven by open-collector and open-drain outputs although 0-to-1 transitions will not be fast since there is little current pulling the pin up. An input 0 turns off pullup P3, leaving only the very weak pullup P2 to drive the transition. With the exception of port 2, some 80C51 port signals on the 83C51KB have been modified to facilitate keyboard scanning operation.



5.1 Port Pullup Configuration Port 1

Port 1 is the same on the 83C51KB as on the 80C51, except that logic has been added to generate an interrupt when any of the Port 1 pins is pulled low, as shown in Figure 6. The interrupt can be directed to either INT0# or INT1#, depending on the state of the KSIINT bit, bit 6 in the PCON register. KSIINT = 0 directs the interrupt to INT0#. KSIINT = 1 directs it to INT1#.

NOTE: KSIINT = 0 disconnects INT0# from the P3.2 pin, and KSIINT = 1 disconnects INT1# from the P3.3 pin.

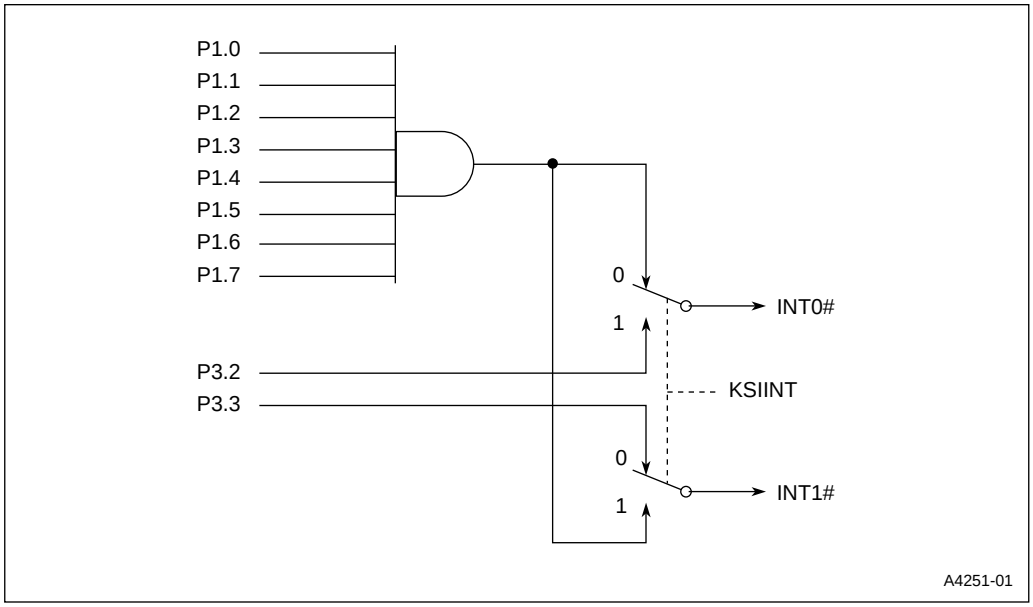


Figure 3. Port 1 and Port 3 KSIINT Structure

5.2 Port 3

As the 83C51KB has no UART or Timer 1, the port 3 alternate functions associated with these peripherals are not applicable.

Communication with the keyboard controller on the PC motherboard is accomplished with the DATA and CLK signals. The port 3.0 signal and either port 3.2 or port 3.3 are used as the DATA and CLK signals. In keyboard applications the enhanced strength pullup device is enabled on the port by setting the CDPU bit (PCON.7).

When the KSI port uses INT0# (e.g. KSIINT = 0), then the enhanced pullups need to be enabled on port 3.0 and port 3.3 (INT1#). The port 3.0 pin is then used for the DATA signal and the port 3.3 (INT1#) pin is used for the CLK signal.

When the KSI port uses INT1# (e.g. KSIINT = 1), then the enhanced pullups are enabled on port 3.0 and port 3.2 (INT0#). The port 3.0 pin is used for DATA and the port 3.2 (INT0#) pin is used for CLK. The combined effects of the CDPU and KSIINT bits are shown in Table 5.

Table 5. CDPU and KSIINT Affects on Port 3

PCON.7	**PCON.6**	**P3.0**	**P3.2**	**P3.3**	**Keyboard Functions**	
CDPU	KSIINT	pullup	pullup	pullup	DATA	CLK
0	X	normal	normal	normal		
1	0	enhanced	normal	enhanced	P3.0	P3.3
1	1	enhanced	enhanced	normal	P3.0	P3.2

This arrangement allows either external interrupt to be used for the KSI port, and leaves the other external interrupt, with an enhanced pullup, available for CLK. The reset values of CDPU and KSIINT are both zero (see Figure 5).

Four outputs of port 3 (see Figure 4) have pulldown devices sized to limit their drain currents to a safe maximum on each pin when used to drive LEDs. The protected pins are port 3.7:4. Each output can drive an LED directly, as shown in Figure 4. Writing a one to the port pin turns the LED off, and writing a zero turns the LED on. When on, the LED voltage drop is about 2 VDC and raises V_{OL} to approximately 3 VDC. The drain current of the pulldown transistor is limited by the I_D / V_{DS} device characteristic.

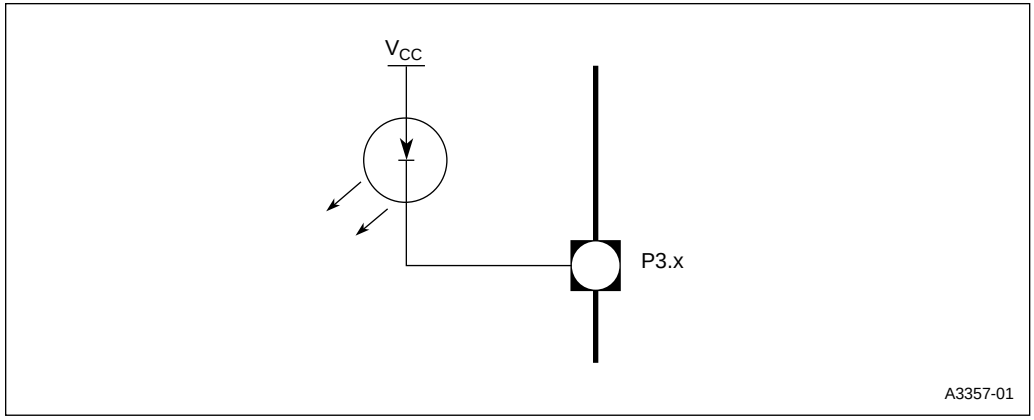


Figure 4. Driving an LED with P3.7:4

6.0 POWER-ON RESET

A special feature of the 83C51KB makes it possible to effect a power-on reset with no external components connected to the reset (RST) pin. When power is applied to the chip, the internal reset signal remains high for approximately 80ms to 260ms (see the datasheet for current specifications). During operation, should VCC fall below 3VDC and then return to normal operating levels, a seperate internal reset will be generated. The internal reset signal does not appear as an output on the RST pin, and the RST pin retains its full functionality. Additional reset time can be accomplished with an external capacitor connected between RST and VCC.

7.0 IDLE AND POWER DOWN

The Idle and power down modes are identical to the 80C51 with one exception. The 83C51KB power down can be terminated by either of the external interrupt request pins (INT0# or INT1#). Both the global interrupt bit and the individual interrupt must be enabled in the interrupt enable register (see Figure 8). The power control bits in the PCON register are located in the special function register area (address 87H, see Figure 5).

An instruction that sets the power down (PD) bit at PCON.1 is the last instruction executed prior to the power down sequence. In this mode the RC oscillator is stopped. With no internal clock signal, all chip functions are halted. The on-chip RAM and special function registers continue to retain their data. The port pins also continue to drive the values held by their respective SFRs. The ALE and PSEN# signals are driven low.

The VCC power supply can be reduced as low as 2VDC. However, lowering VCC below 3VDC and then raising it again generates an automatic power-on reset (see section 6.0 Power-On Reset).

The 83C51KB can exit power down mode with either a reset or an external interrupt request. The external interrupt (INT0# or INT1#) must be enabled and configured in the level-sensitive mode. Driving

the interrupt signal low restarts the oscillator. Driving the interrupt signal high completes the exit from power down. After the RETI instruction is executed in the interrupt service routine (ISR), the next instruction to be executed follows the instruction that set the PCON.1 (PD) bit.

PCON

Address: 87H
Reset State: 00X0 0000B

Power Control Register. Contains the power off flag (POF) and bits for enabling the idle and powerdown modes. Also contains two general-purpose flags and two bits that control serial I/O functions—the double baud rate bit and a bit that selects whether accesses to SCON.7 are to the FE bit or the SM0 bit.

7 **0**

CDPU	KSIINT	—	POF	GF1	GF0	PD	IDL

Bit Number	Bit Mnemonic	Function
7	CDPU	Setting this bit enhances the pullup strength on port 3 keyboard signals. This bit works in concert with KSIINT (PCON.6). Refer to Table 5.
6	KSIINT	Setting this bit enhances the pullup strength on port 3 keyboard signals. This bit works in concert with CDPU (PCON.7). Refer to Table 5.
5	—	Reserved.
4	POF	Power Off Flag. Set by hardware on rising edge of V_{CC}. Set or cleared by software. Detects resets caused by power failures. V_{CC} must remain above 3 VDC to retain the flag value.
3	GF1	General Purpose Flag: Set or cleared by software. One use is to indicate whether an interrupt occurred during normal operation or during idle mode.
2	GF0	General Purpose Flag: Set or cleared by software. One use is to indicate whether an interrupt occurred during normal operation or during idle mode.
1	PD	Powerdown Mode Bit: When set, activates powerdown mode. Cleared by hardware when an interrupt or reset occurs.
0	IDL	Idle Mode Bit: When set, activates idle mode. Cleared by hardware when an interrupt or reset occurs. If IDL and PD are both set, PD takes precedence.

Figure 5. Power Control Register

8.0 TIMER 0

The 83C51KB has one 16-bit timer/counter (Timer 0). The timer consists of two 8-bit registers, TH0 and TL0. This peripheral circuit can be configured to operate either as a timer or event counter.

In the timer function, the peripheral register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the counter function, the register is incremented in response to a negative transition on a corresponding external input pin; in this case T0 configured as an alternate function to the port 3.4 pin. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (24 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

The Timer or Counter function is selected by control bits C/T in the Special Function Register TMOD (Figure 6). The timer/counter has four operating modes (Mode 0-3) selected by bit-pairs (M1, M0) in TMOD.

TMOD

Address: 89H
Reset State: XXXX 0000B

7							0
—	—	—	—	GATE	C/T#	M1	M0

Bit Number	Bit Mnemonic	Function
7-4	—	Reserved.
3	GATE	Timer 0 Gate: When GATE = 0, run control bit TR0 gates the input signal to the timer register. When GATE = 1 and TR0 = 1, external signal INT0# gates the timer input.
2	C/T#	Timer 0 Counter/Timer Select: C/T# = 0 selects timer operation: timer 0 counts the divided-down system clock. C/T# = 1 selects counter operation: timer 0 counts negative transitions on external pin T0.
1, 0	M1, M0	Timer 0 Mode Select: **M1 M0** 0 0 Mode 0: 8-bit timer/counter (TH0) with 5-bit prescaler (TL0) 0 1 Mode 1: 16-bit timer/counter 1 0 Mode 2: 8-bit auto-reload timer/counter (TL0). Reloaded from TH0 at overflow 1 1 Mode 3: TL0 is 8-bit timer/counter. TH0 is an 8-bit timer.

Figure 6. TMOD: Timer/Counter Mode Register

8.1 Mode 0

Timer 0 in Mode 0 is an 8-bit counter with a divide-by-32 prescaler. In this mode, the timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the timer interrupt flag TF0. The counted input is enabled to the timer when TR0 = 1 and either GATE = 0 or INT0# = 1. (Setting GATE = 1 allows the timer to be controlled by external input port 3.2 (see section 9.3 Timer Interrupts).

TR0 and TF0 are control bits in the TCON register (see Figure 7). The GATE bit is in the TMOD register (TMOD.3). The 13-bit register consists of all 8 bits of TH0 and the lower 5 bits of TL0. The upper 3 bits of TL0 are indeterminate and should be ignored. Setting the run flag (TR0) does not clear these registers.

8.2 Mode 1

Mode 1 is the same as Mode 0, except that the timer register uses all 16 bits. In this mode, TH0 and TL0 are cascaded without prescaler functionality.

8.3 Mode 2

Mode 2 configures the timer register as an 8-bit Counter (TL0) with automatic reload. Overflow from TL0 not only sets TF0, but also reloads TL0 with the contents of TH0, preset by software. The reload leaves TH0 unchanged.

8.4 Mode 3

Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. TL0 uses the Timer 0 control bits: C/T, GATE, TR0, INT0, and TF0. TH0 is locked into a timer function (counting machine cycles). Mode 3 is provided for applications requiring an extra 8-bit timer or counter. When enabled In mode 3 the application software sets the TR1 bit to operate the TH0 register. The TF1 flag is set by hardware when the TH0 register overflows. The TF1 flag is cleared by hardware during the vector to the service routine. TH0 can be halted at any time by using application software to clear the TR1 bit.

TCON Address: 88H
Reset State: 0000 0000B

7							0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Bit Number	Bit Mnemonic	Function
7	TF1	TH0 Overflow Flag (Mode 3 only) Set by hardware when TH0 overflows. Cleared by hardware when the processor vectors to the interrupt routine.
6	TR1	TH0 Run Control Bit (Mode 3 only) Set and cleared by software to switch TH0 on or off.
5	TF0	Timer 0 Overflow Flag: Set by hardware when TH0 overflows. Cleared by hardware when the processor vectors to the interrupt routine.
4	TR0	Timer 0 Run Control Bit: Set and cleared by software to turn timer 0 on or off.
3	IE1	Interrupt 1 Flag for INT1#: Set by hardware when an INT1# event is detected. Edge- or level-triggered (see IT1). Cleared by interrupt vector if edge-triggered.
2	IT1	Interrupt 1 Type Control Bit: Set this bit to select edge-triggered (high-to-low) for external interrupt 1. Clear this bit to select level-triggered (active-low).
1	IE0	Interrupt 1 Flag for INT0#: Set by hardware when an INT0# event is detected. Edge- or level-triggered (see IT0). Cleared by interrupt vector if edge-triggered.
0	IT0	Interrupt 0 Type Control Bit: Set this bit to select edge-triggered (high-to-low) for external interrupt 0. Clear this bit to select level-triggered (active-low).

Figure 7. TCON: Timer/Counter Control Register

9.0 INTERRUPT SYSTEM

The 83C51KB, like other control-oriented computer architectures, employs a program interrupt method. This operation branches to a subroutine and performs some service in response to the interrupt. When the subroutine completes, execution resumes at the point where the interrupt occurred. 83C51KB interrupts may occur as a result of internal 83C51KB activity (e.g., a timer overflow) or at the initiation of electrical signals external to the microcontroller (e.g. an external interrupt). In all cases, interrupt operation is programmed by the system designer, who determines the priority of interrupt service relative to normal code execution and other interrupt service routines. The interrupts are enabled or disabled by the system designer and may be manipulated dynamically.

Table 6. Interrupt Description of INT1:0

Signal Name	Type	Description	Alternate Function
INT1:0#	I	**External Interrupts 0 and 1**. These inputs set bits IE1:0 in the TCON register. If bits IT1:0 in the TCON register are set, bits IE1:0 are set by a falling edge on INT1#/INT0#. If bits INT1:0 are clear, bits IE1:0 are set by a low level on INT1:0#. For keyboard applications, these signals are normally used for the CLK signals. (See KSIINT and CDPU bits in the PCON register)	CLK1:0 P3.3:2

9.1 Interrupt Sources

The 83C51KB has four maskable interrupt sources; the maskable sources include two external interrupts (INT0# and INT1#) and two timer interrupts associated with timer 0 operation. Each interrupt has an interrupt request flag, set by software as well as by hardware. For some interrupts, hardware clears the request flag when the CPU grants service to an interrupt. Software can clear any request flag to cancel a pending interrupt.

9.2 External Interrupts

External interrupts INT0# and INT1# (INTx#) pins may each be programmed to be level-triggered or edge-triggered, dependent upon bits IT0 and IT1 in the TCON register (see Figure 7). If ITx = 0, INTx# is triggered by a detected low at the pin. If ITx = 1, INTx# is negative-edge triggered.

External interrupts are enabled with bits EX0 and EX1 in the IE register (see Figure 8). Events on the external interrupt pins set the interrupt request flags IEx in TCON. These request bits are cleared by hardware vectors to service routines only if the interrupt is negative-edge triggered. If the interrupt is level-triggered, the interrupt source controls the interrrupt flag. The source must hold the request active until acknowledged in some manner by the ISR. After acknowledgment, the source must deassert INTx# before the service routine completes, or an additional interrupt is requested. External interrupt pins are sampled once every machine cycle. A level-triggered interrupt pin held low or high for at least a six-state time period guarantees detection. Edge-triggered external interrupts must hold the request pin high for at least 6 state times and low for at least six state times. This ensures edge recognition and sets interrupt request flag.

9.3 Timer Interrupts

Timer interrupts are enabled by ET0 in the IE register (see Figure 8). The timer-interrupt request flag TF0 is set in the TCON register by the timer 0 overflow signal (see Figure 7). The exception is Mode 3 where the interrupt is instead enabled by ET1 and the associated overflow sets the TF1 flag in TCON. When a timer interrupt is generated, the flag is cleared by an on-chip-hardware vector to an interrupt service routine.

IE

Address: A8H
Reset State: 0XXX 0000B

7							0
EA	—	—	—	ET1	EX1	ET0	EXO

Bit Number	Bit Mnemonic	Function
7	EA	Global Interrupt Enable: Setting this bit enables all interrupts enabled by bits 0-2 in this register.
6:4	—	Reserved
3	ET1	TH0 Overflow Interrupt Enable (Mode 3 only).
2	EX1	External Interrupt 1 Enable: Setting this bit enables external interrupt 1.
1	ET0	Timer 0 Overflow Interrupt Enable: Setting this bit enables the timer 0 overflow interrupt.
0	EX0	External Interrupt 0 Enable: Setting this bit enables external interrupt 0.

Figure 8. Interrupt Enable Register

IP

Address: B8H
Reset State: XXXX 0000B

7							0
—	—	—	—	PT1	PX1	PT0	PX0

Bit Number	Bit Mnemonic	Function
7:4	—	Reserved. The value read from this bit is indeterminate. Do not write a “1” to this bit.
3	PT1	TH0 Overflow Interrupt Priority Bit (Mode 3 only)
2	PX1	External Interrupt 1 Priority Bit
1	PT0	Timer 0 Overflow Interrupt Priority Bit
0	PX0	External Interrupt 0 Priority Bit Low

Figure 9. Interrupt Priority Register

9.4 Interrupt Enable

Each interrupt source is individually enabled or disabled with the appropriate interrupt enable bit in the IE register at A8H (see Figure 8). Note IE also contains a global disable bit (EA). If EA is set, interrupts are individually enabled or disabled by other bits in IE. If EA is clear, all interrupts are disabled.

9.5 Interrupt Priorities

Each of the 83C51KB interrupt sources may be individually programmed to one of four priority levels. This is accomplished with the IP.x and IPH.x bits in the interrupt priority (IP and IPH) registers (Figure 9).

Specify the priority level as shown in Table 8.A low-priority interrupt is always interrupted by a higher priority interrupt but not by another interrupt of equal or lower priority. The highest priority interrupt is not interrupted by any other interrupt source.

Higher priority interrupts are serviced before lower priority interrupts. The response to simultaneous occurrence of equal priority interrupts (i.e., sampled within the same interrupt request cycle) is determined by a hardware priority-within-level resolver (see Table 7).

Table 7. Interrupt Priority Within Level

Priority Number	Interrupt Name
1(Highest Priority)	INT0#
2	Timer 0
3	INT1#
4	TH0 (Mode 3 only)

Table 8. Level of Priority

IP Value	IPH Value	Priority Level
0	0	Level 0 (Low Priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (High Priority)

IPH Address: B7H
Reset State: XXXX 0000B

7							0
—	—	—	—	PT1H	PX1H	PT0H	PX0H

Bit Number	Bit Mnemonic	Function
7:4	—	Reserved
3	PT1H	TH0 Interrupt Priority high bit (Mode 3 only)
2	PX1H	INT1# Priority high bit
1	PT0H	Timer 0 Interrupt Priority high bit
0	PX0H	INT0# Priority high bit

Table 9. Interrupt Priority High Register

9.6 Interrupt Processing

The interrupt flags are sampled at S5P2 of every machine cycle. The samples are polled during the following machine cycle. If one of the flags was in a set condition at S5P2 of the preceding cycle, the polling cycle will find it and the interrupt system will generate an LCALL to the appropriate service routine, provided this hardware-generated LCALL is not blocked by any of the following conditions:

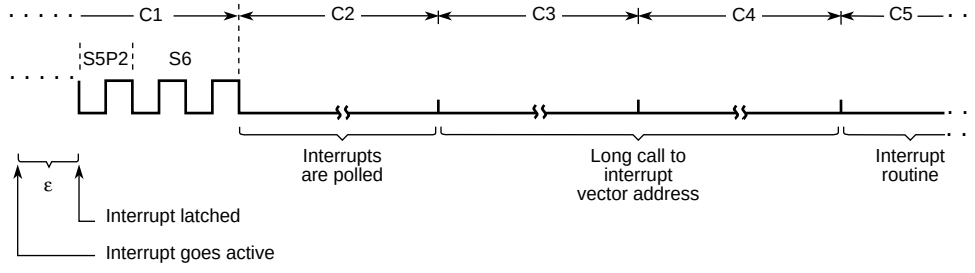
1. An interrupt of equal or higher priority level is already in progress.

2. The current (polling) cycle is not the final cycle in the execution of the instruction in progress.

3. The instruction in progress is RETI or any write to the IE or IP registers.

Any of these three conditions will block the generation of the LCALL to the interrupt service routine. Condition 2 ensures that the instruction in progress will be completed before vectoring to any service routine. Condition 3 ensures that if the instruction in progress is RETI or any write to IE or IP, then at least one more instruction will be executed before any interrupt is vectored to. The polling cycle is repeated with each machine cycle, and the values polled are the values that were present at S5P2 of the previous machine cycle. If the interrupt flag for a level-sensitive external interrupt is active but not being responded to for one of the above conditions and is not still active when the blocking condition is removed, the denied interrupt will not be serviced. In other words, the fact that the interrupt flag was once active but not serviced is not remembered. Every polling cycle is new.

The interrupt vector cycle/LCALL sequence is illustrated in Figure .



This is the fastest possible response when C2 is the final cycle of an instruction other than RETI or an access to IE or IP.

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Interrupt Vector to LCALL

NOTE

Note that if an interrupt of a higher priority level goes active prior to S5P2 of the first machine cycle labeled C3 in Figure , then in accordance with the above rules it will be vectored to during C5 and C6, without any instruction of the lower priority routine having been executed.

9.7 Interrupt Service Routine Cycle

When interrupt service is granted, the CPU breaks the instruction stream sequence and pushes program counter (PC) information onto the stack. The CPU then reloads the PC with a start address for the appropriate ISR.

The starting addresses of consecutive interrupt service routines are only 8 bytes apart. That means if consecutive interrupts are being used (IE0 and TF0, for example, or TF0 and IE1), and if the first interrupt routine is more than 7 bytes long, then that routine will have to execute a jump to some other memory location where the service routine can be completed without overlapping the starting address of the next interrupt routine.

The ISR executes until the RETI instruction is encountered. RETI informs the processor that the ISR is no longer in progress. Two bytes are popped from the stack and reloaded into the PC. Execution of the interrupted program continues from where it left off.

Table 10. Interrupt Vector Addresses

Interrupt Source	TCON Request Flag	Hardware Clear	Vector Address
INT0#	IE0	No (level) Yes (edge)	0003H
Timer 0	TF0	Yes	000BH
INT1#	IE1	No (level) Yes (edge)	0013H
TH0 Overflow (Mode 3 only)	TF1	Yes	001BH

9.8 Response Time

The INT0 and INT1 levels are inverted and latched into the Interrupt Flags IE0 and IE1 at S5P2 of every machine cycle. The values are not actually polled by the circuitry until the next machine cycle.

If a request is active and conditions are right for it to be acknowledged, a hardware subroutine call to the requested service routine will be the next instruction to be executed. The call itself takes two cycles. Thus, a minimum of three complete machine cycles elapses between activation of an external interrupt request and the beginning of execution of the service routine's first instruction. Figure illustrates interrupt response timing.

A longer response time would result if the request is blocked by one of the 3 previously listed conditions. If an interrupt of equal or higher priority level is already in progress, the additional wait time obviously depends on the nature of the other interrupt's service routine. If the instruction in progress is not in its final cycle, the additional wait time cannot be more than 3 cycles, since the longest instructions (MUL and DIV) are only 4 cycles long, and if the instruction in progress is RETI or write to IE or IP, the additional wait time cannot be more than 5 cycles (a maximum of one or more cycle to complete the instruction in progress, plus 4 cycles to complete the next instruction if the instruction is MUL or DIV).

Thus, in a single-interrupt system, the response time is always more than 3 cycles and less than 9 cycles.

10.0 ONCE MODE

The ONCE (ON-Circuit Emulation) mode facilitates testing and debugging of systems using the 83C51KB without having to remove the device from the circuit.

The ONCE mode is invoked by:

1. 1. Pulling ALE low while the device is in reset and PSEN is high;
2. 2. Holding ALE low as RST is deactivated.

While the device is in ONCE mode, the port pins, ALE, and PSEN are weakly pulled high. The oscillator circuit remains active. While the device is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored after a valid reset is applied.

11.0 ADDITIONAL REFERENCES

The following application notes provide supplemental information to this document and can be found in the two volumes of the Embedded Applications handbook (order number 270648).

1. AP-125 "Designing Microcontroller Systems for Electrically Noisy Environments"
2. AP-155 "Oscillators for Microcontrollers"
3. AP-252 "Designing with the 80C51BH"