



74VHCT238A

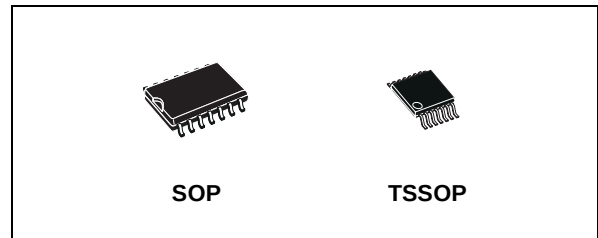
3 TO 8 LINE DECODER

- HIGH SPEED: $t_{PD} = 5.5 \text{ ns}$ (TYP.) at $V_{CC} = 5V$
- LOW POWER DISSIPATION:
 $I_{CC} = 4 \mu A$ (MAX.) at $T_A = 25^\circ C$
- COMPATIBLE WITH TTL OUTPUTS:
 $V_{IH} = 2V$ (MIN.), $V_{IL} = 0.8V$ (MAX)
- POWER DOWN PROTECTION ON INPUTS & OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 8 \text{ mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \approx t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC(OPER)} = 4.5V \text{ to } 5.5V$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 238
- IMPROVED LATCH-UP IMMUNITY

DESCRIPTION

The 74VHCT238A is an advanced high-speed CMOS 3 TO 8 LINE DECODER fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology.

When the device is enabled, 3 binary select inputs (A, B, and C) determine which one of the outputs will go high. If enable input G1 is held low or either G2A or G2B is held high, decoding function is inhibited and all the 8 outputs go to low.



ORDER CODES

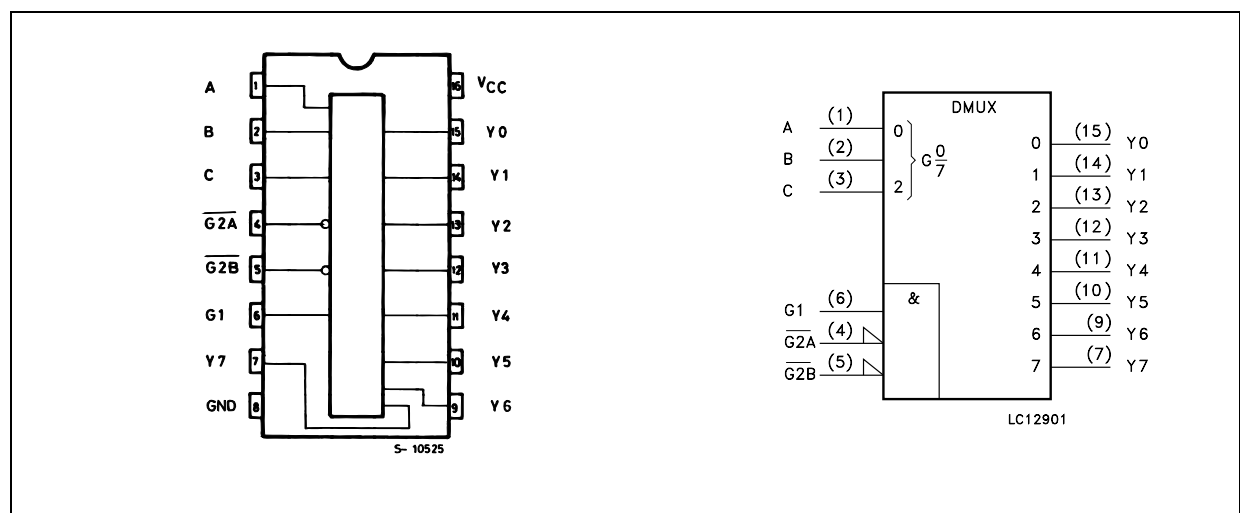
PACKAGE	TUBE	T & R
SOP	74VHCT238AM	74VHCT238AMTR
TSSOP		74VHCT238ATTR

The three enable inputs are provided to ease cascade connection and application of address decoders for memory systems.

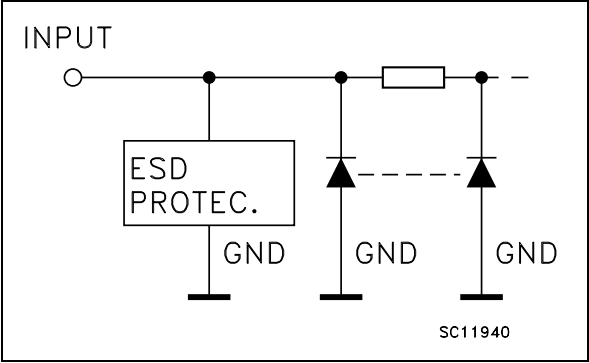
Power down protection is provided on all inputs and outputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V since all inputs are equipped with TTL threshold.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

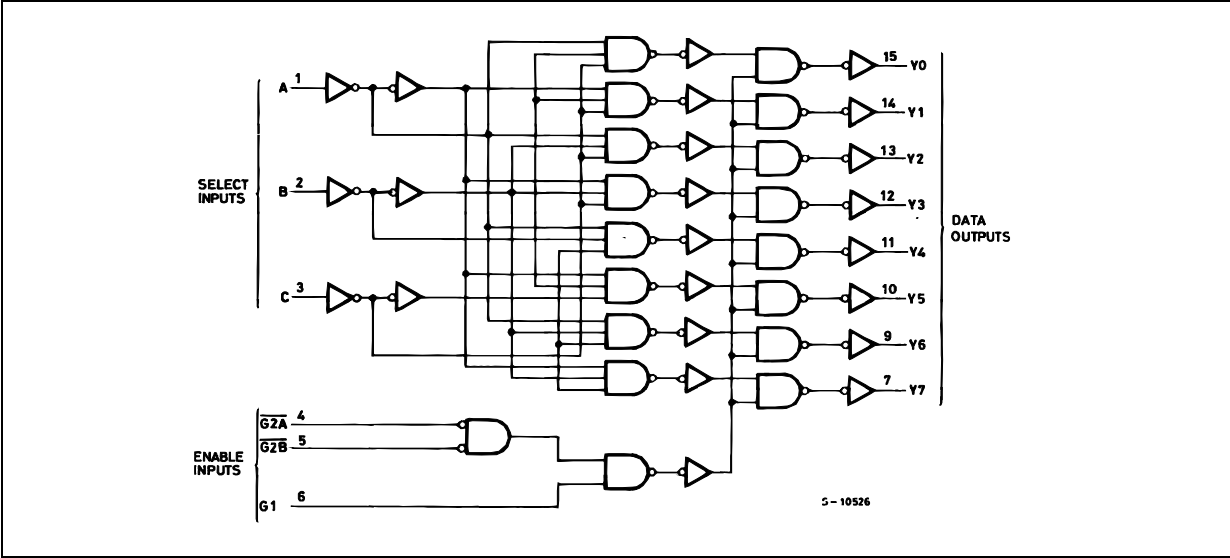
PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3	A, B, C	Address Inputs
4, 5	G2A, G2B	Enable Inputs
6	G1	Enable Input
15, 14, 13, 12, 11, 10, 9, 7	Y0 to Y7	Outputs
8	GND	Ground (0V)
16	V _{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
G2B	G2A	G1	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	L	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
H	X	X	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	L	L	H	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	L	H	H	L	L	L	H	L	L	L	L
L	L	H	H	L	L	L	L	L	L	H	L	L	L
L	L	H	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H

X : Don't Care

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage (see note 1)	-0.5 to +7.0	V
V_O	DC Output Voltage (see note 2)	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	- 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

1) $V_{CC} = 0V$

2) High or Low State

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage (see note 1)	0 to 5.5	V
V_O	Output Voltage (see note 2)	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (see note 3) ($V_{CC} = 5.0 \pm 0.5V$)	0 to 20	ns/V

1) $V_{CC} = 0V$

2) High or Low State

3) V_{IN} from 0.8V to 2V

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value							Unit
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V _{IH}	High Level Input Voltage	4.5 to 5.5		2			2		2		V
V _{IL}	Low Level Input Voltage	4.5 to 5.5				0.8		0.8		0.8	V
V _{OH}	High Level Output Voltage	4.5	I _O =-50 μA	4.4	4.5		4.4		4.4		V
		4.5	I _O =-8 mA	3.94			3.8		3.7		
V _{OL}	Low Level Output Voltage	4.5	I _O =50 μA		0.0	0.1		0.1		0.1	V
		4.5	I _O =8 mA			0.36		0.44		0.55	
I _I	Input Leakage Current	0 to 5.5	V _I = 5.5V or GND			± 0.1		± 1.0		± 1.0	μA
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			4		40		40	μA
ΔI _{CC}	Additional Worst Case Supply Current	5.5	One Input at 3.4V, other input at V _{CC} or GND			1.35		1.5		1.5	mA
I _{OPD}	Output Leakage Current	0	V _{OUT} = 5.5V			0.5		5.0		5.0	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3ns)

Symbol	Parameter	Test Condition			Value						Unit	
		V _{CC} (*) (V)	C _L (pF)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{PLH}	Propagation Delay	5.0	15			5.5	8.1	1.0	9.5	1.0	9.5	ns
t _{PHL}	Time A,B,C to Y	5.0	50			7.0	10.1	1.0	11.5	1.0	11.5	
t _{PLH}	Propagation Delay	5.0	15			5.4	8.1	1.0	9.5	1.0	9.5	ns
t _{PHL}	Time G1 to Y	5.0	50			6.9	10.1	1.0	11.5	1.0	11.5	
t _{PLH}	Propagation Delay	5.0	15			5.7	8.1	1.0	9.5	1.0	9.5	ns
t _{PHL}	Time <u> </u> G2A, G2B to Y	5.0	50			7.2	10.1	1.0	11.5	1.0	11.5	

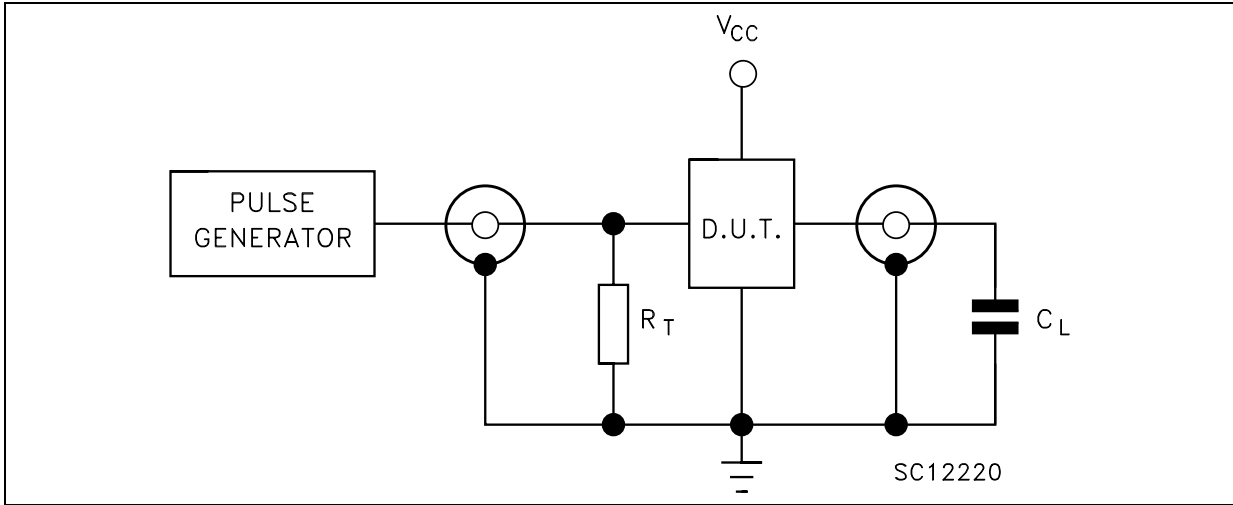
(*) Voltage range is 5.0V ± 0.5V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition	Value								Unit
			T _A = 25°C			-40 to 85°C		-55 to 125°C			
			Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
C _{IN}	Input Capacitance			6	10		10		10	pF	
C _{PD}	Power Dissipation Capacitance (note 1)			37						pF	

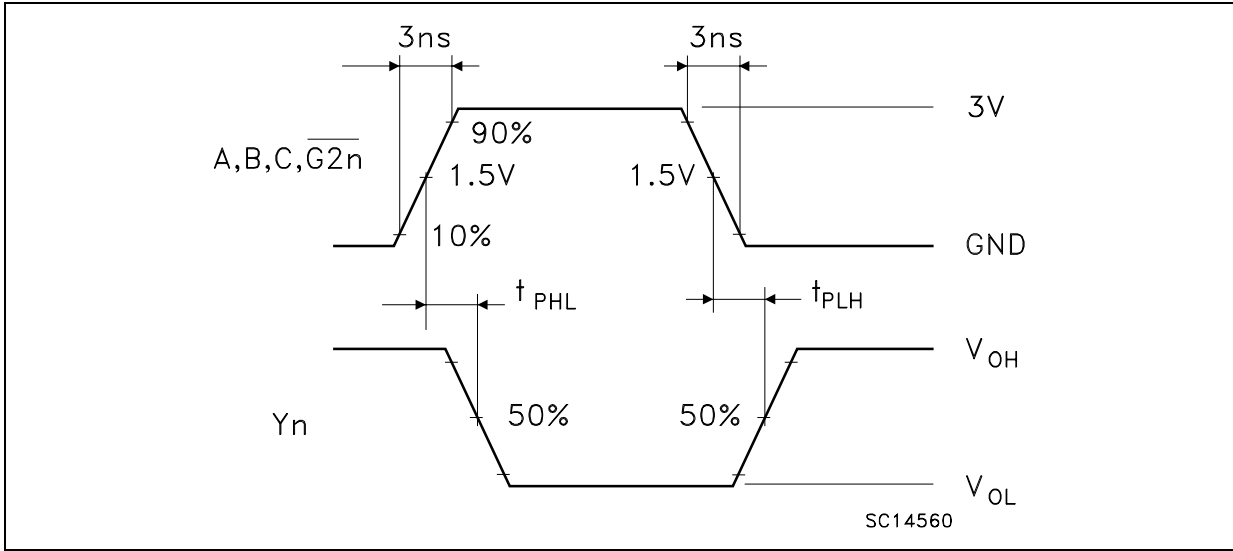
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I_{CC(opr)} = C_{PD} × V_{CC} × f_{IN} + I_{CC}

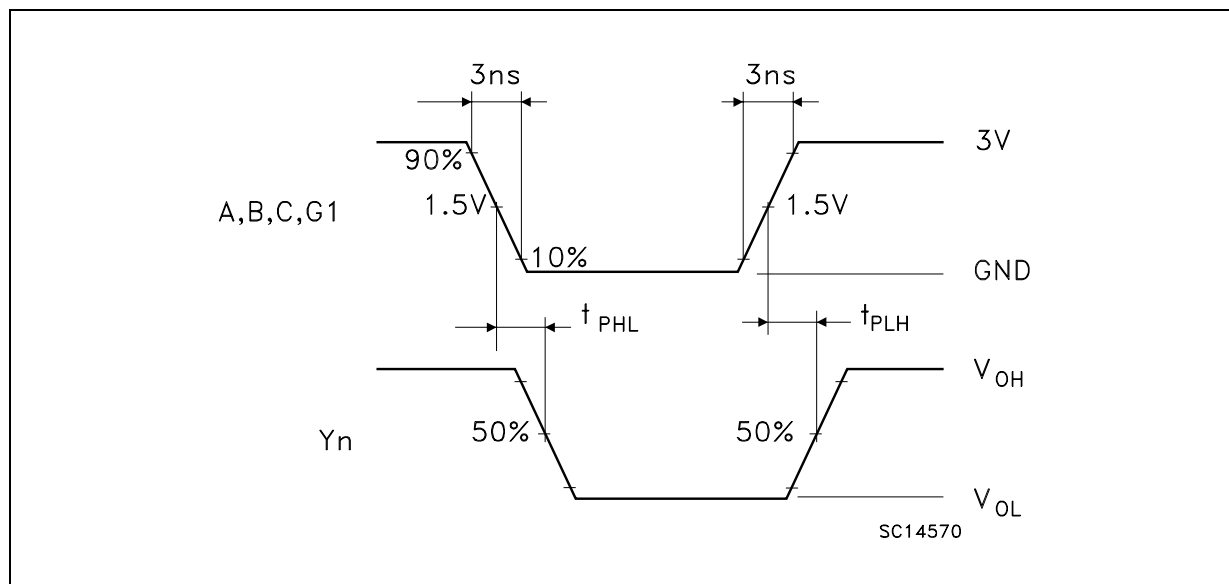
TEST CIRCUIT



$C_L = 15/50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

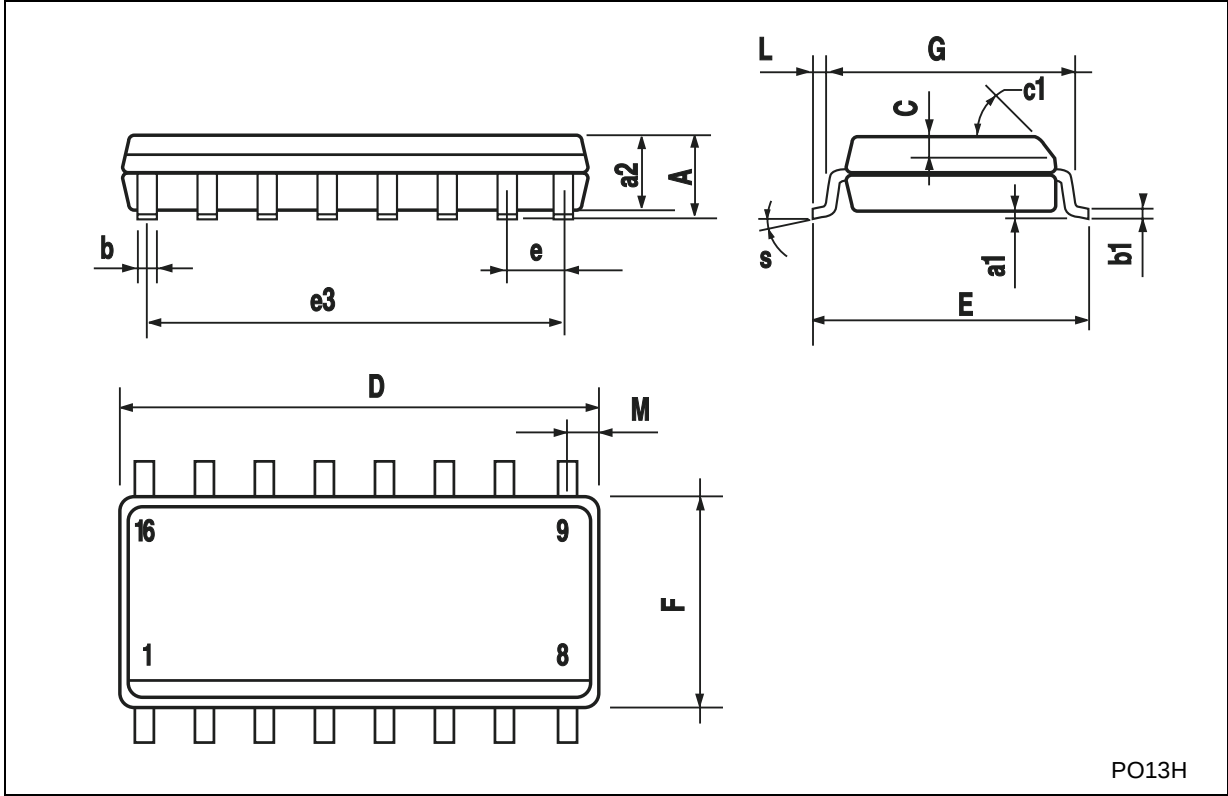
WAVEFORM 1: PROPAGATION DELAYS FOR INVERTING OUTPUTS ($f=1\text{MHz}$; 50% duty cycle)



WAVEFORM 2: PROPAGATION DELAYS FOR NON-INVERTING OUTPUTS ($f=1\text{MHz}$; 50% duty cycle)

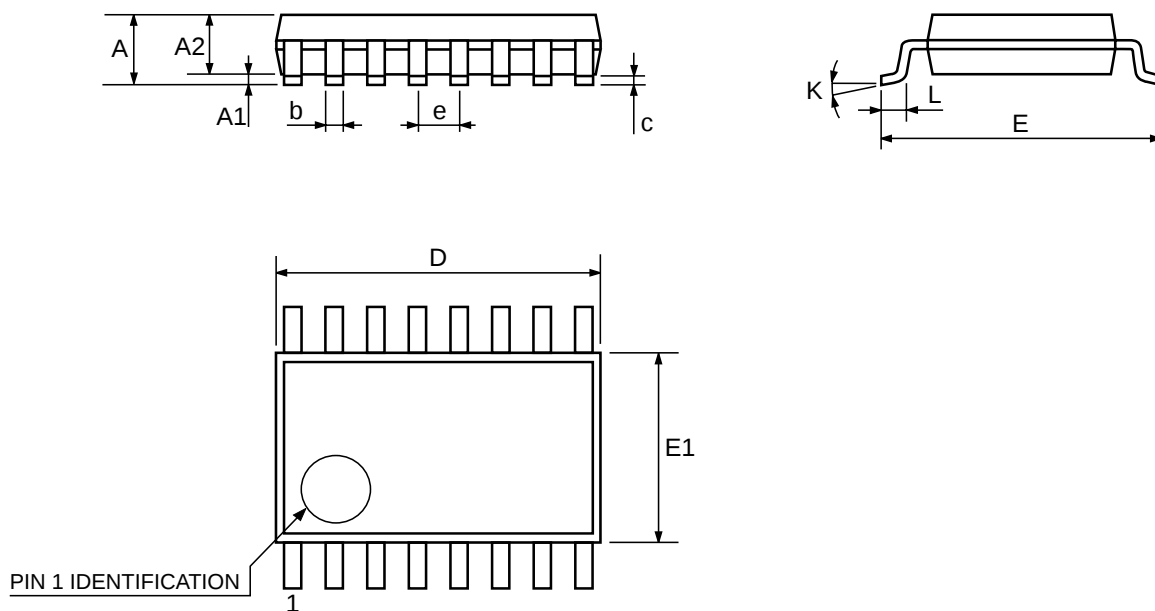
SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



0080338D

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2001 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom

© <http://www.st.com>

