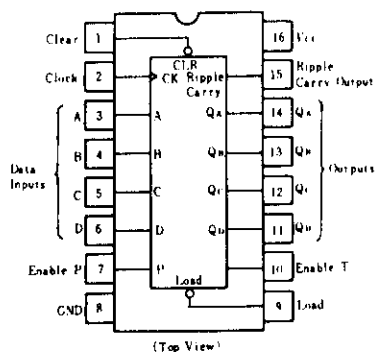


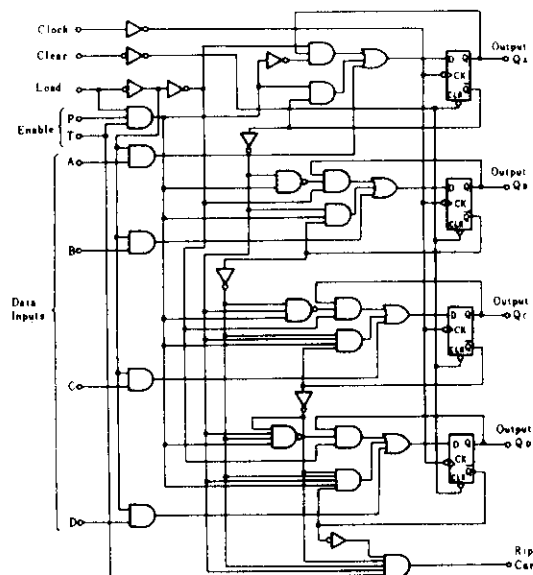
This synchronous 4-bit binary counter features an internal carry look-ahead for application in high speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs changes coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input should be avoided when the clock is low if the enable inputs are high at or before the transition. The clear function is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs. The carry look-ahead circuitry provides for cascading counters for n -bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low level transitions at the enable P or T inputs should occur only when the clock input is high.

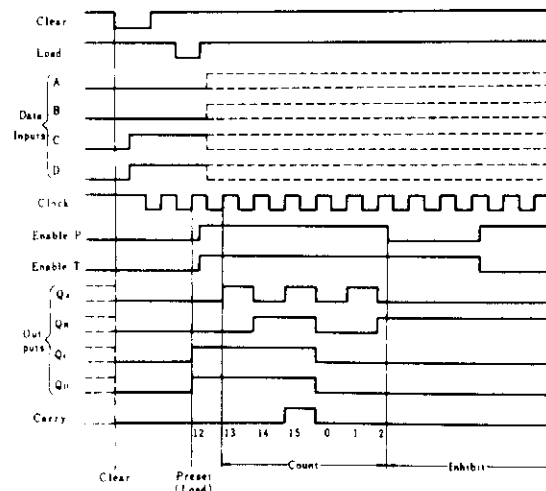
PIN ARRANGEMENT



BLOCK DIAGRAM



TYPICAL CLEAR, PRESET, AND INHIBIT SEQUENCE



RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Clock frequency	f_{clock}	0	—	25	MHz
Clock pulse width	$t_w(CK)$	25	—	—	ns
Clear pulse width	$t_w(CLR)$	20	—	—	ns
Setup time	A, B, C, D	20	—	—	ns
	Enable P, T	20	—	—	
	Load	20	—	—	
Hold time	t_h	3	—	—	ns

ELECTRICAL CHARACTERISTICS (Ta = -20 ~ +75°C)

Item		Symbol	Test Conditions	min	typ*	max	Unit
Input voltage		V _{IH}		2.0	—	—	V
		V _{IL}		—	—	0.8	V
Output voltage		V _{OH}	V _{CC} =4.75V, V _{IH} =2V, V _{IL} =0.8V, I _{OH} =-400μA	2.7	—	—	V
		V _{OL}	V _{CC} =4.75V, V _{IH} =2V, I _{OL} =4mA	—	—	0.4	V
			V _{IL} =0.8V, I _{OL} =8mA	—	—	0.5	
Input current	Data, Enable P	I _{IH}	V _{CC} =5.25V, V _I =2.7V	—	—	20	μA
	Load, Clock, Enable T			—	—	40	
	Clear			—	—	20	
	Data, Enable P	I _{IL}	V _{CC} =5.25V, V _I =0.4V	—	—	-0.4	mA
	Load, Clock, Enable T			—	—	-0.8	
	Clear			—	—	-0.4	
	Data, Enable P	I _I	V _{CC} =5.25V, V _I =7V	—	—	0.1	mA
	Load, Clock, Enable T			—	—	0.2	
	Clear			—	—	0.1	
Short-circuit output current		I _{OS}	V _{CC} =5.25V	-20	—	-100	mA
Supply current**		I _{CCH}	V _{CC} =5.25V	—	18	31	mA
		I _{CCL}	V _{CC} =5.25V	—	19	32	mA
Input clamp voltage		V _{IK}	V _{CC} =4.75V, I _{IN} =-18mA	—	—	-1.5	V

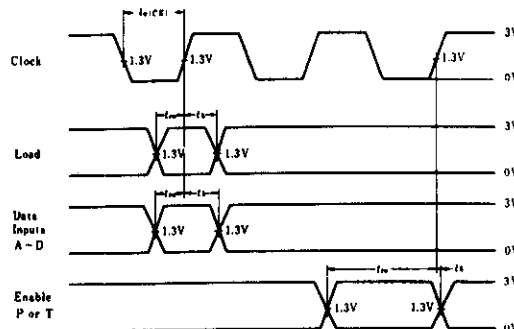
* V_{CC}=5V, Ta=25°C

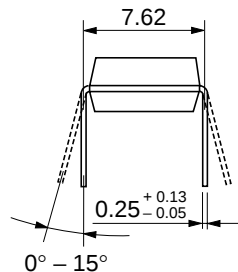
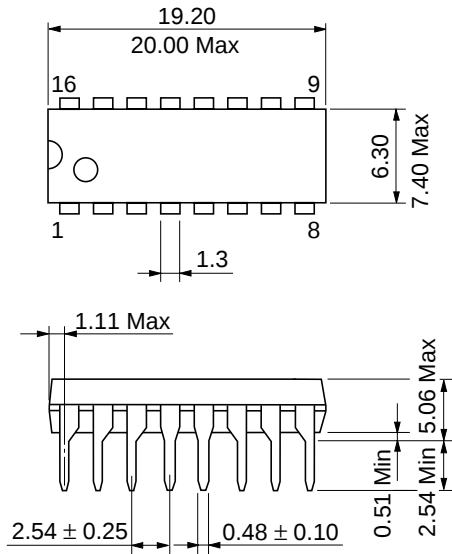
** I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C)

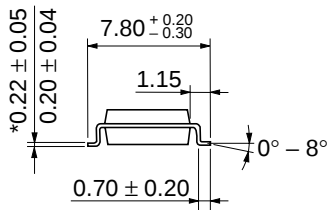
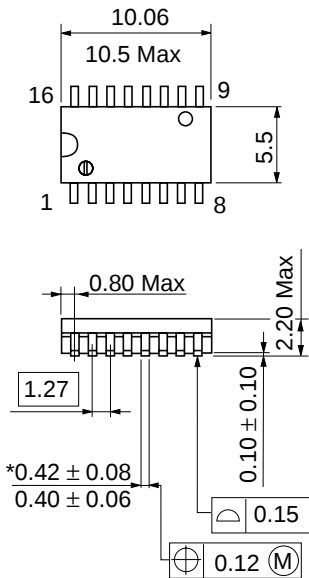
Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}	Clock	$Q_A \sim Q_D$	$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$	25	32	—	MHz
Propagation delay time	t_{PLH}	Clock	Ripple		—	20	35	ns
	t_{PHL}		Carry		—	18	35	ns
	t_{PLH}	Clock (Load=H ⁺)	$Q_A \sim Q_D$		—	13	24	ns
	t_{PHL}				—	18	27	ns
	t_{PLH}	Clock (Load=L ⁺)	$Q_A \sim Q_D$		—	13	24	ns
	t_{PHL}				—	18	27	ns
	t_{PLH}	Enable T	Ripple		—	9	14	ns
	t_{PHL}		Carry		—	9	14	ns
	t_{PHL}	Clear	$Q_A \sim Q_D$		—	20	28	ns

TIMING DEFINITION



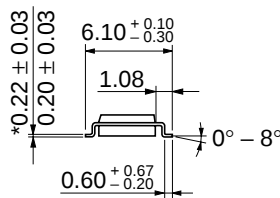
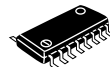


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL	NorthAmerica	:	http://semiconductor.hitachi.com/
	Europe	:	http://www.hitachi-eu.com/hel/ecg
	Asia (Singapore)	:	http://www.has.hitachi.com.sg/grp3/sicd/index.htm
	Asia (Taiwan)	:	http://www.hitachi.com.tw/E/Product/SICD_Frame.htm
	Asia (HongKong)	:	http://www.hitachi.com.hk/eng/bo/grp3/index.htm
	Japan	:	http://www.hitachi.co.jp/Sicd/indx.htm

For further information write to:

Hitachi Semiconductor (America) Inc. 179 East Tasman Drive, San Jose, CA 95134 Tel: <1> (408) 433-1990 Fax: <1> (408) 433-0223	Hitachi Europe GmbH Electronic components Group Dornacher Straße 3 D-85622 Feldkirchen, Munich Germany Tel: <49> (89) 9 9180-0 Fax: <49> (89) 9 29 30 00 Hitachi Europe Ltd. Electronic Components Group. Whitebrook Park Lower Cookham Road Maidenhead Berkshire SL6 8YA, United Kingdom Tel: <44> (1628) 585000 Fax: <44> (1628) 778322
--	---

Hitachi Asia Pte. Ltd. 16 Collyer Quay #20-00 Hitachi Tower Singapore 049318 Tel: 535-2100 Fax: 535-1533 Hitachi Asia Ltd. Taipei Branch Office 3F, Hung Kuo Building, No.167, Tun-Hwa North Road, Taipei (105) Tel: <886> (2) 2718-3666 Fax: <886> (2) 2718-8180
--

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

Copyright ' Hitachi, Ltd., 1999. All rights reserved. Printed in Japan.