



74ALVCH162374

LOW VOLTAGE CMOS 16-BIT D-TYPE FLIP-FLOP (3-STATE) WITH 3.6V TOLERANT INPUTS AND OUTPUTS

PRELIMINARY DATA

- 3.6V TOLERANT INPUTS AND OUTPUTS
- HIGH SPEED :
 - $t_{PD} = 4.6 \text{ ns (MAX.) at } V_{CC} = 3.0 \text{ to } 3.6\text{V}$
 - $t_{PD} = 5.4 \text{ ns (MAX.) at } V_{CC} = 2.3 \text{ to } 2.7\text{V}$
 - $t_{PD} = 6.5 \text{ ns (MAX.) at } V_{CC} = 1.65\text{V}$
- POWER DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 - $|I_{OH}| = I_{OL} = 24\text{mA (MIN) at } V_{CC} = 3.0\text{V}$
 - $|I_{OH}| = I_{OL} = 18\text{mA (MIN) at } V_{CC} = 2.3\text{V}$
 - $|I_{OH}| = I_{OL} = 4\text{mA (MIN) at } V_{CC} = 1.65\text{V}$
- BUS HOLD PROVIDED ON DATA INPUTS
- 26Ω SERIE RESISTORS IN OUTPUTS
- OPERATING VOLTAGE RANGE:
 - $V_{CC(OPR)} = 1.65\text{V to } 3.6\text{V}$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 16374
- LATCH-UP PERFORMANCE EXCEEDS 300mA (JESD 17)
- ESD PERFORMANCE:
 - HBM > 2000V (MIL STD 883 method 3015);
 - MM > 200V

DESCRIPTION

The 74ALVCH162374 is a low voltage CMOS 16 BIT D-TYPE LATCH with 3 STATE OUTPUTS NON INVERTING fabricated with sub-micron silicon gate and five-layer metal wiring C²MOS technology. It is ideal for low power and very high speed 1.65 to 3.6V applications; it can be interfaced to 3.6V signal environment for both inputs and outputs.

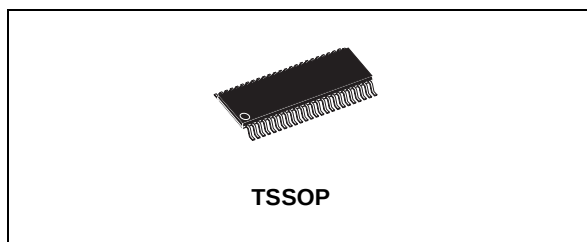
These flip-flops are controlled by two clock inputs (nCK) and two output enable inputs (nOE).

On the positive transition of the (nCK), the nQ outputs will be set to the logic state that were setup at the nD inputs.

While the (nOE) input is low, the outputs (nQ) will be in a normal state (HIGH or LOW logic level) and while high level the outputs will be in a high impedance state.

Any output control does not affect the internal operation of flip flops; that is, the old data can be retained or the new data can be entered even while the outputs are off. The device circuits is including 26Ω series resistance in the outputs. These resistors permit to reduce line noise in high speed applications.

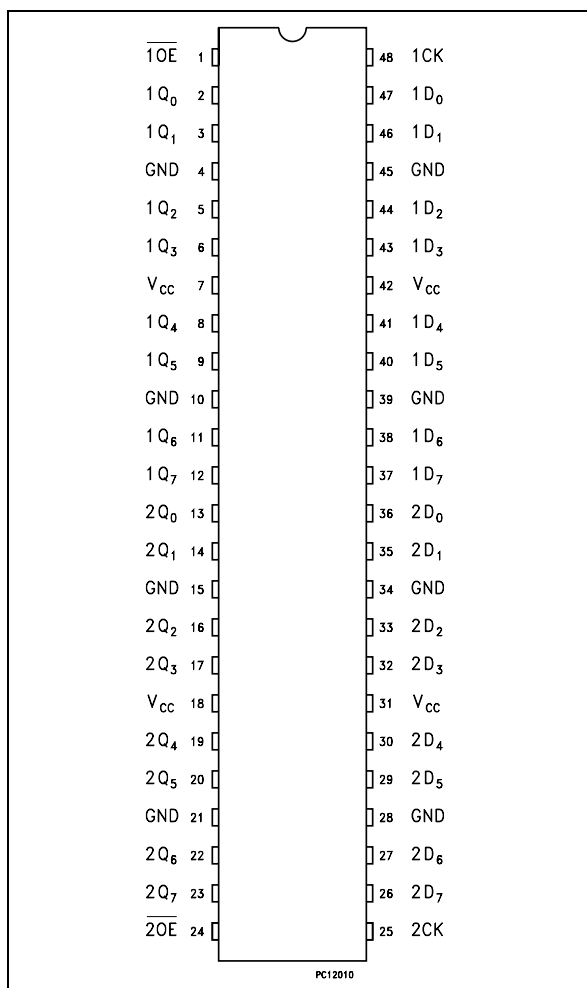
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.



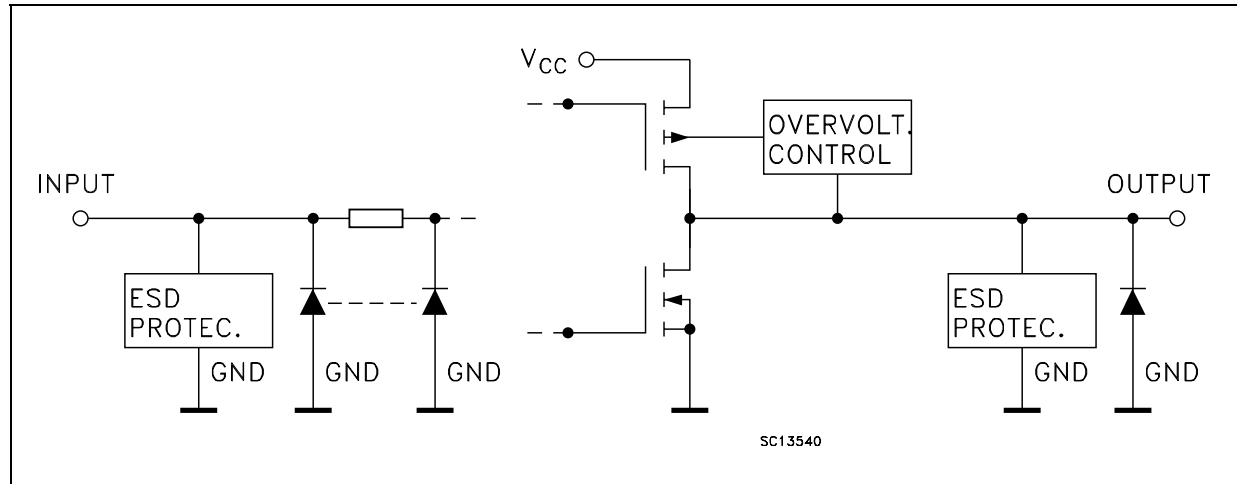
ORDER CODES

PACKAGE	TUBE	T & R
TSSOP		74ALVCH162374T

PIN CONNECTION



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	1OE	3 State Output Enable Input (Active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q0 to 1Q7	3-State Outputs
13, 14, 16, 17, 19, 20, 22, 23	2Q0 to 2Q7	3-State Outputs
24	2OE	3 State Output Enable Input (Active LOW)
25	2CK	Clock Input
36, 35, 33, 32, 30, 29, 27, 26	2D0 to 2D7	Data Inputs
47, 46, 44, 43, 41, 40, 38, 37	1D0 to 1D7	Data Inputs
48	1CK	Clock Input
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V _{CC}	Positive Supply Voltage

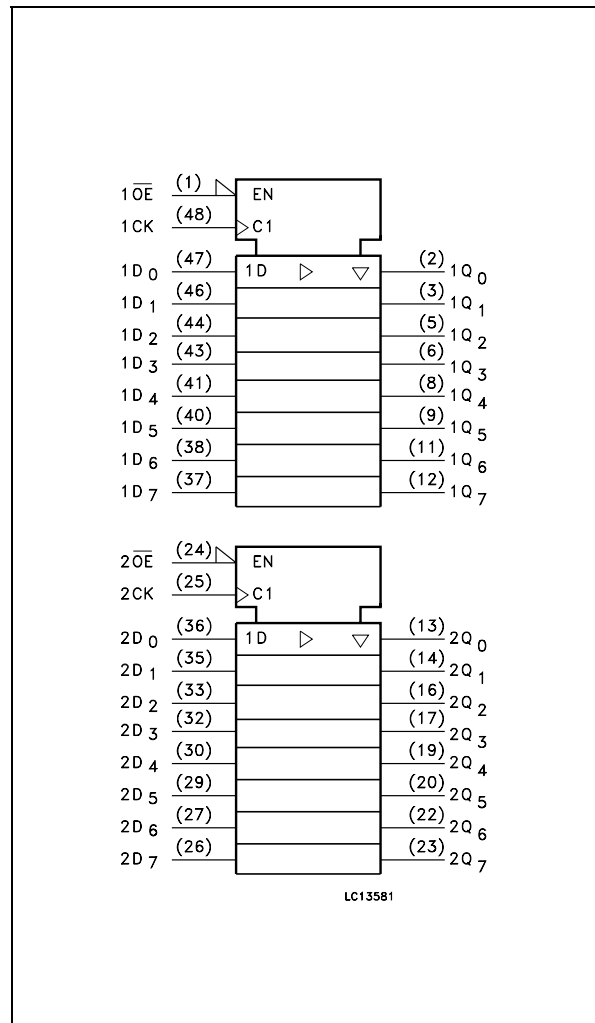
TRUTH TABLE

INPUTS			OUTPUT
OE	CK	D	Q
H	X	X	Z
L		X	NO CHANGE
L		L	L
L		H	H

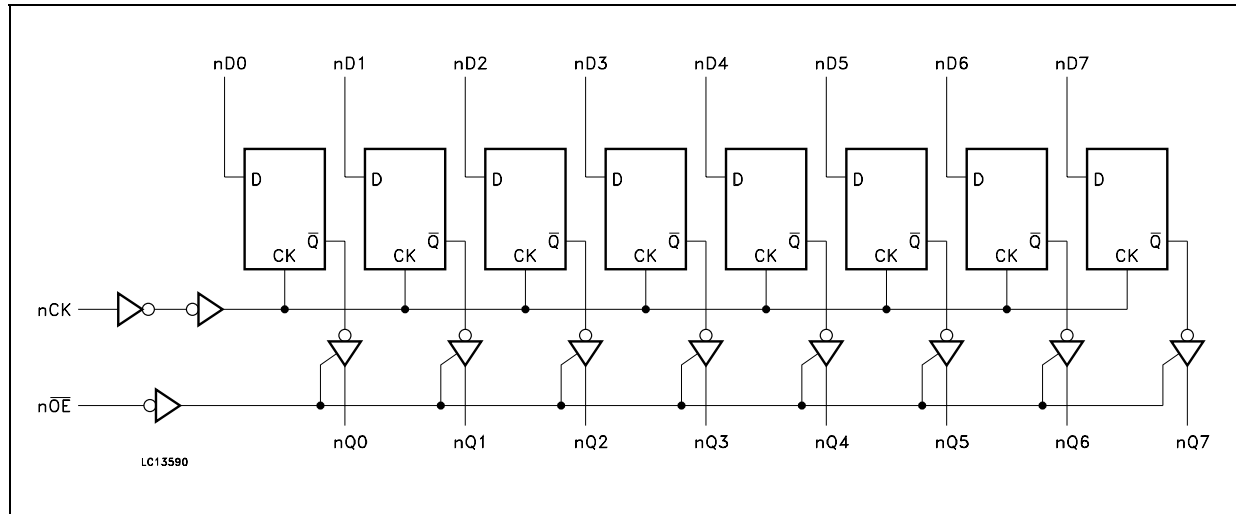
X : Don't Care

Z : High Impedance

IEC LOGIC SYMBOLS



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +4.6	V
V_I	DC Input Voltage	-0.5 to +4.6	V
V_O	DC Output Voltage (OFF State)	-0.5 to +4.6	V
V_O	DC Output Voltage (High or Low State) (note 1)	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	- 50	mA
I_{OK}	DC Output Diode Current (note 2)	- 50	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Supply Pin	± 100	mA
P_D	Power Dissipation	400	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

1) I_O absolute maximum rating must be observed

2) $V_O < GND$, $V_O > V_{CC}$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	1.65 to 3.6	V
V_I	Input Voltage	-0.3 to 3.6	V
V_O	Output Voltage (OFF State)	0 to 3.6	V
V_O	Output Voltage (High or Low State)	0 to V_{CC}	V
I_{OH} , I_{OL}	High or Low Level Output Current ($V_{CC} = 3.0$ to $3.6V$)	± 12	mA
I_{OH} , I_{OL}	High or Low Level Output Current ($V_{CC} = 2.3$ to $2.7V$)	± 6	mA
I_{OH} , I_{OL}	High or Low Level Output Current ($V_{CC} = 1.65V$)	± 2	mA
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (note 1)	0 to 10	ns/V

1) V_{IN} from 0.8V to 2V at $V_{CC} = 3.0V$

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value				Unit
		V _{CC} (V)		-40 to 85 °C		-55 to 125 °C		
				Min.	Max.	Min.	Max.	
V _{IH}	High Level Input Voltage	1.65 to 1.95		0.65 V _{CC}		0.65 V _{CC}		V
		2.3 to 2.7		1.7		1.7		
		2.7 to 3.6		2.0		2.0		
V _{IL}	Low Level Input Voltage	1.65 to 1.95			0.35 V _{CC}		0.35 V _{CC}	
		2.3 to 2.7			0.7		0.7	
		2.7 to 3.6			0.8		0.8	
V _{OH}	High Level Output Voltage	1.65 to 3.6	I _O =-100 μA	V _{CC} -0.2		V _{CC} -0.2		V
		1.65	I _O =-2 mA	1.2		1.2		
		2.3	I _O =-4 mA	2.0		2.0		
		2.3	I _O =-6 mA	1.7		1.7		
		2.7	I _O =-8 mA	2.2		2.2		
		3.0	I _O =-6 mA	2.4		2.4		
		3.0	I _O =-12 mA	2.0		2.0		
V _{OL}	Low Level Output Voltage	1.65 to 3.6	I _O =100 μA		0.2		0.2	V
		1.65	I _O =2 mA		0.45		0.45	
		2.3	I _O =4 mA		0.4		0.4	
		2.3	I _O =6 mA		0.55		0.55	
		2.7	I _O =8 mA		0.6		0.6	
		3.0	I _O =12 mA		0.8		0.8	
I _I	Input Leakage Current	3.6	V _I = 0 or 3.6V		± 5		± 5	μA
I _{IHOLD}	Bus Hold Input Leakage Current	1.65	V _I =0.58 V	+ 25		+ 25		μA
		1.65	V _I =1.07 V	- 25		- 25		
		2.3	V _I =0.7 V	+ 45		+ 45		
		2.3	V _I =1.7 V	- 45		- 45		
		3.0	V _I =0.8 V	+ 75		+ 75		
		3.0	V _I =2 V	- 75		- 75		
		3.6	V _I = 0 to 3.6 V		± 500		± 500	
I _{off}	Power Off Leakage Current	0	V _I or V _O = 3.6V		10		20	μA
I _{OZ}	High Impedance Output Leakage Current	3.6	V _I = V _{IH} or V _{IL} V _O = 0 to V _{CC}		± 5		± 10	μA
I _{CC}	Quiescent Supply Current	3.6	V _I = V _{CC} or GND I _O = 0		20		40	μA
ΔI _{CC}	I _{CC} incr. per Input	3.0 to 3.6	V _{IH} = V _{CC} - 0.6V		500		750	μA

AC ELECTRICAL CHARACTERISTICS

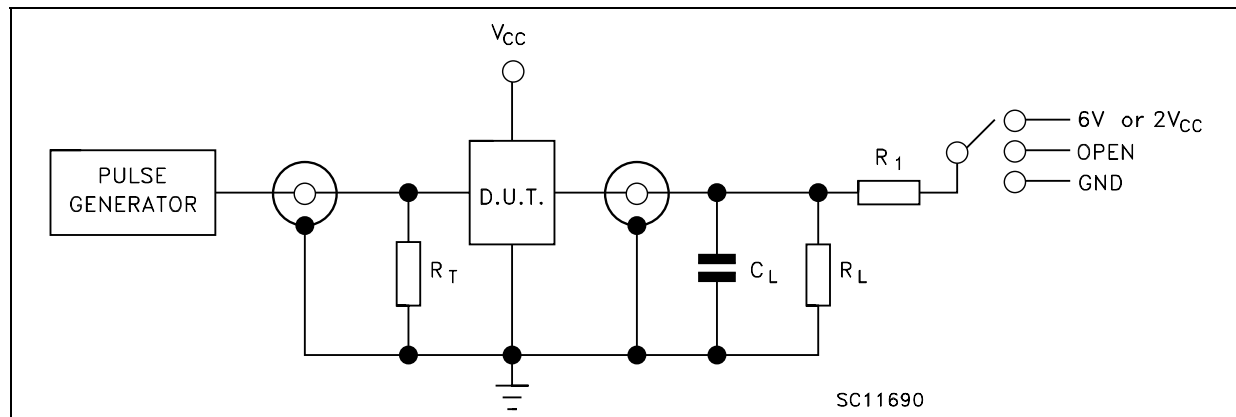
Symbol	Parameter	Test Condition				Value				Unit
		V _{CC} (V)	C _L (pF)	R _L (Ω)	t _s = t _r (ns)	-40 to 85 °C		-55 to 125 °C		
						Min.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay Time CK to Qn	1.65 to 1.95	30	1000	2.0	1	6.5	1	6.5	ns
		2.3 to 2.7	30	500	2.0	1	5.4	1	5.4	
		2.7	50	500	2.5	1	5.4	1	5.4	
		3.0 to 3.6	50	500	2.5	1	4.6	1	4.6	
t _{PZL} t _{PZH}	Output Enable Time	1.65 to 1.95	30	1000	2.0	1	8.0	1	8.0	ns
		2.3 to 2.7	30	500	2.0	1	6.5	1	6.5	
		2.7	50	500	2.5	1	6.4	1	6.4	
		3.0 to 3.6	50	500	2.5	1	5.2	1	5.2	
t _{PLZ} t _{PHZ}	Output Disable Time	1.65 to 1.95	30	1000	2.0	1	6.8	1	6.8	ns
		2.3 to 2.7	30	500	2.0	1	5.6	1	5.6	
		2.7	50	500	2.5	1	5	1	4.5	
		3.0 to 3.6	50	500	2.5	1	4.5	1	4.5	
t _s	Setup Time, HIGH or LOW level Dn to CK	1.65 to 1.95	30	1000	2.0	2.1		2.1		ns
		2.3 to 2.7	30	500	2.0	2.1		2.1		
		2.7	50	500	2.5	2.2		2.2		
		3.0 to 3.6	50	500	2.5	1.9		1.9		
t _h	Hold Time High or LOW level Dn to CK	1.65 to 1.95	30	1000	2.0	0.8		0.8		ns
		2.3 to 2.7	30	500	2.0	0.6		0.6		
		2.7	50	500	2.5	0.5		0.5		
		3.0 to 3.6	50	500	2.5	0.5		0.5		
t _w	CK Pulse Width, HIGH	1.65 to 1.95	30	1000	2.0	4		4		ns
		2.3 to 2.7	30	500	2.0	3.3		3.3		
		2.7	50	500	2.5	3.3		3.3		
		3.0 to 3.6	50	500	2.5	3.3		3.3		
f _{MAX}	Maximum Clock Pulse Frequency	1.65 to 1.95	30	1000	2.0	120		120		MHz
		2.3 to 2.7	30	500	2.0	150		150		
		2.7	50	500	2.5	200		200		
		3.0 to 3.6	50	500	2.5	300		300		

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value			Unit
		V _{CC} (V)		T _A = 25 °C			
				Min.	Typ.	Max.	
C _{IN}	Input Capacitance Control Inputs	3.3	V _{IN} =V _{CC} or GND		3		pF
C _{IN}	Input Capacitance Data Inputs	3.3	V _{IN} =V _{CC} or GND		6		pF
C _{OUT}	Output Capacitance	3.3	V _{IN} = 0 to V _{CC}		7		pF
C _{PD}	Power Dissipation Capacitance Output enabled (note 1)	3.3	f _{IN} = 10MHZ C _L =50pF V _{IN} = 0 or V _{CC}		19		pF
		2.5			16		
C _{PD}	Power Dissipation Capacitance Output disabled (note 1)	3.3			5		
		2.5			4		

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/16$ (per circuit)

TEST CIRCUIT



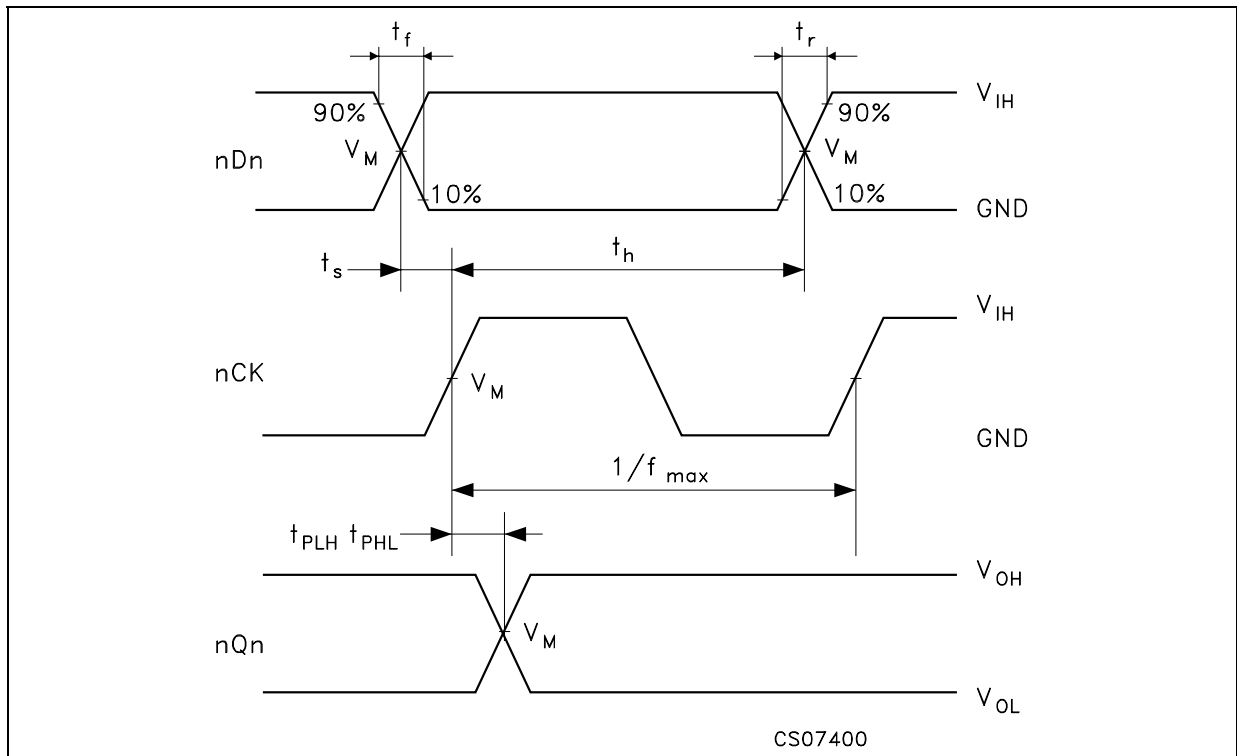
TEST	SWITCH
t _{PLH} , t _{PHL}	Open
t _{PZL} , t _{PLZ} (V _{CC} = 3.0 to 3.6V)	6V
t _{PZL} , t _{PLZ} (V _{CC} = 2.3 to 2.7V)	2V _{CC}
t _{PZH} , t _{PHZ}	GND

R_T = Z_{OUT} of pulse generator (typically 50Ω)

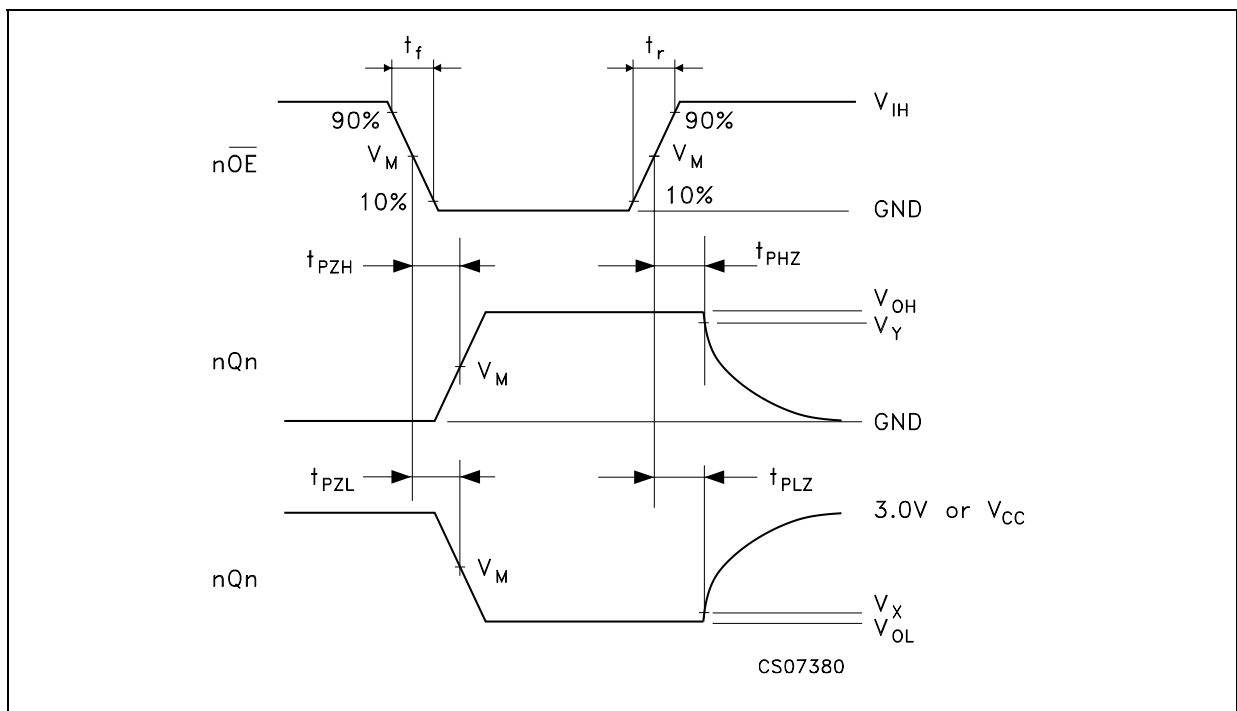
TEST CIRCUIT AND WAVEFORM SYMBOL VALUE

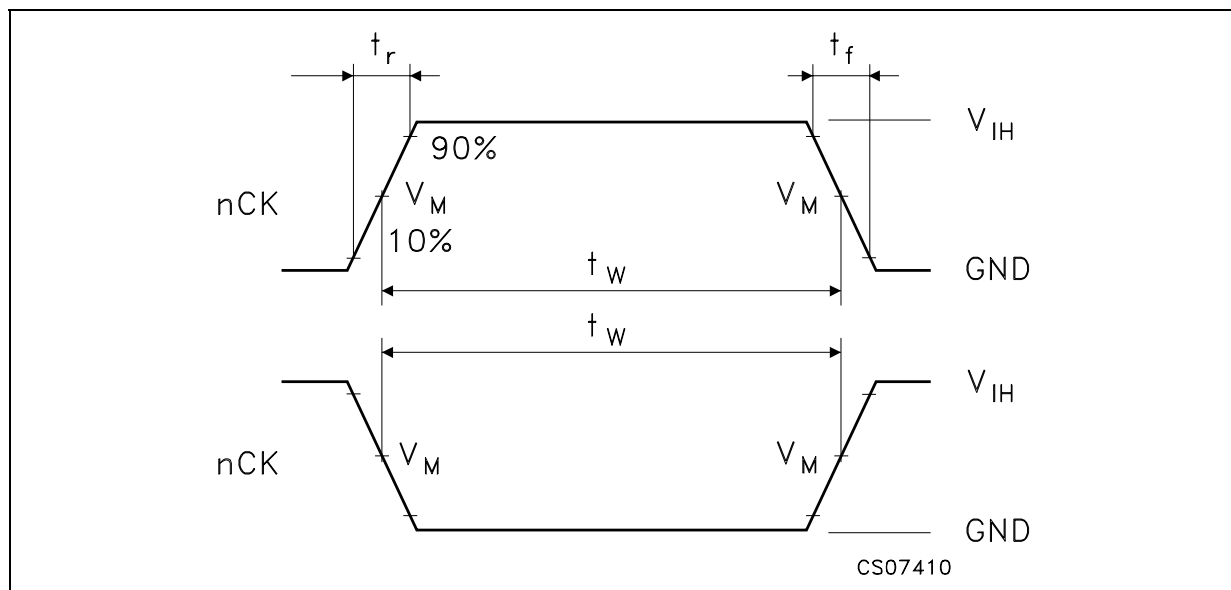
Symbol	V _{CC}			
	3.0 to 3.6V	2.7V	2.3 to 2.7V	1.65 to 1.95V
V _{IH}	2.7V	2.7V	V _{CC}	V _{CC}
V _M	1.5V	1.5V	V _{CC} /2	V _{CC} /2
V _X	V _{OL} + 0.3V	V _{OL} + 0.3V	V _{OL} + 0.15V	V _{OL} + 0.15V
V _Y	V _{OH} - 0.3V	V _{OH} - 0.3V	V _{OH} - 0.15V	V _{OH} - 0.15V
C _L	50pF	50pF	30pF	30pF
R _L = R ₁	500Ω	500Ω	500Ω	1000Ω
t _r = t _f	<2.5ns	<2.5ns	<2.0ns	<2.0ns

WAVEFORM 1 : PROPAGATION DELAYS, CK MINIMUM PULSE WIDTH, Dn TO CK SETUP AND HOLD TIMES, CK MAXIMUM FREQUENCY ($f=1\text{MHz}$; 50% duty cycle)



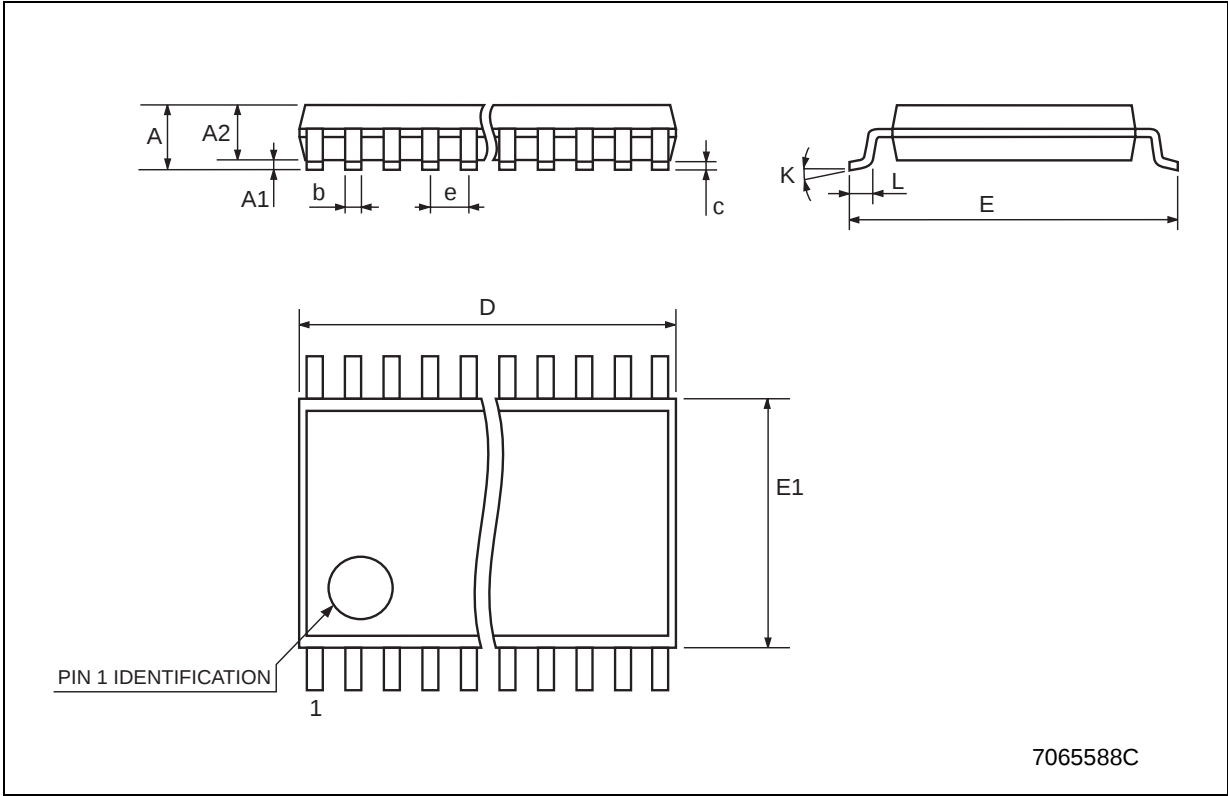
WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIME ($f=1\text{MHz}$; 50% duty cycle)



WAVEFORM 3 : CK MINIMUM PULSE WIDTH ($f=1\text{MHz}$; 50% duty cycle)

TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	12.4		12.6	0.408		0.496
E		8.1 BSC			0.318 BSC	
E1	6.0		6.2	0.236		0.244
e		0.5 BSC			0.0197 BSC	
K	0°		8°	0°		8°
L	0.50		0.75	0.020		0.030



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