



74ACT574

OCTAL D-TYPE FLIP-FLOP WITH 3 STATE OUTPUTS (NON INVERTED)

- HIGH SPEED:
 $f_{MAX} = 270\text{MHz}$ (TYP.) at $V_{CC} = 5.0\text{V}$
- LOW POWER DISSIPATION:
 $I_{CC} = 4\mu\text{A}$ (MAX.) at $T_A = 25^\circ\text{C}$
- COMPATIBLE WITH TTL OUTPUTS
 $V_{IH} = 2\text{V}$ (MIN.), $V_{IL} = 0.8\text{V}$ (MAX.)
- 50Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 24\text{mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \approx t_{PHL}$
- OPERATING VOLTAGE RANGE:
 V_{CC} (OPR) = 4.5V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 574
- IMPROVED LATCH-UP IMMUNITY

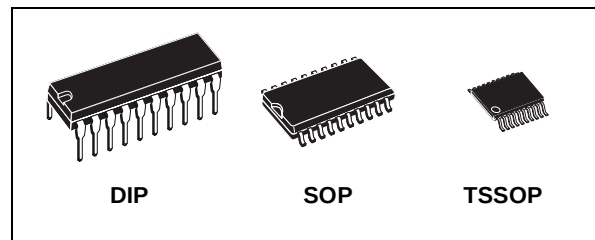
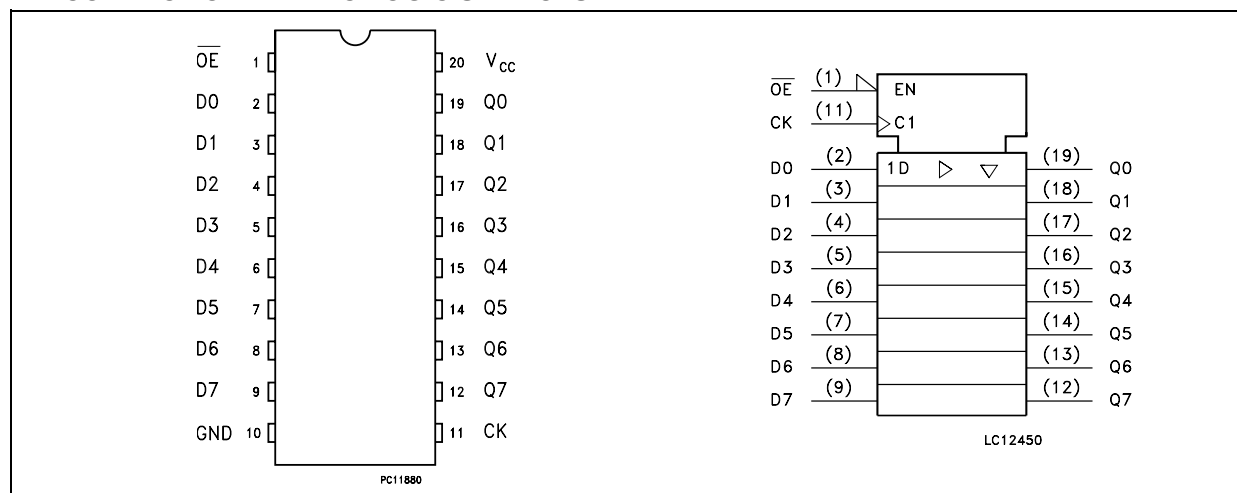
DESCRIPTION

The 74ACT574 is an advanced high-speed CMOS OCTAL D-TYPE FLIP-FLOP with 3 STATE OUTPUT NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology.

These 8 bit D-Type Flip-Flop are controlled by a clock input (CK) and an output enable input ($\overline{OE}$). On the positive transition of the clock, the Q outputs will be set to the logic that were setup at the D inputs.

While the ($\overline{OE}$) input is low, the 8 outputs will be in

PIN CONNECTION AND IEC LOGIC SYMBOLS



ORDER CODES

PACKAGE	TUBE	T & R
DIP	74ACT574B	
SOP	74ACT574M	74ACT574MTR
TSSOP		74ACT574TTR

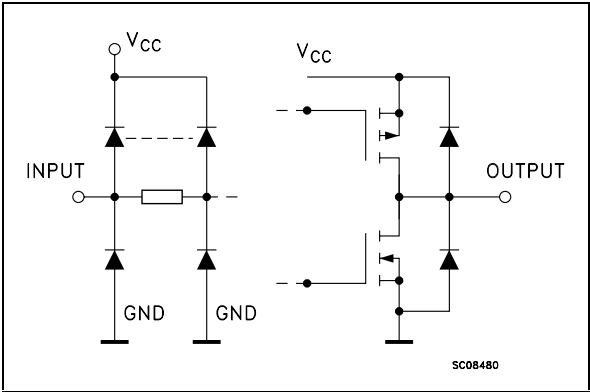
a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state.

The output control does not affect the internal operation of flip-flops; that is, the old data can be retained or the new data can be entered even while the outputs are off.

This device is designed to interface directly High Speed CMOS systems with TTL and NMOS components.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

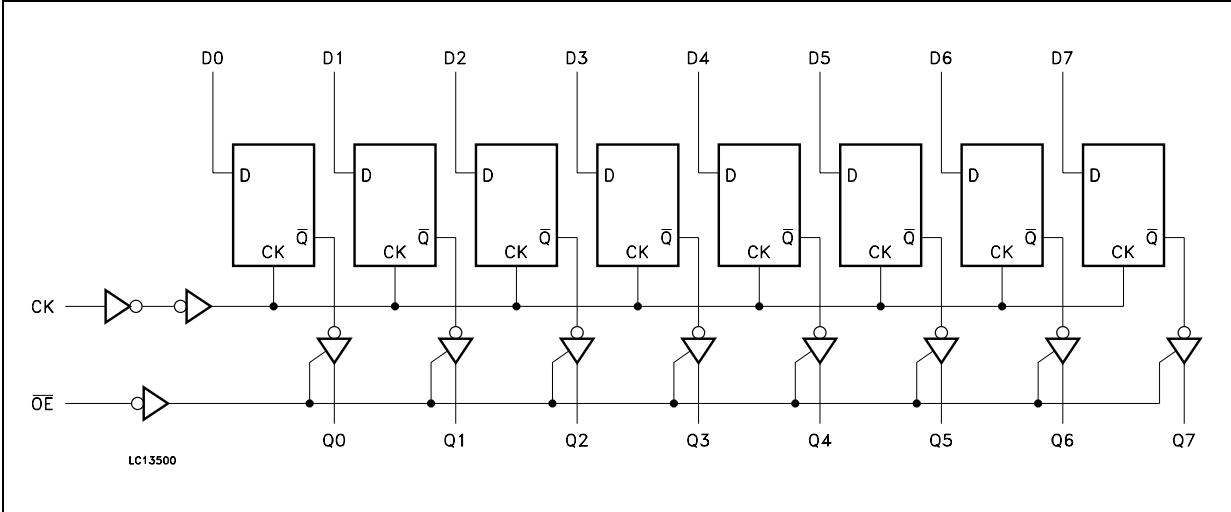
PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3-State Output Enable (Active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0 to D7	Data Inputs
12, 13, 14, 15, 16, 17, 18, 19	Q0 to Q7	3-State Outputs
11	CK	Clock Input (LOW-to-HIGH Edge Trigger)
10	GND	Ground (0V)
20	V _{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS			OUTPUT
$\overline{OE}$	CK	D	Q
H	X	X	Z
L		X	NO CHANGE
L		L	L
L		H	H

X : Don't Care
Z : High Impedance

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 400	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time $V_{CC} = 4.5$ to 5.5V (note 1)	8	ns/V

1) V_{IN} from 0.8V to 2.0V

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value								Unit
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C			
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
V _{IH}	High Level Input Voltage	4.5	V _O = 0.1 V or V _{CC} -0.1V	2.0	1.5		2.0		2.0		V	
		5.5		2.0	1.5		2.0		2.0			
V _{IL}	Low Level Input Voltage	4.5	V _O = 0.1 V or V _{CC} -0.1V		1.5	0.8		0.8		0.8	V	
		5.5			1.5	0.8		0.8		0.8		
V _{OH}	High Level Output Voltage	4.5	I _O =-50 μA	4.4	4.49		4.4		4.4		V	
		5.5	I _O =-50 μA	5.4	5.49		5.4		5.4			
		4.5	I _O =-24 mA	3.86			3.76		3.7		V	
		5.5	I _O =-24 mA	4.86			4.76		4.7			
V _{OL}	Low Level Output Voltage	4.5	I _O =50 μA		0.001	0.1		0.1		0.1	V	
		5.5	I _O =50 μA		0.001	0.1		0.1		0.1		
		4.5	I _O =24 mA			0.36		0.44		0.5		
		5.5	I _O =24 mA			0.36		0.44		0.5		
I _I	Input Leakage Cur- rent	5.5	V _I = V _{CC} or GND			± 0.1		± 1		± 1	μA	
I _{OZ}	High Impedance Output Leakege Current	5.5	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND			± 0.5		± 5		± 5	μA	
I _{CCT}	Max I _{CC} /Input	5.5	V _I = V _{CC} - 2.1V		0.6			1.5		1.6	mA	
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			4		40		80	μA	
I _{OLD}	Dynamic Output Current (note 1, 2)	5.5	V _{OLD} = 1.65 V max					75		50	mA	
I _{OHD}			V _{OHD} = 3.85 V min					-75		-50	mA	

1) Maximum test duration 2ms, one output loaded at time

2) Incident wave switching is guaranteed on trasmission lines with impedances as low as 50Ω

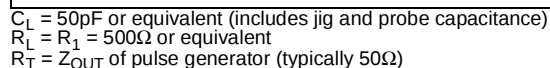
AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, Input $t_r = t_f = 3\text{ns}$)

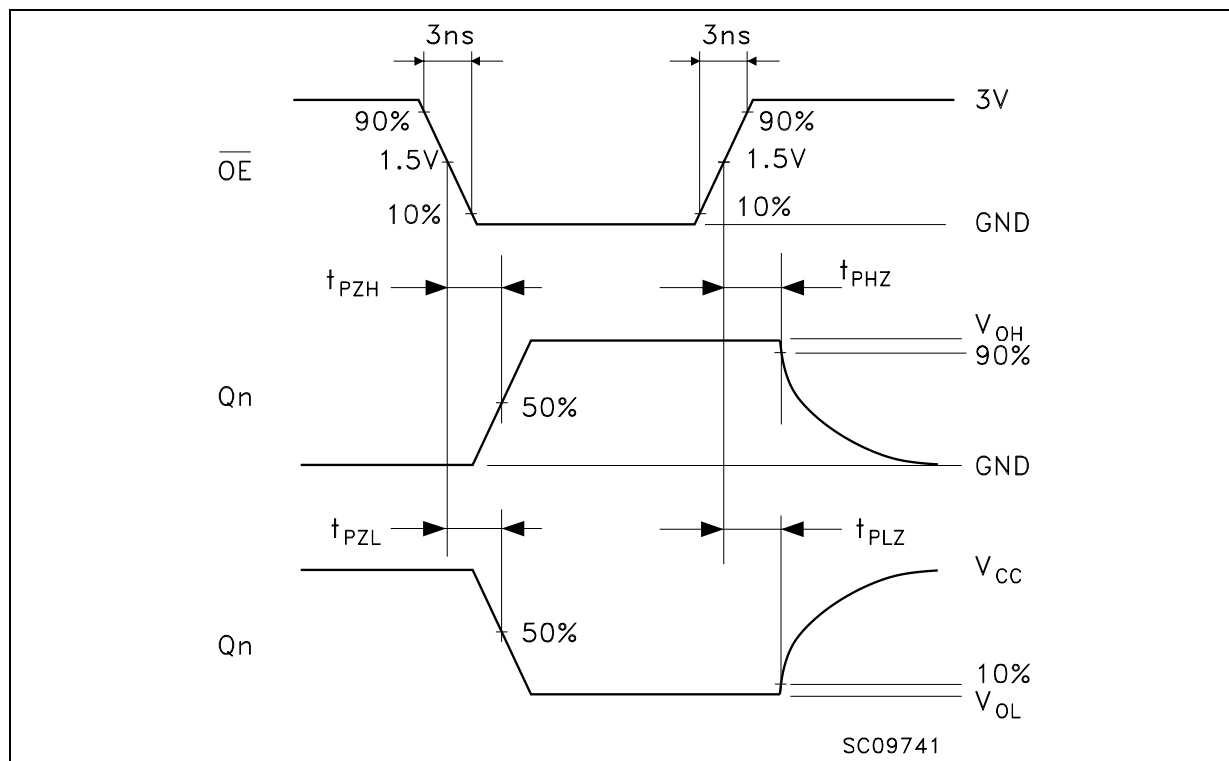
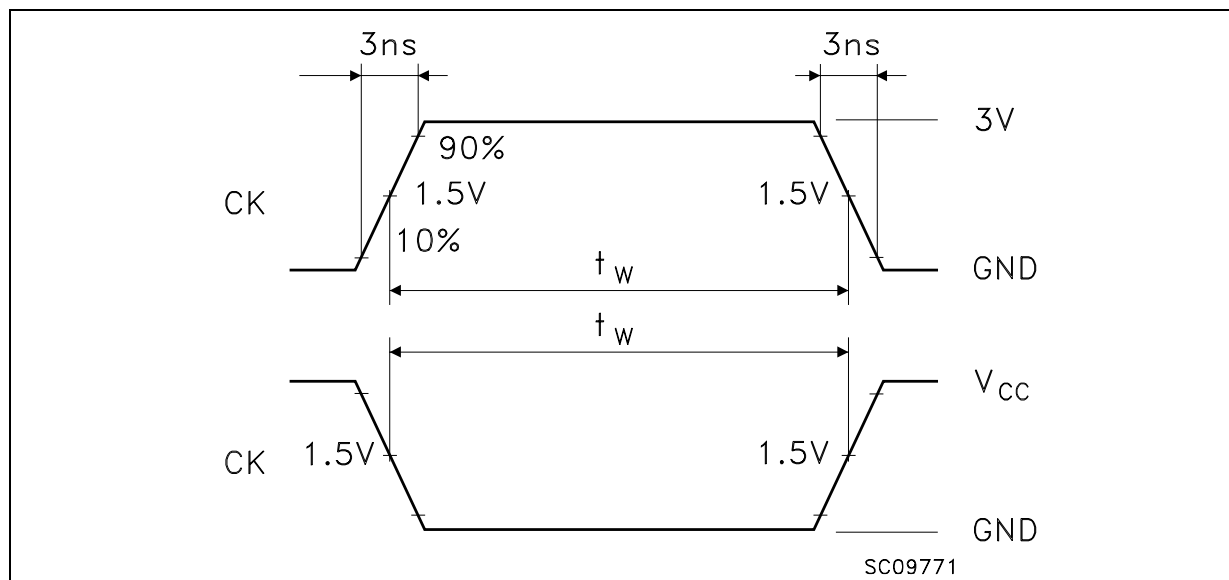
Symbol	Parameter	Test Condition		Value								Unit
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C			
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Time CK to Q	5.0 ^(*)			5.0	10.0		11.0		11.0	ns	
t _{PZL} t _{PZH}	Output Enable Time	5.0 ^(*)			5.5	9.0		10.0		10.0	ns	
t _{PLZ} t _{PHZ}	Output Disable Time	5.0 ^(*)			5.0	8.5		9.0		9.0	ns	
t _W	CK Pulse Width HIGH or LOW	5.0 ^(*)			1.5	3.0		4.0		4.0	ns	
t _s	Setup Time D to CK, HIGH or LOW	5.0 ^(*)			1.0	2.5		3.0		3.0	ns	
t _h	Hold Time D to CK, HIGH or LOW	5.0 ^(*)			-1.0	2.5		3.0		3.0	ns	
f _{MAX}	Maximum CK Frequency	5.0 ^(*)		100	270		85		85		MHz	

(*) Voltage range is $5.0\text{V} \pm 0.5\text{V}$ **CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Test Condition		Value								Unit
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C			
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
C _{IN}	Input Capacitance	5.0			4						pF	
C _{OUT}	Output Capacitance	5.0			8						pF	
C _{PD}	Power Dissipation Capacitance (note 1)	5.0	f _{IN} = 10MHz		26						pF	

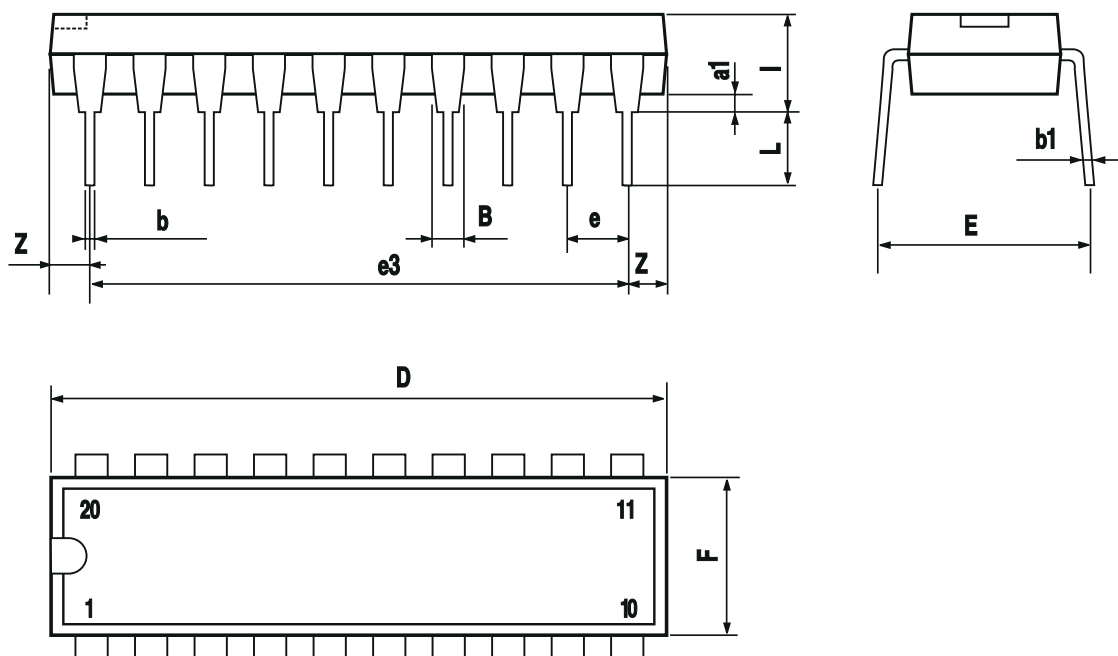
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/n$ (per circuit)



WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIMES ($f=1\text{MHz}$; 50% duty cycle)**WAVEFORM 3: PULSE WIDTH** ($f=1\text{MHz}$; 50% duty cycle)

Plastic DIP-20 (0.25) MECHANICAL DATA

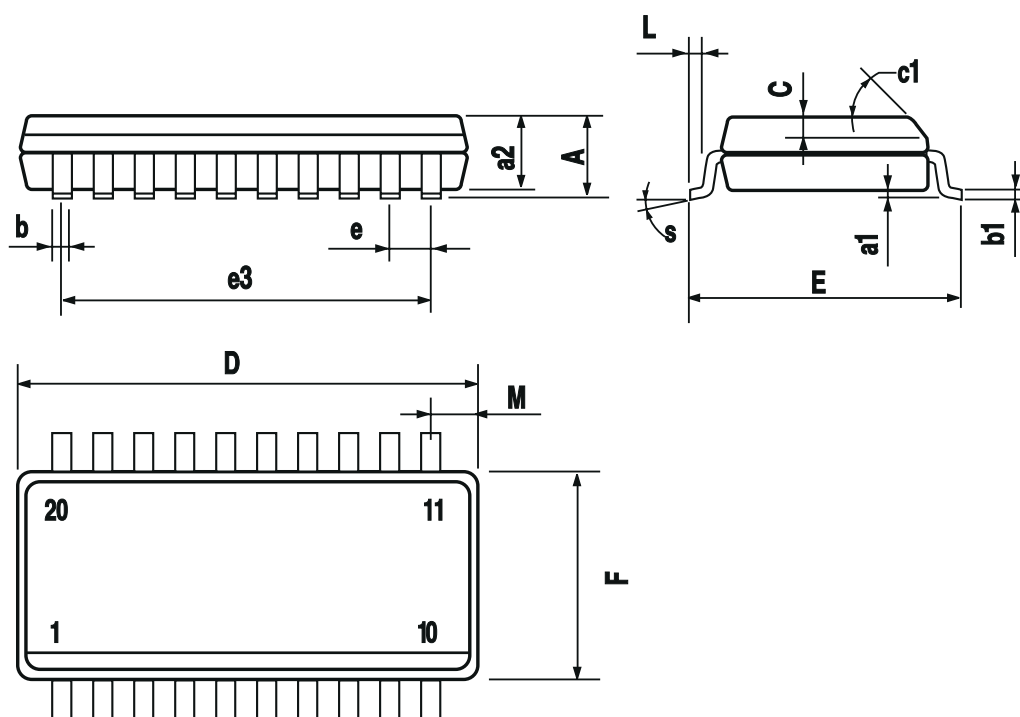
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053



P001J

SO-20 MECHANICAL DATA

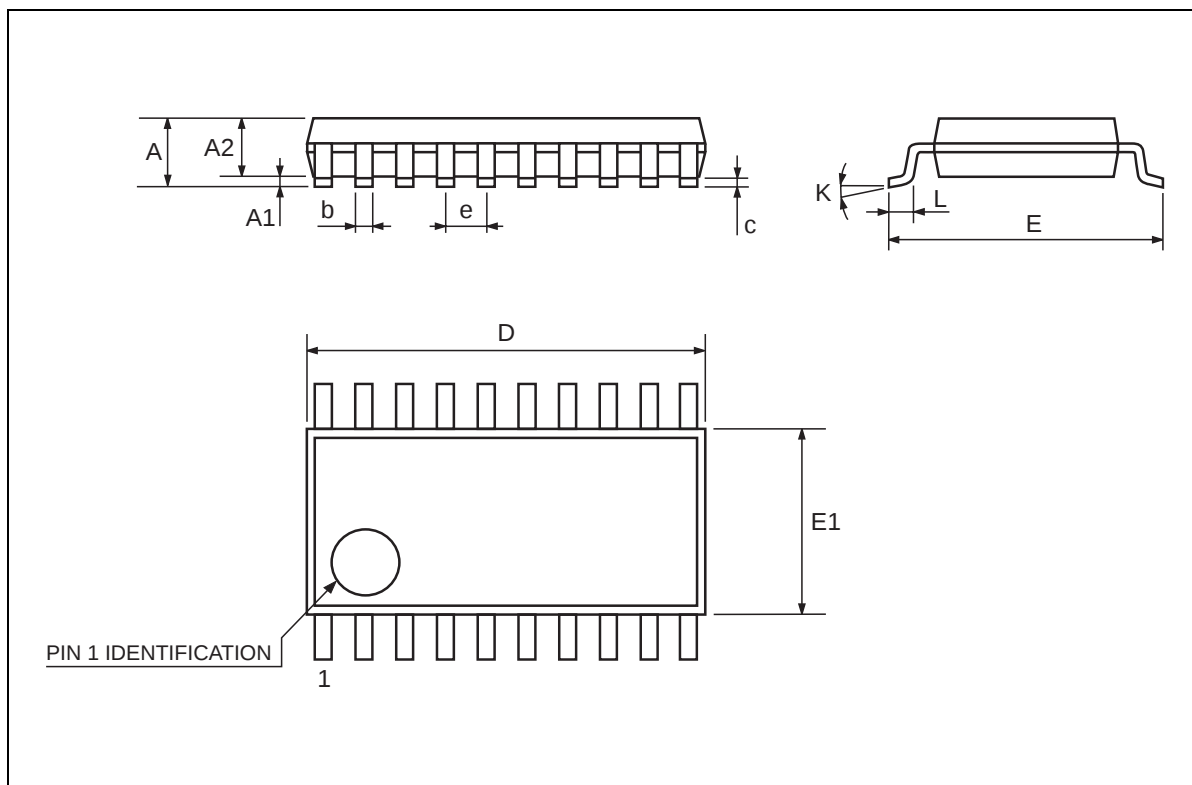
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45 (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
M			0.75			0.029
S	8 (max.)					



P013L

TSSOP20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.2	0.0035		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028



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