Ordering number:ENN2129B

N-Channel Silicon MOSFET (Dual Gate)

3SK180

High-Frequency General-Purpose Amplifier Applications

Applications

· FM tuners and VHF tuners.

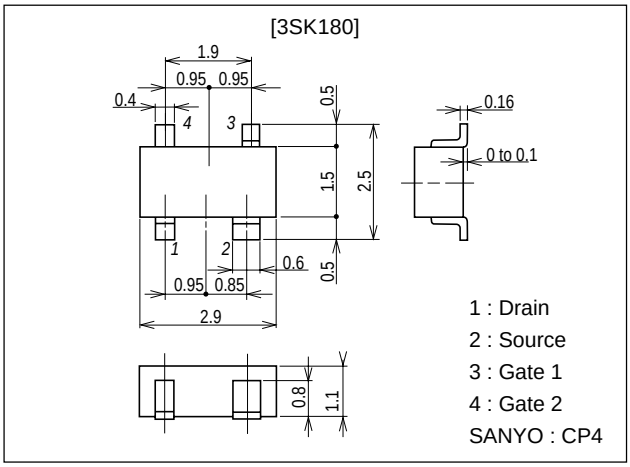
Features

· High power gain and low noise figure.
· High forward transfer admittance.

Package Dimensions

unit:mm

2046A



Specifications

Absolute Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DS}		15	V
Gate1-to-Source Voltage	V_{G1S}		±7	V
Gate2-to-Source Voltage	V_{G2S}		±7	V
Drain Current	I_D		30	mA
Allowable Power Dissipation	P_D		200	mW
Channel Temperature	Tch		125	˚C
Storage Temperature	Tstg		–55 to +125	˚C

Electrical Characteristics at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Voltage	V_{DS}	V_{G1S}=–4V, V_{G2S}=0V, I_{DS}=100µA	15			V
Gate1-to-Source Breakdown Voltage	$V_{(BR)G1SS}$	I_{G1}=10µA, V_{DS}=0, V_{G2S}=0V	±7			V
Gate2-to-Source Breakdown Voltage	$V_{(BR)G2SS}$	I_{G2}=10µA, V_{DS}=0, V_{G1S}=0V	±7			V
Gate1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS}=10V, V_{G2S}=4V, I_D=100µA			–3	V
Gate2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS}=10V, V_{G1S}=0V, I_D=100µA			–2.5	V
Gate1-to-Source Leakage Current	I_{G1SS}	V_{G1S}=±5V, V_{G2S}=V_{DS}=0V			±50	nA
Gate2-to-Source Leakage Current	I_{G2SS}	V_{G2S}=±5V, V_{G1S}=V_{DS}=0V			±50	nA
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=10V, V_{G1S}=0, V_{G2S}=4V	2.5*		24*	mA

* : The 3SK180 is classified by I_{DSS} as follows : (unit : mA)

2.5	4	6.0	5.0	5	12.0	10.0	6	24.0

Marking : DJ
I_{DSS} rank : 4, 5, 6

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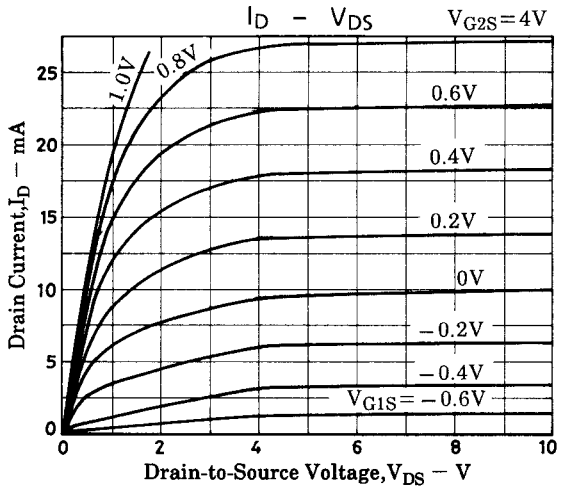
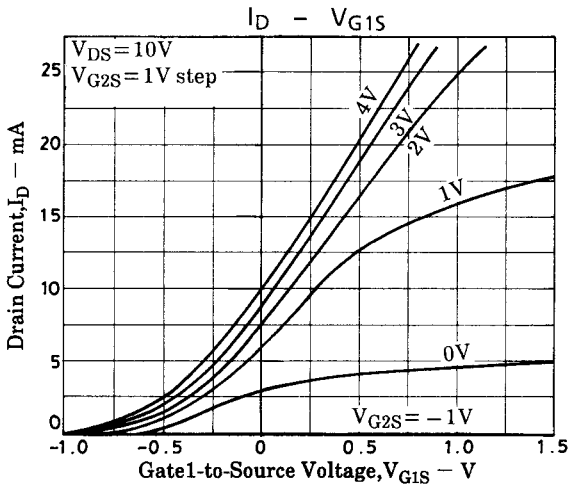
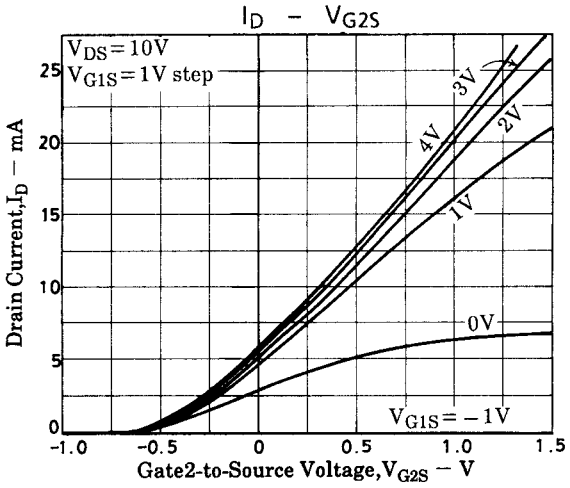
SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

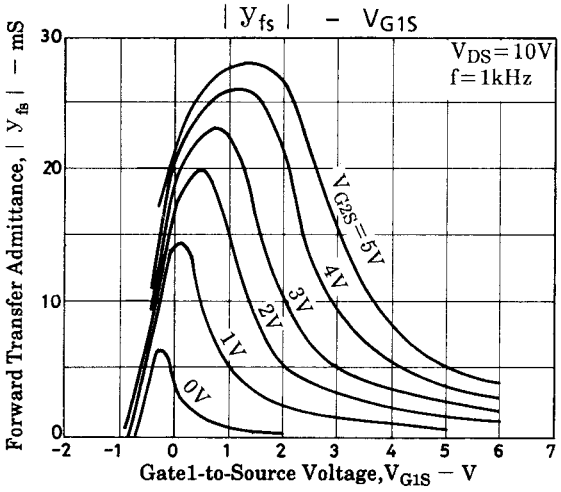
Continued from preceding page.

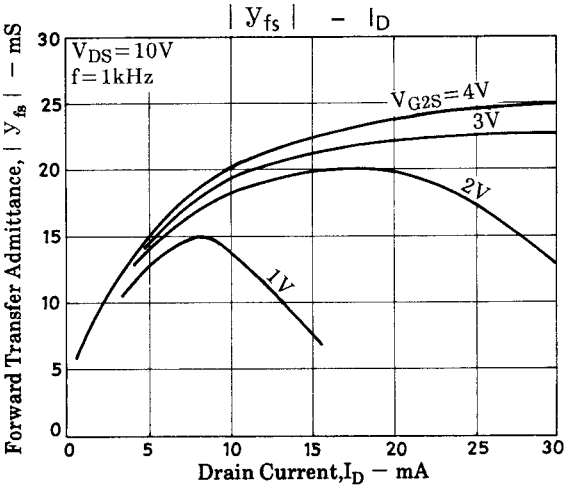
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Forward Transfer Admittance	| yfs |	f=1kHz, I_D=10mA, V_{DS}=10V, V_{G2S}=4V		20		mS
Input Capacitance	Ciss	V_{DS}=10V, f=1MHz, V_{G1S}=0V, V_{G2S}=4V		3.0		pF
Reverse Transfer Capacitance	Crss	V_{DS}=10V, f=1MHz, V_{G1S}=0V, V_{G2S}=4V		0.02	0.05	pF
Power Gain	PG	V_{DS}=10V, I_D=10mA	22	28		dB
Noise Figure	NF	f=100MHz, V_{G2S}=4V		1.8	3.0	dB

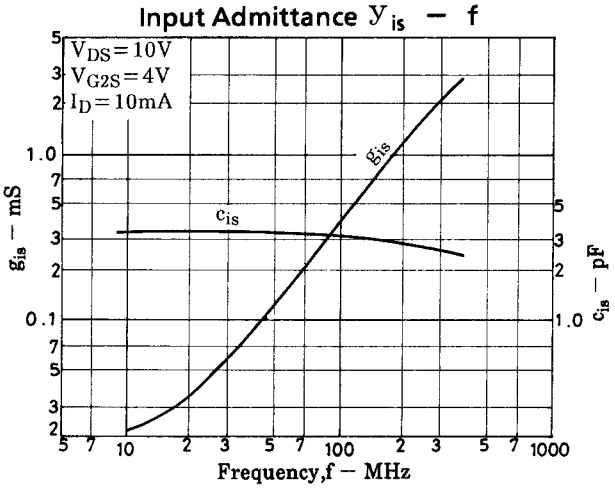




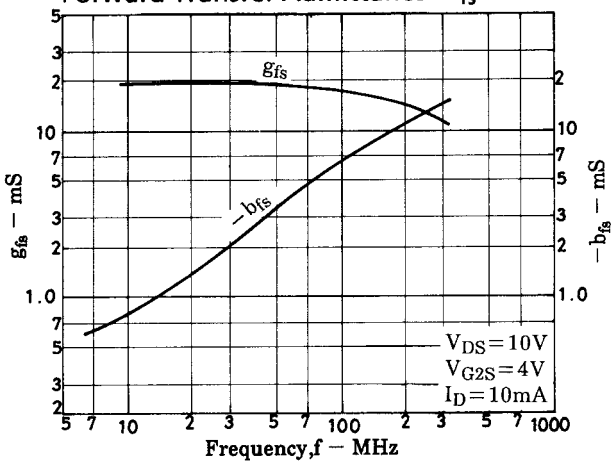




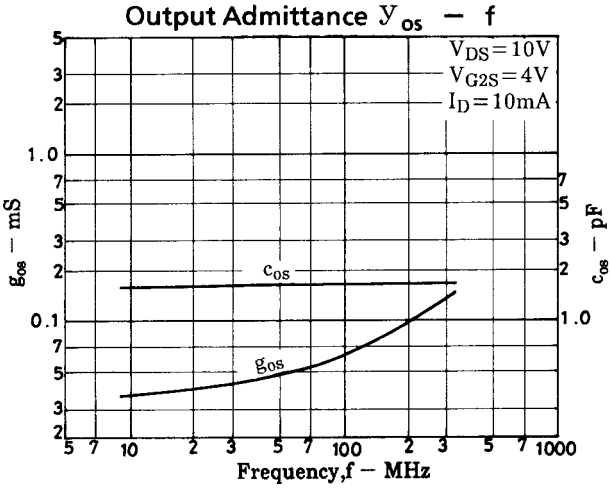




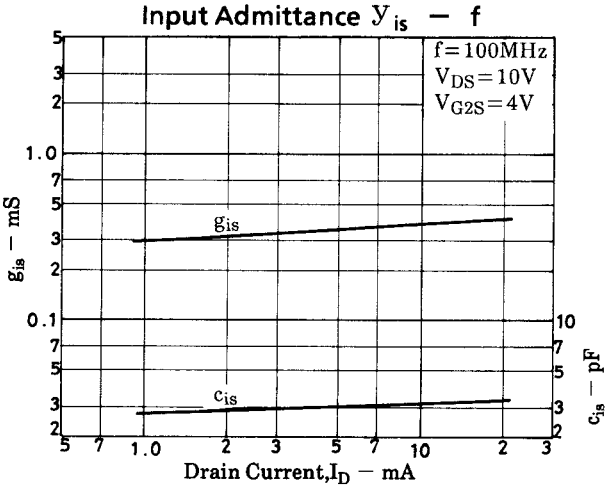
Forward Transfer Admittance y_{fs} — f



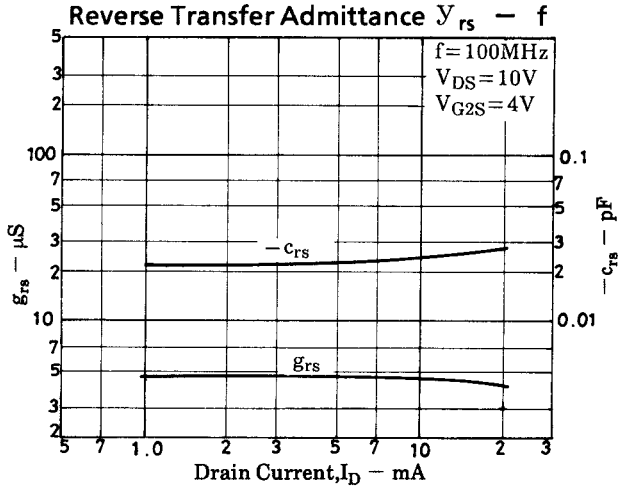
Output Admittance y_{os} — f



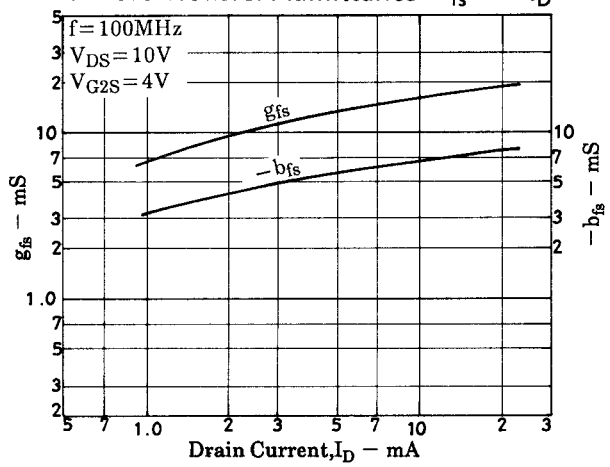
Input Admittance y_{is} — f



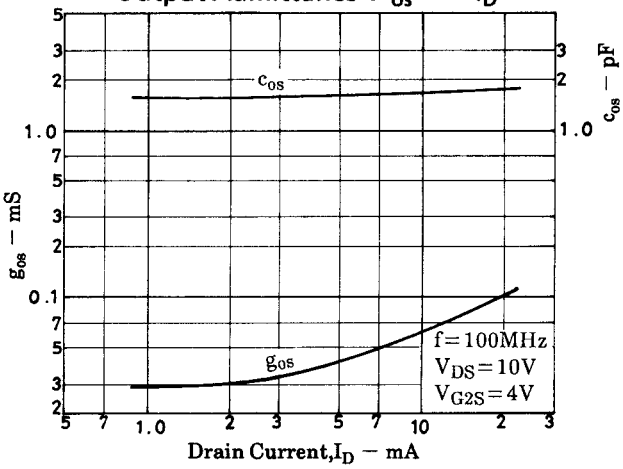
Reverse Transfer Admittance y_{rs} — f



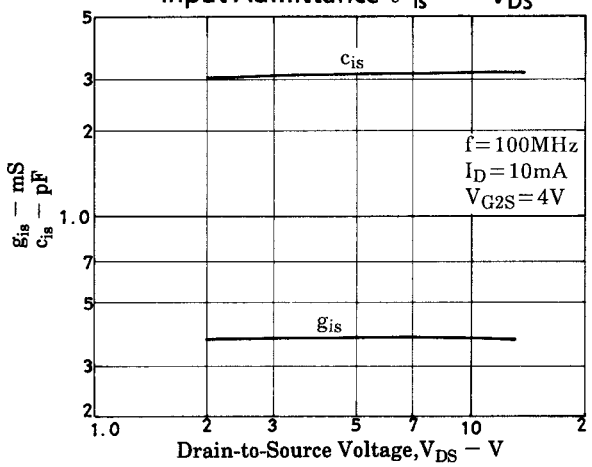
Forward Transfer Admittance y_{fs} — I_D



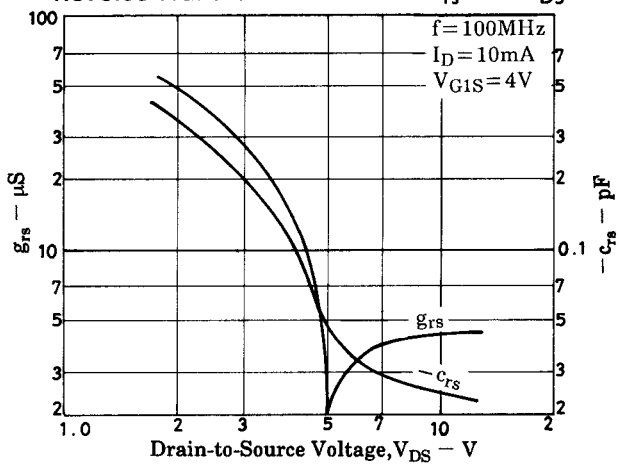
Output Admittance y_{os} — I_D



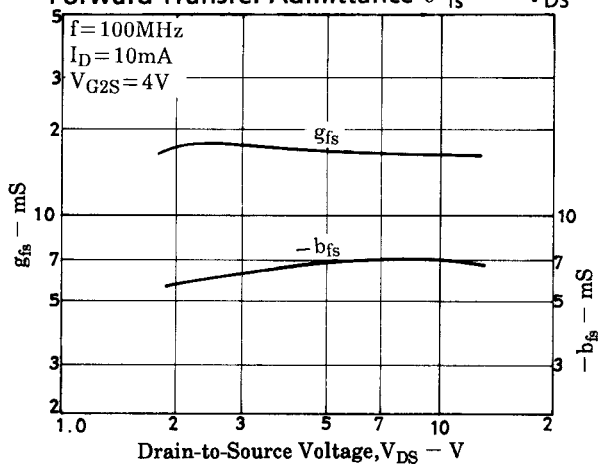
Input Admittance y_{is} — V_{DS}



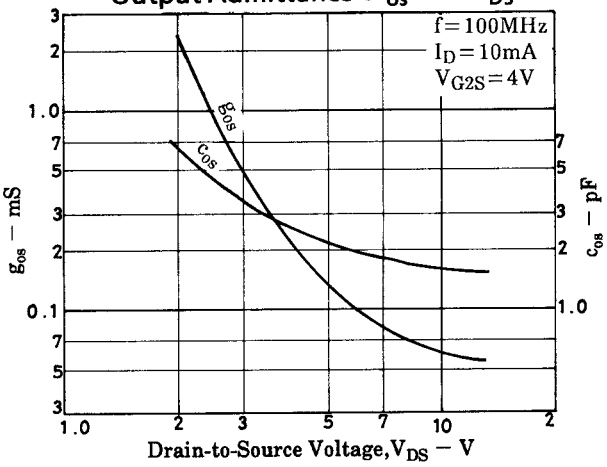
Reverse Transfer Admittance y_{rs} — V_{DS}



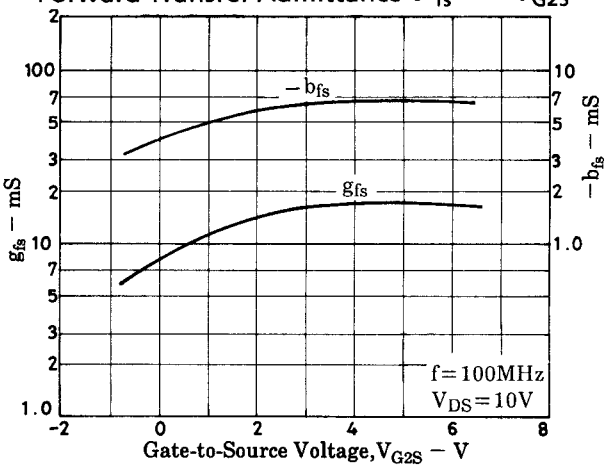
Forward Transfer Admittance y_{fs} – V_{DS}



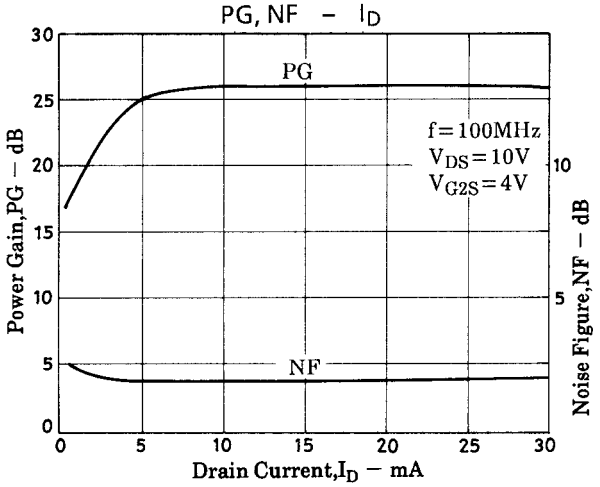
Output Admittance y_{os} – V_{DS}



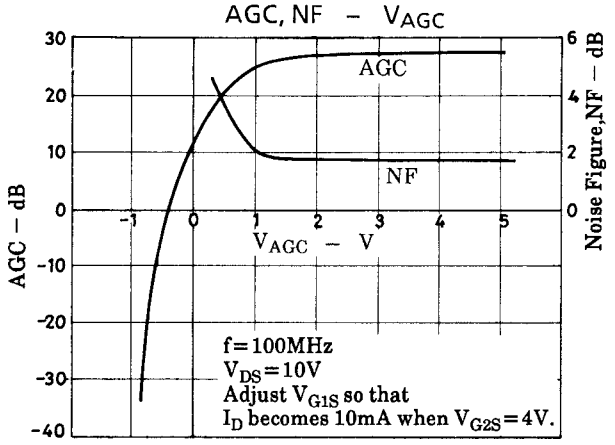
Forward Transfer Admittance y_{fs} – V_{G2S}



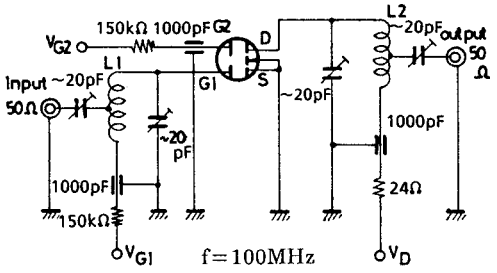
PG, NF – I_D



AGC, NF – V_{AGC}



PG, NF Specified Test Circuit



L1 : 1mmø plated wire 10mmø 4T, tap : 1T from gate side

L2 : 1mmø plated wire 10mmø 6T, tap : 1T from drain side