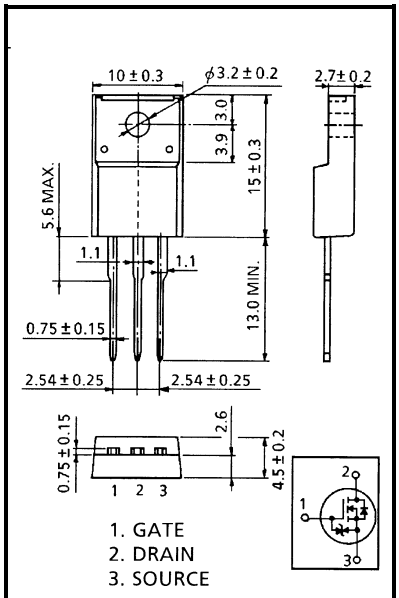
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (π−MOSV)

2SK2952

Chopper Regulator Applications

- Low drain−source ON resistance : $R_{DS\ (ON)}$ = 0.4 Ω (typ.)
- High forward transfer admittance : $|Y_{fs}|$ = 8.0 S (typ.)
- Low leakage current : I_{DSS} = 100 μA (max) (V_{DS} = 400 V)
- Enhancement−mode : V_{th} = 2.0~4.0 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



JEDEC	—
JEITA	SC-67
TOSHIBA	2-10R1B

Weight: 1.9 g (typ.)

Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain−source voltage		V_{DSS}	400	V
Drain−gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	400	V
Gate−source voltage		V_{GSS}	±30	V
Drain current	DC (Note 1)	I_D	8.5	A
	Pulse (Note 1)	I_{DP}	34	A
Drain power dissipation (Tc = 25°C)		P_D	40	W
Single pulse avalanche energy (Note 2)		E_{AS}	427	mJ
Avalanche current		I_{AR}	8.5	A
Repetitive avalanche energy (Note 3)		E_{AR}	4.0	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch-c)}$	3.125	°C / W
Thermal resistance, channel to ambient	$R_{th\ (ch-a)}$	62.5	°C / W

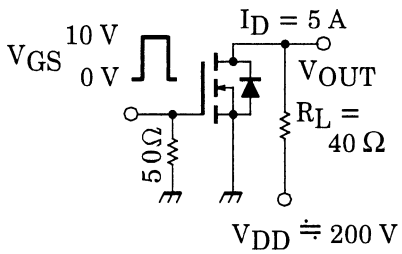
Note 1: Please use devices on condition that the channel temperature is below 150°C.

Note 2: V_{DD} = 90 V, T_{ch} = 25°C, L = 9.6 mH, R_G = 25 Ω, I_{AR} = 8.5 A

Note 3: Repetitive rating: Pulse width limited by maximum channel temperature

This transistor is an electrostatic sensitive device.
Please handle with caution.

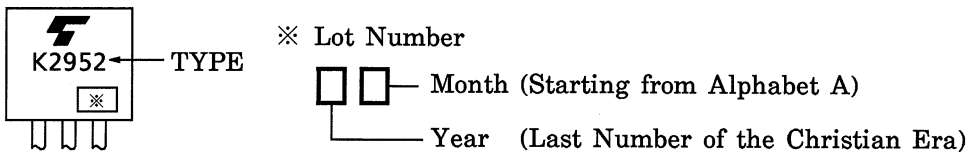
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±25 V, V_{DS} = 0 V	—	—	±10	μA
Gate−source breakdown voltage		$V_{(BR)\ GSS}$	I_G = ±10 μA, V_{DS} = 0 V	±30	—	—	V
Drain cut−off current		I_{DSS}	V_{DS} = 400 V, V_{GS} = 0 V	—	—	100	μA
Drain−source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	400	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	2.0	—	4.0	V
Drain−source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 10 V, I_D = 5 A	—	0.4	0.55	Ω
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 5 A	4.0	8.0	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	1340	—	pF
Reverse transfer capacitance		C_{rss}		—	160	—	
Output capacitance		C_{oss}		—	490	—	
Switching time	Rise time	t_r	 Duty ≦ 1%, t_w = 10 μs	—	22	—	ns
	Turn−on time	t_{on}		—	60	—	
	Fall time	t_f		—	32	—	
	Turn−off time	t_{off}		—	140	—	
Total gate charge (gate−source plus gate−drain)		Q_g	V_{DD} ≈ 320 V, V_{GS} = 10 V, I_D = 8.5 A	—	34	—	nC
Gate−source charge		Q_{gs}		—	18	—	
Gate−drain (“miller”) Charge		Q_{gd}		—	16	—	

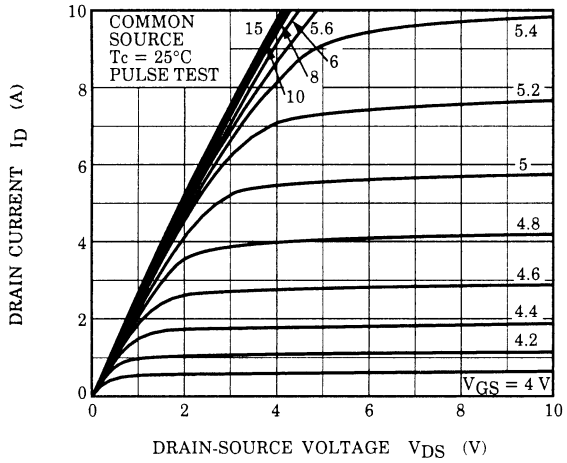
Source−Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	8.5	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	34	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 8.5 A, V_{GS} = 0 V	—	—	−1.7	V
Reverse recovery time	t_{rr}	I_{DR} = 8.5 A, V_{GS} = 0 V dI_{DR}/dt = 100 A/μs	—	350	—	ns
Reverse recovery charge	Q_{rr}		—	2.6	—	μC

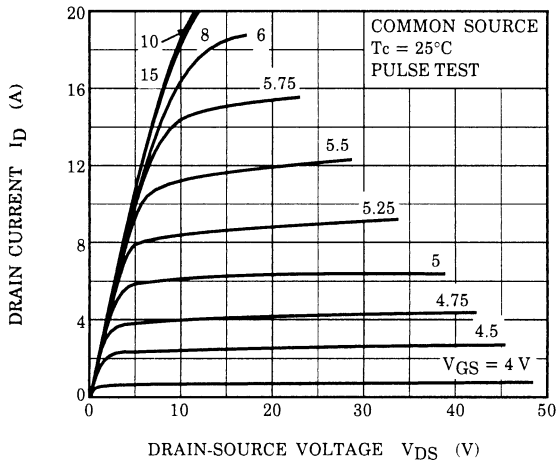
Marking



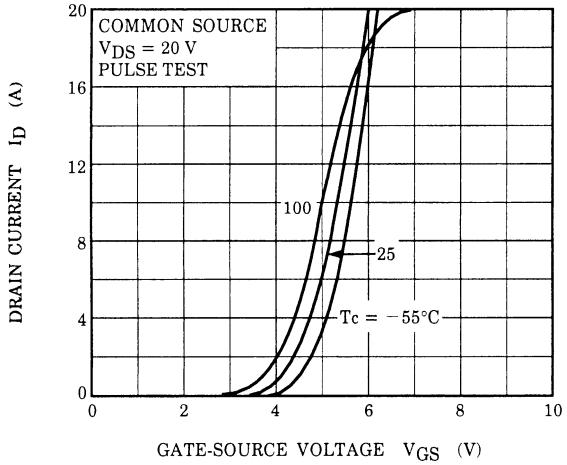
$I_D - V_{DS}$



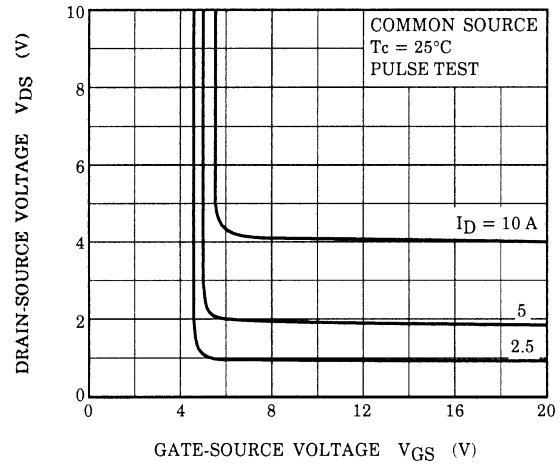
$I_D - V_{DS}$



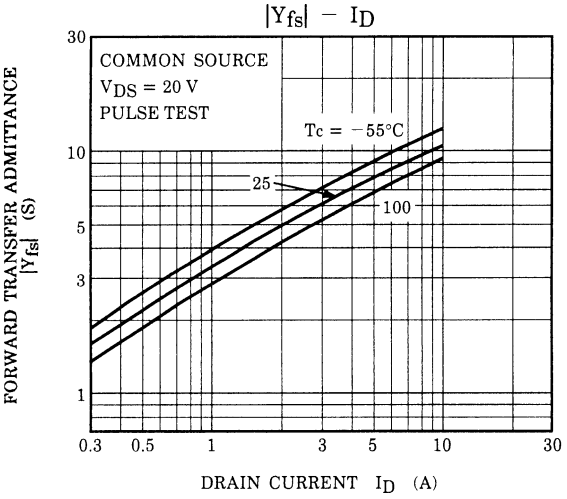
$I_D - V_{GS}$



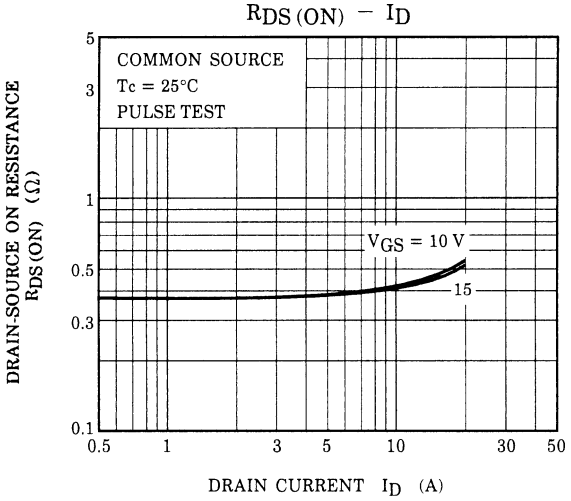
$V_{DS} - V_{GS}$



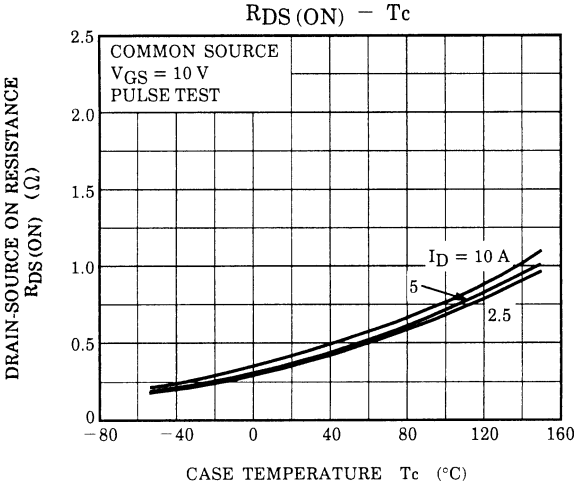
$|Y_{fs}| - I_D$



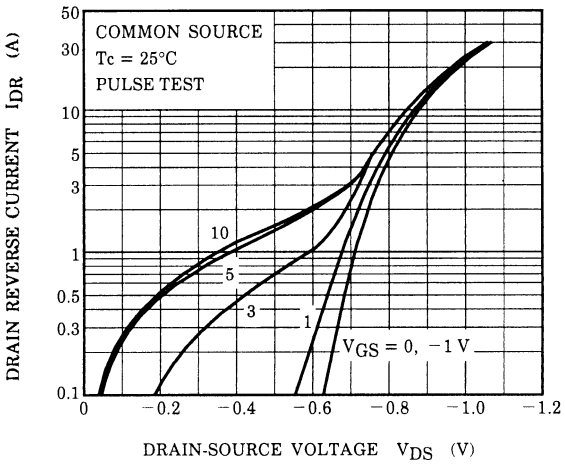
$R_{DS\,(ON)} - I_D$



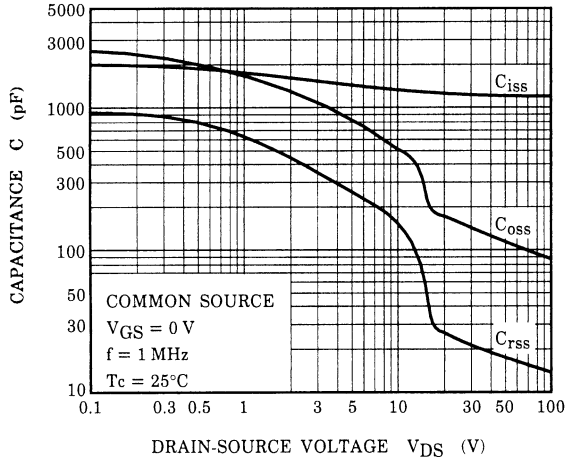
$R_{DS\,(ON)}$ – Tc



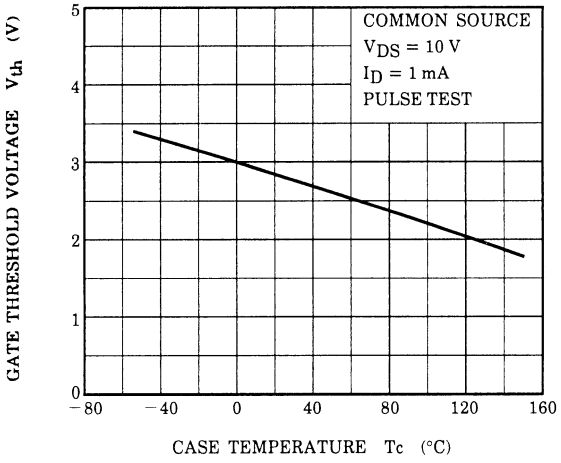
I_{DR} – V_{DS}



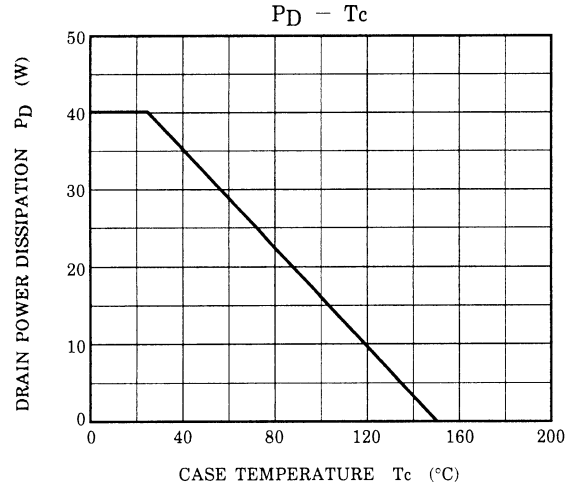
CAPACITANCE – V_{DS}



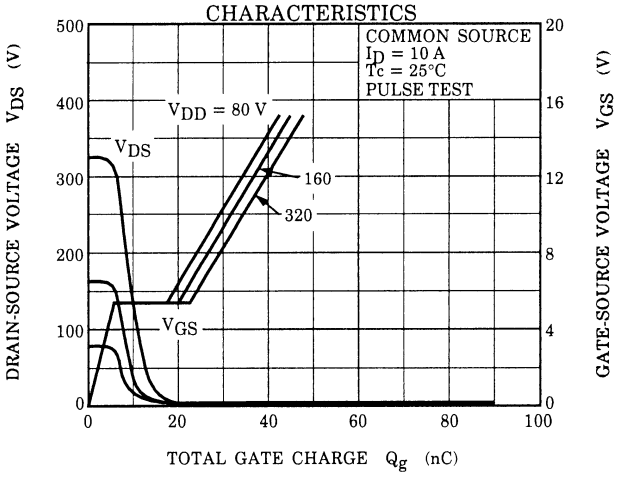
V_{th} – Tc



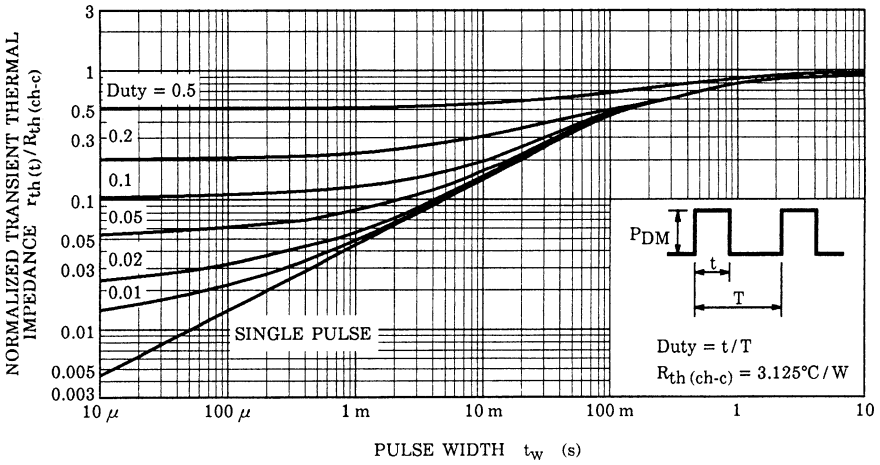
P_D – Tc



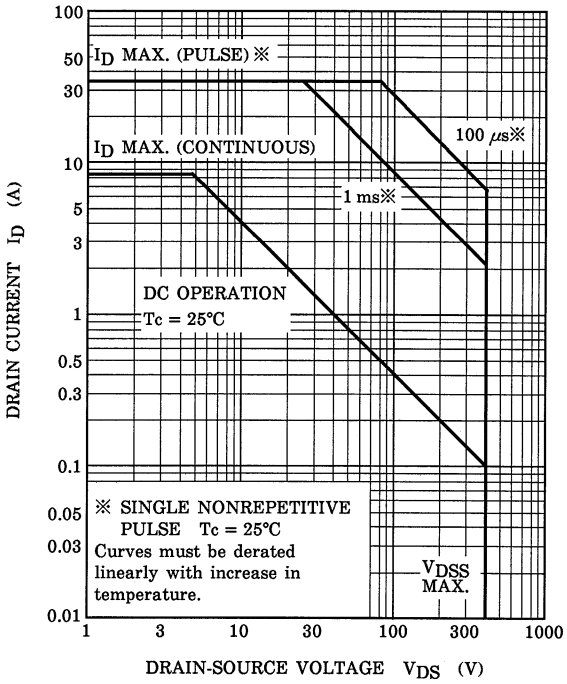
DYNAMIC INPUT / OUTPUT CHARACTERISTICS



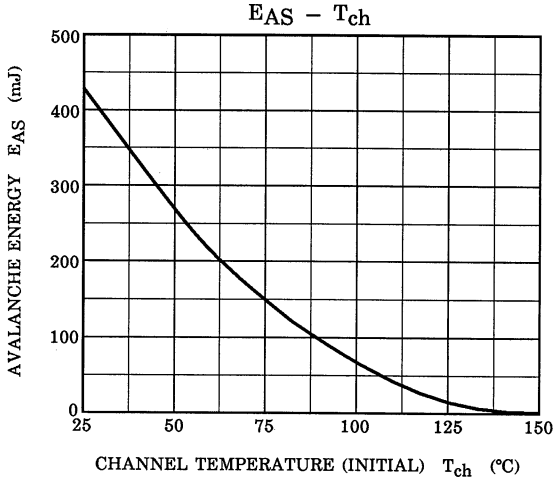
r_{th} – t_w

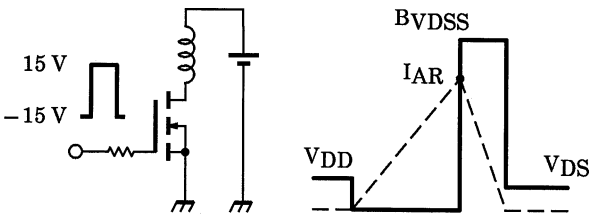


SAFE OPERATING AREA



E_{AS} – T_{ch}





TEST CIRCUIT WAVE FORM

R_G = 25 Ω
V_{DD} = 90 V, L = 9.6 mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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