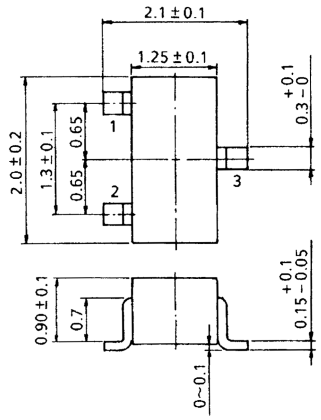
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

2SK2034

High Speed Switching Applications
Analog Switch Applications

- High input impedance.
- Low gate threshold voltage.: V_{th} = 0.5~1.5 V
- Excellent switching times: t_{on} = 0.16 μs (typ.)
  t_{off} = 0.15 μs (typ.)
- Small package.
- Enhancement-mode

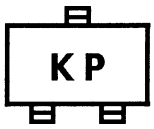
Unit: mm



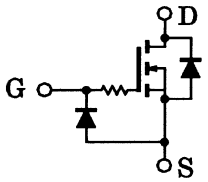
JEDEC	—
JEITA	SC-70
TOSHIBA	2-2E1E

Weight: 0.006 g (typ.)

Marking



Equivalent Circuit



Maximum Ratings (Ta = 25°C)

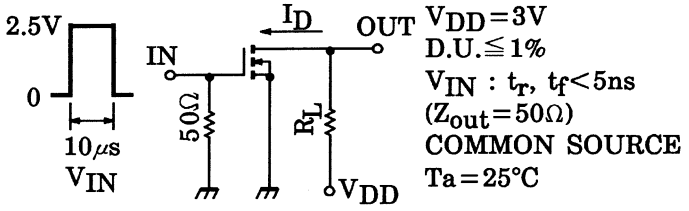
Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DS}	20	V
Gate-source voltage	V_{GSS}	10	V
DC drain current	I_D	100	mA
Drain power dissipation	P_D	100	mW
Channel temperature	T_{ch}	150	°C
Storage temperature range	T_{stg}	−55~150	°C

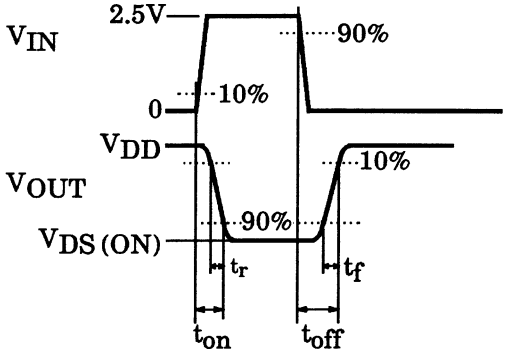
Note: This transistor is electrostatic sensitive device. Please handle with caution.

Electrical Characteristics (Ta = 25°C)

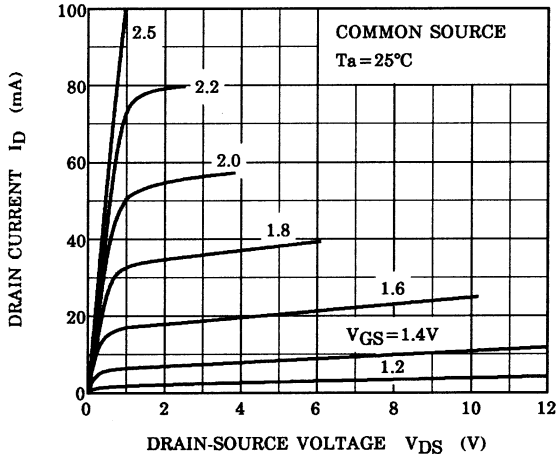
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = 10 V, V_{DS} = 0	—	—	1	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 100 μA, V_{GS} = 0	20	—	—	V
Drain cut-off current		I_{DSS}	V_{DS} = 20 V, V_{GS} = 0	—	—	1	μA
Gate threshold voltage		V_{th}	V_{DS} = 3 V, I_D = 0.1 mA	0.5	—	1.5	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 3 V, I_D = 10 mA	25	50	—	mS
Drain-source ON resistance		$R_{DS\ (ON)}$	I_D = 10 mA, V_{GS} = 2.5 V	—	8	12	Ω
Input capacitance		C_{iss}	V_{DS} = 3 V, V_{GS} = 0, f = 1 MHz	—	8.5	—	pF
Reverse transfer capacitance		C_{rss}	V_{DS} = 3 V, V_{GS} = 0, f = 1 MHz	—	3.3	—	pF
Output capacitance		C_{oss}	V_{DS} = 3 V, V_{GS} = 0, f = 1 MHz	—	9.3	—	pF
Switching time	Turn-on time	t_{on}	V_{DD} = 3 V, I_D = 10 mA V_{GS} = 0~2.5 V	—	0.16	—	μs
	Turn-off time	t_{off}	V_{DD} = 3 V, I_D = 10 mA V_{GS} = 0~2.5 V	—	0.15	—	

Switching Time Test Circuit

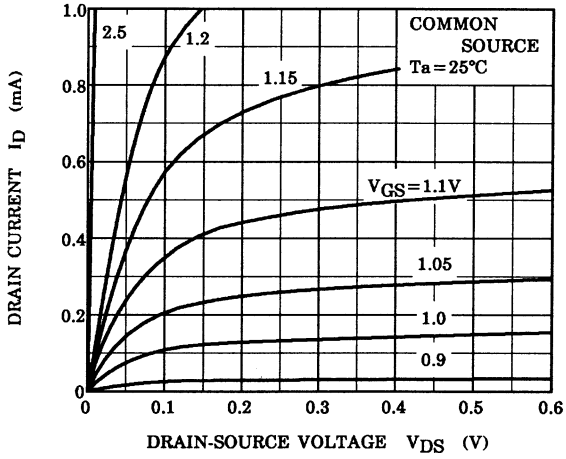




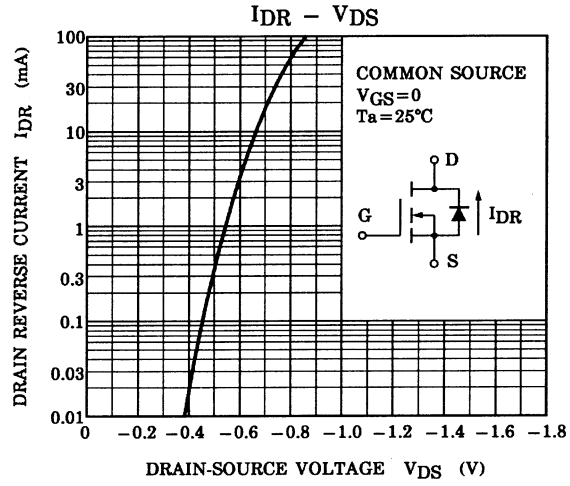
I_D – V_{DS}



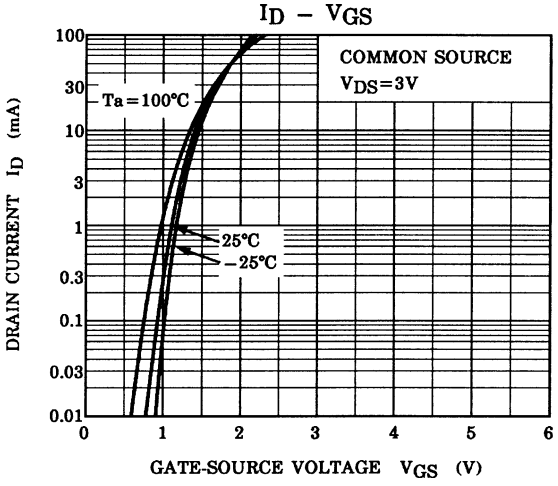
I_D – V_{DS} (LOW VOLTAGE REGION)



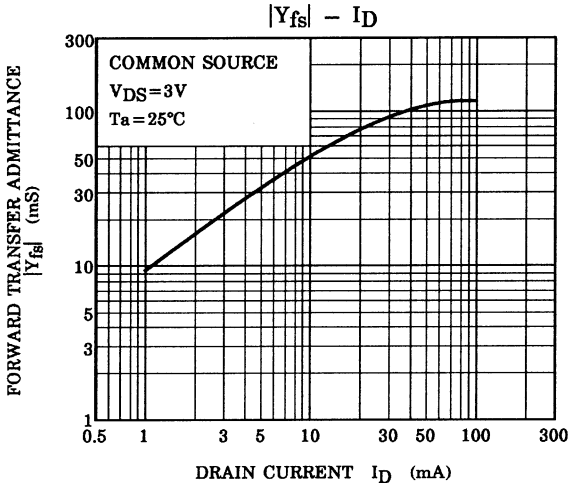
I_{DR} – V_{DS}



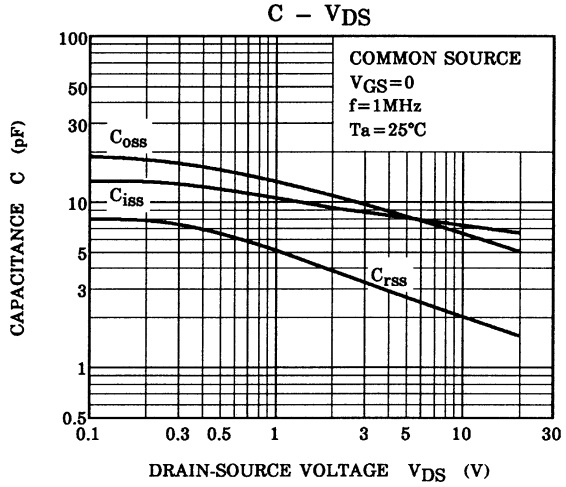
I_D – V_{GS}



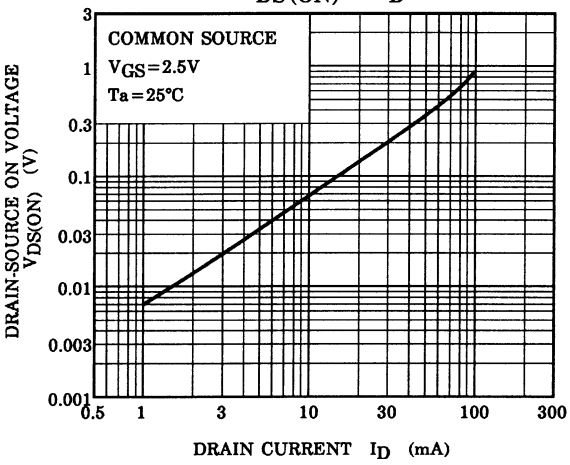
$|Y_{fs}|$ – I_D



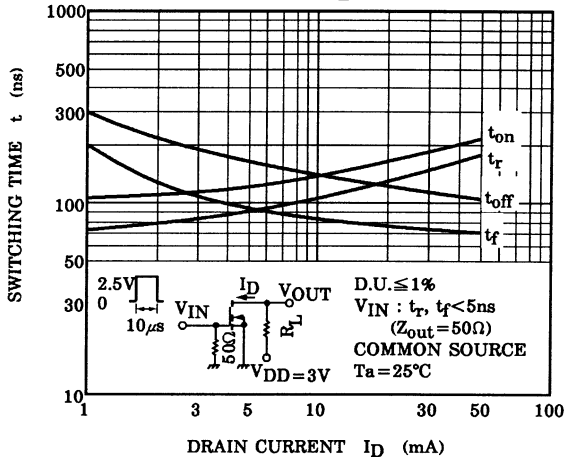
C – V_{DS}



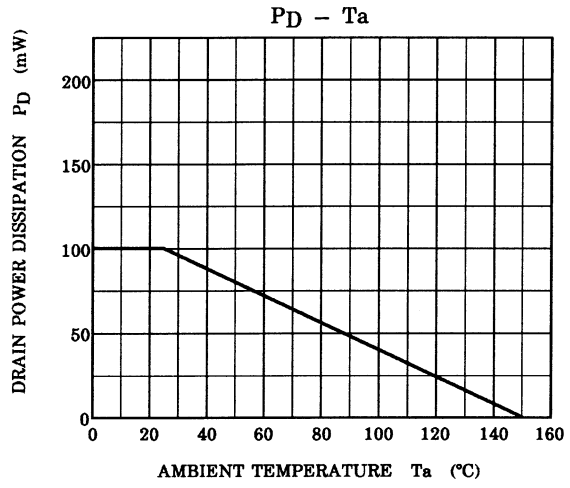
$V_{DS\,(ON)}$ – I_D



t – I_D



P_D – Ta



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