#### TOSHIBA TRANSISTOR SILICON NPN TRIPLE DIFFUSED MESA TYPE

# 2SD2539

### HORIZONTAL DEFLECTION OUTPUT FOR COLOR TV

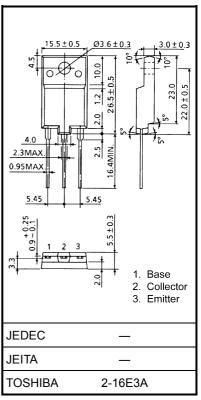
Unit: mm

Bult-in Damper Type

• Collector Metal (Fin) is Fully Covered with Mold Resin.

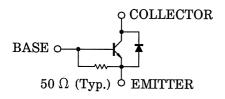
## **MAXIMUM RATINGS (Tc = 25°C)**

CHARACTERISTIC		SYMBOL	RATING	UNIT	
Collector-Base Voltage		$V_{CBO}$	1500	V	
Collector-Emitter Voltage		V <sub>CEO</sub>	600	V	
Emitter-Base Voltage		V <sub>EBO</sub>	5	V	
Collector Current	DC	Ic	7	A	
	Pulse	I <sub>CP</sub>	14		
Base Current		Ι <sub>Β</sub>	3.5	Α	
Collector Power Dissipation		PC	50	W	
Junction Temperature		Tj	150	°C	
Storage Temperature Range		T <sub>stg</sub>	-55~150	°C	



Weight: 5.5 g (typ.)

## **EQUIVALENT CIRCUIT**

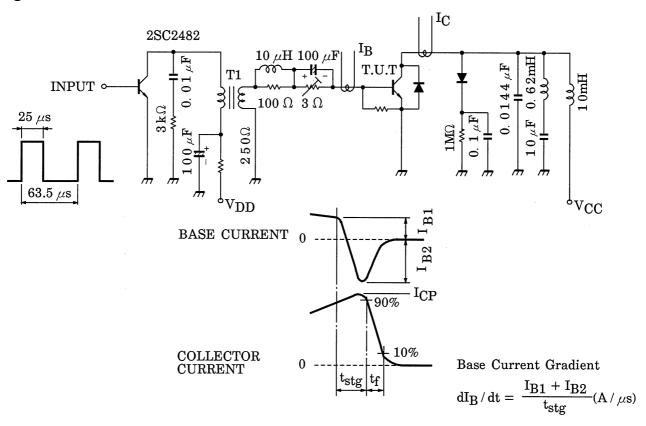


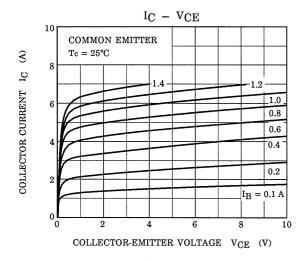
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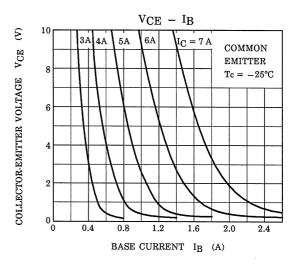
## **ELECTRICAL CHARACTERISTICS (Tc = 25°C)**

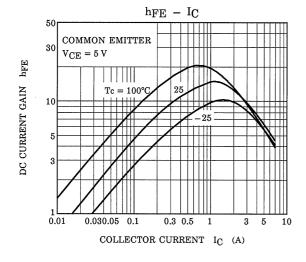
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Collector Cut-off Current		I <sub>CBO</sub>	V <sub>CB</sub> = 1500 V, I <sub>E</sub> = 0	_	_	1	mA
Emitter Cut-off Current		I <sub>EBO</sub>	V <sub>EB</sub> = 5 V, I <sub>C</sub> = 0	66	_	200	mA
Emitter-Base Breakdown Voltage		V <sub>(BR) EBO</sub>	I <sub>C</sub> = 400 mA, I <sub>B</sub> = 0	5	_	_	٧
DC Current Gain		h <sub>FE (1)</sub>	V <sub>CE</sub> = 5 V, I <sub>C</sub> = 1 A	8	_	28	_
		h <sub>FE (2)</sub>	V <sub>CE</sub> = 5 V, I <sub>C</sub> = 5A	5	_	9	
Collector-Emitter Saturation Voltage		V <sub>CE</sub> (sat)	I <sub>C</sub> = 5 A, I <sub>B</sub> = 1.0 A	_	_	5	V
Base-Emitter Saturation Voltage		V <sub>BE (sat)</sub>	I <sub>C</sub> = 5 A, I <sub>B</sub> = 1.0 A	_	1.0	1.3	V
Forward Voltage (Damper Diode)		V <sub>F</sub>	I <sub>F</sub> = 5 A	_	1.6	2.0	٧
Transition Frequency		f <sub>T</sub>	V <sub>CE</sub> = 10 V, I <sub>C</sub> = 0.1 A	_	2	_	MHz
Collector Output Capacitance		C <sub>ob</sub>	V <sub>CB</sub> = 10 V, I <sub>E</sub> = 0, f = 1 MHz	_	115	_	pF
Switching Time	Storage Time	t <sub>stg</sub>	I <sub>CP</sub> = 5 A, I <sub>B1</sub> (end) = 1.0 A f <sub>H</sub> = 15.75 kHz	_	6	9	μs
	Fall Time	t <sub>f</sub>		_	0.3	0.6	

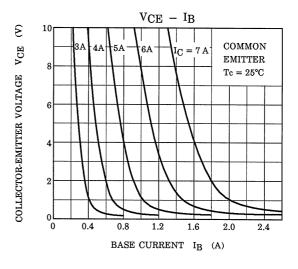
Fig.1 SWITCHING TIME TEST CIRCUIT

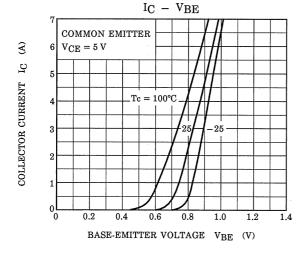


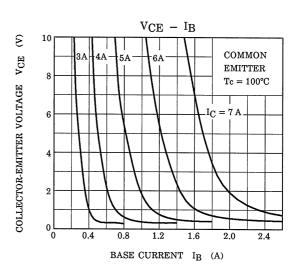


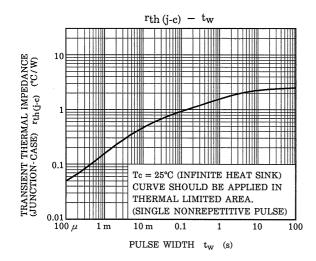


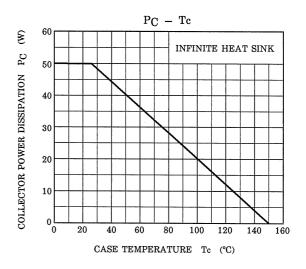


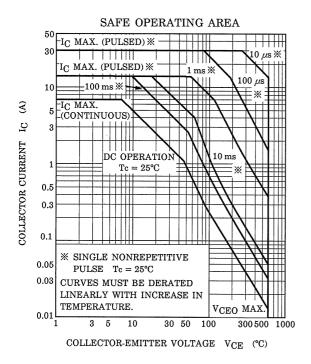












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