# **High-Current Complementary Silicon Power Transistors**

- . . . designed for use in high–power amplifier and switching circuit applications.
- High Current Capability I<sub>C</sub> Continuous = 50 Amperes.
- DC Current Gain -

hFE = 15-60 @ IC = 25 Adc

 Low Collector–Emitter Saturation Voltage — VCE(sat) = 1.0 Vdc (Max) @ I<sub>C</sub> = 25 Adc

### **MAXIMUM RATINGS (1)**

Rating	Symbol	2N5685	2N5684 2N5686	Unit
Collector–Emitter Voltage	VCEO	60	80	Vdc
Collector–Base Voltage	VCB	60	80	Vdc
Emitter-Base Voltage	VEB	5.0		Vdc
Collector Current — Continuous	IC	50		Adc
Base Current	ΙΒ	15		Adc
Total Device Dissipation @ T <sub>C</sub> = 25°C Derate above 25°C	PD	300 1.715		Watts W/°C
Operating and Storage Junction Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-65 to +200		°C

#### **THERMAL CHARACTERISTICS (1)**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θJC	0.584	°C/W

(1) Indicates JEDEC Registered Data.

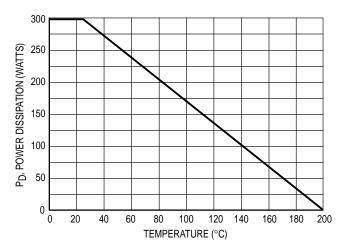


Figure 1. Power Derating

Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

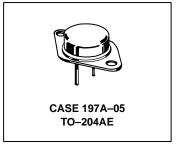
Preferred devices are Motorola recommended choices for future use and best overall value.

#### REV 7

PNP 2N5684 NPN 2N5685 2N5686\*

\*Motorola Preferred Device

50 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60-80 VOLTS
300 WATTS



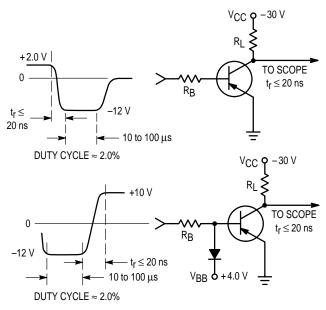


## \*ELECTRICAL CHARACTERISTICS ( $T_C = 25$ °C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (Note 1) (I <sub>C</sub> = 0.2 Adc, I <sub>B</sub> = 0)	2N5685 2N5684, 2N5686	V <sub>CEO(sus)</sub>	60 80	_ _	Vdc
Collector Cutoff Current (V <sub>CE</sub> = 30 Vdc, I <sub>B</sub> = 0) (V <sub>CE</sub> = 40 Vdc, I <sub>B</sub> = 0)	2N5685 2N5684, 2N5686	ICEO	_ _	1.0 1.0	mAdc
Collector Cutoff Current (VCE = 60 Vdc, VEB(off) = 1.5 Vdc) (VCE = 80 Vdc, VEB(off) = 1.5 Vdc) (VCE = 60 Vdc, VEB(off) = 1.5 Vdc, TC = 150°C) (VCE = 80 Vdc, VEB(off) = 1.5 Vdc, TC = 150°C)	2N5685 2N5684, 2N5686 2N5685 2N5684, 2N5686	ICEX	  -  -	2.0 2.0 10 10	mAdo
Collector Cutoff Current (V <sub>CB</sub> = 60 Vdc, I <sub>E</sub> = 0) (V <sub>CB</sub> = 80 Vdc, I <sub>E</sub> = 0)	2N5685 2N5684, 2N5686	ICBO		2.0 2.0	mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0 \text{ Vdc}$ , $I_{C} = 0$ )		I <sub>EBO</sub>	_	5.0	mAdo
ON CHARACTERISTICS					
DC Current Gain (Note 1) ( $I_C = 25$ Adc, $V_{CE} = 2.0$ Vdc) ( $I_C = 50$ Adc, $V_{CE} = 5.0$ Vdc)		hFE	15 5.0	60 —	_
Collector–Emitter Saturation Voltage (Note 1) (I <sub>C</sub> = 25 Adc, I <sub>B</sub> = 2.5 Adc) (I <sub>C</sub> = 50 Adc, I <sub>B</sub> = 10 Adc)		VCE(sat)	_ _	1.0 5.0	Vdc
Base–Emitter Saturation Voltage (Note 1) (I <sub>C</sub> = 25 Adc, I <sub>B</sub> = 2.5 Adc)		V <sub>BE(sat)</sub>		2.0	Vdc
Base–Emitter On Voltage (Note 1) (I <sub>C</sub> = 25 Adc, V <sub>CE</sub> = 2.0 Vdc)		V <sub>BE</sub> (on)	_	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I <sub>C</sub> = 5.0 Adc, V <sub>CE</sub> = 10 Vdc, f = 1.0 MHz)		f <sub>T</sub>	2.0	_	MHz
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 0.1 MHz)	2N5684 2N5685, 2N5686	C <sub>ob</sub>	_ 	2000 1200	pF
Small–Signal Current Gain (I <sub>C</sub> = 10 Adc, V <sub>CE</sub> = 5.0 Vdc, f = 1.0 kHz)		h <sub>fe</sub>	15		

<sup>\*</sup> Indicates JEDEC Registered Data.

Note 1: Pulse Test: Pulse Width  $\leq$  300  $\mu$ s, Duty Cycle  $\leq$  2.0%.



FOR CURVES OF FIGURES 3 & 6, RB & RL ARE VARIED. INPUT LEVELS ARE APPROXIMATELY AS SHOWN. FOR NPN CIRCUITS, REVERSE ALL POLARITIES.

Figure 2. Switching Time Test Circuit

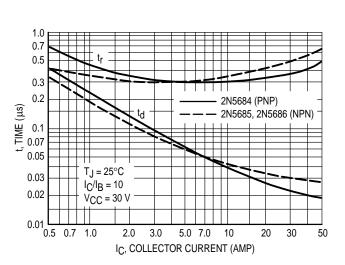


Figure 3. Turn-On Time

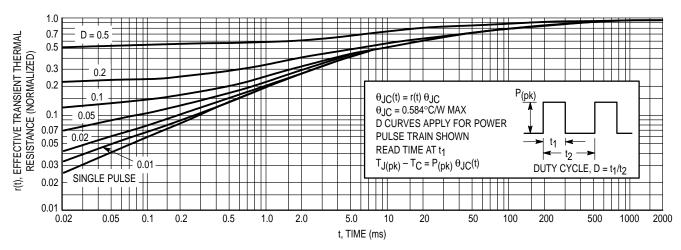


Figure 4. Thermal Response

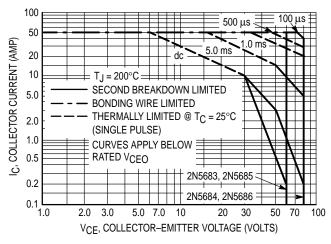


Figure 5. Active-Region Safe Operating Area

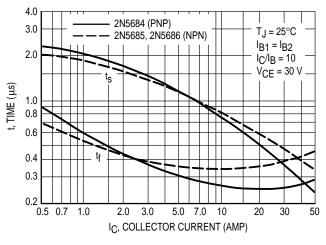


Figure 6. Turn-Off Time

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I<sub>C</sub> – V<sub>CE</sub> limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 200^{\circ}C$ ;  $T_{C}$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \le 200^{\circ}C$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

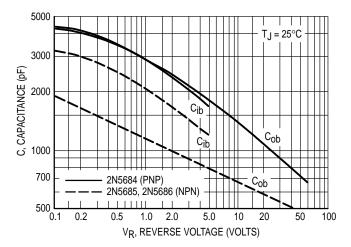


Figure 7. Capacitance

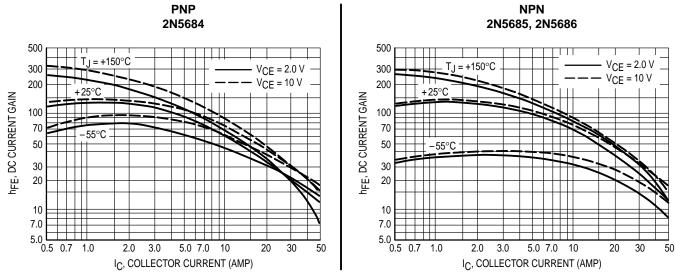


Figure 8. DC Current Gain

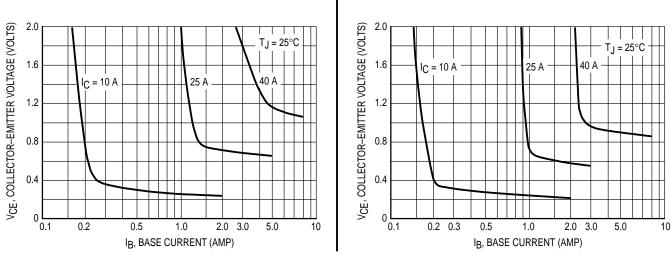


Figure 9. Collector Saturation Region

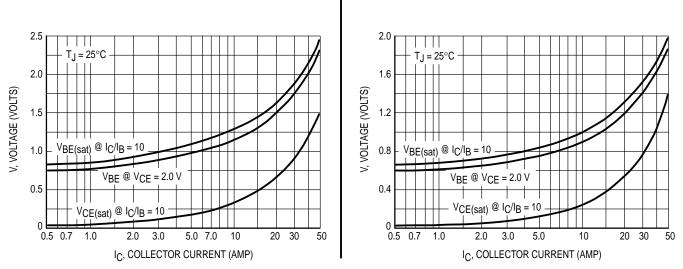
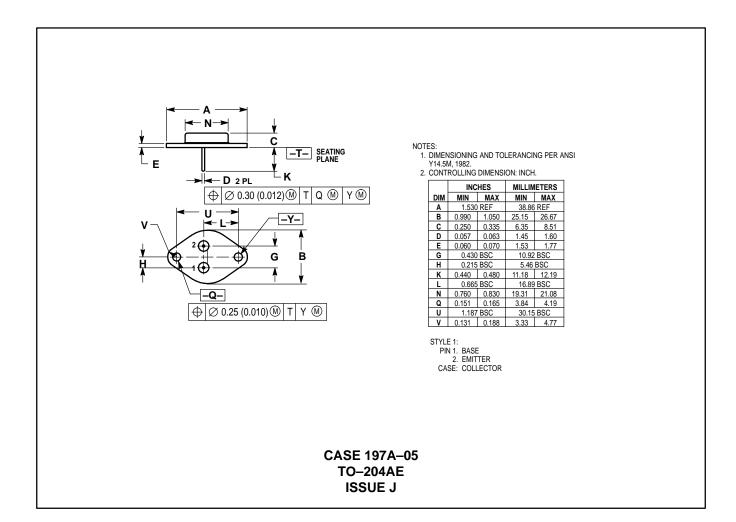


Figure 10. "On" Voltages

#### **PACKAGE DIMENSIONS**



#### 2N5684 2N5685 2N5686

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How to reach us:

**USA/EUROPE**: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE (602) 244–6609 INTERNET: http://Design-NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, Toshikatsu Otsuki, 6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-3521-8315

**HONG KONG:** Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298



