2N4347
(See 2N3442)

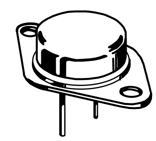
PNP Silicon High-Power Transistors

. . . designed for use in power amplifier and switching circuits.

- Low Collector–Emitter Saturation Voltage —
  I_C = 15 Adc, $V_{CE(sat)}$ = 1.0 Vdc (Max) 2N4398,99
  = 1.5 Vdc (Max) 2N5745
- DC Current Gain Specified — 1.0 to 30 Adc
- Complements to NPN 2N5301, 2N5302, 2N5303

2N4398
2N4399
2N5745

20, 30 AMPERE
POWER TRANSISTORS
PNP SILICON
40–60–180 VOLTS
200 WATTS



CASE 1–07
TO–204AA
(TO–3)

*MAXIMUM RATINGS

Rating	Symbol	2N4398	2N4399	2N5745	Unit
Collector–Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector–Base Voltage	V_{CB}	40	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	30 50	30 50	20 50	Adc
Base Current — Continuous Peak	I_B	7.5 15			Adc
Total Device Dissipation @ T_A = 25°C** Derate above 25°C	P_D	5.0 28.6			Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.15			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	35	°C/W

* Indicates JEDEC Registered Data.
** Motorola guarantees this data in addition to JEDEC Registered Data.

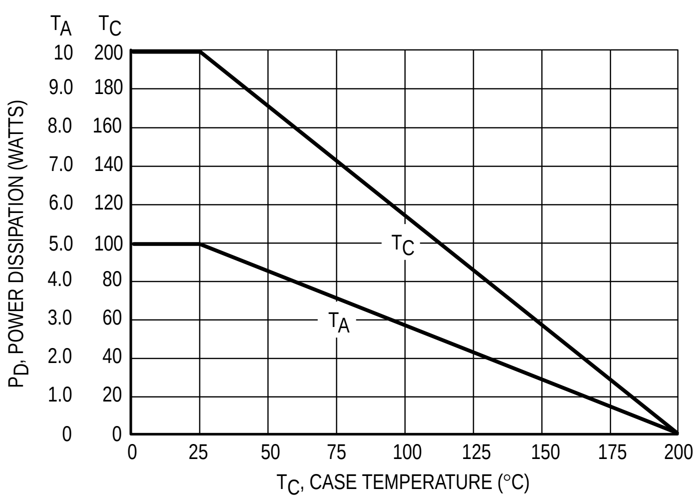


Figure 1. Power–Temperature Derating Curve

Safe Area Curves are indicated by Figure 13. All limits are applicable and must be observed.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	2N4398	$V_{CEO(sus)}$	40	—	Vdc
	2N4399		60	—	
	2N5745		80	—	
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0)	2N4398	I_{CEO}	—	5.0	mAdc
(V_{CE} = 60 Vdc, I_B = 0)	2N4399		—	5.0	
(V_{CE} = 80 Vdc, I_B = 0)	2N5745		—	5.0	
Collector Cutoff Current (V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N4398	I_{CEX}	—	5.0	mAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N4399		—	5.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5745		—	5.0	
(V_{CE} = 30 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N4398, 2N4399		—	10	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5745		—	10	
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0)	2N4398	I_{CBO}	—	1.0	mAdc
(V_{CB} = 60 Vdc, I_E = 0)	2N4399		—	1.0	
(V_{CB} = 80 Vdc, I_E = 0)	2N5745		—	1.0	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	All Types	h_{FE}	40	—	—
(I_C = 10 Adc, V_{CE} = 2.0 Vdc)	2N5745		15	60	
(I_C = 15 Adc, V_{CE} = 2.0 Vdc)	2N4398, 2N4399		15	60	
(I_C = 20 Adc, V_{CE} = 2.0 Vdc)	2N5745		5.0	—	
(I_C = 30 Adc, V_{CE} = 4.0 Vdc)	2N4398, 2N4399		5.0	—	
Collector–Emitter Saturation Voltage (1) (I_C = 10 Adc, I_B = 1.0 Adc)	2N4398, 2N4399	$V_{CE(sat)}$	—	0.75	Vdc
	2N5745		—	1.0	
(I_C = 15 Adc, I_B = 1.5 Adc)	2N4398, 2N4399		—	1.0	
	2N5745		—	1.5	
(I_C = 20 Adc, I_B = 2.0 Adc)	2N4398, 2N4399		—	2.0	
(I_C = 20 Adc, I_B = 4.0 Adc)	2N5745		—	2.0	
(I_C = 30 Adc, I_B = 6.0 Adc)	2N4398, 2N4399		—	4.0	
Base–Emitter Saturation Voltage (1) (I_C = 10 Adc, I_B = 1.0 Adc)**	2N4398, 2N4399	$V_{BE(sat)}$	—	1.6	Vdc
	2N5745		—	1.7	
(I_C = 15 Adc, I_B = 1.5 Adc)	2N4398, 2N4399		—	1.85	
	2N5745		—	2.0	
(I_C = 20 Adc, I_B = 2.0 Adc)**	2N4398, 2N4399		—	2.5	
(I_C = 20 Adc, I_B = 4.0 Adc)	2N5745		—	2.5	
Base–Emitter On Voltage (1) (I_C = 10 Adc, V_{CE} = 2.0 Vdc)	2N5745	$V_{BE(on)}$	—	1.5	Vdc
(I_C = 15 Adc, V_{CE} = 2.0 Vdc)	2N4398, 2N4399		—	1.7	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)	2N5745		—	2.5	
(I_C = 30 Adc, V_{CE} = 4.0 Vdc)	2N4398, 2N4399		—	3.0	

* Indicates JEDEC Registered Data.

(continued)

** Motorola Guarantees this Data in Addition to JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

ELECTRICAL CHARACTERISTICS — continued

Characteristic		Symbol	Min	Max	Unit
DYNAMIC CHARACTERISTICS					
Current–Gain Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	2N4398, 2N4399 2N5745	f_T	4.0 2.0	— —	MHz
Small–Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	40	—	—
SWITCHING CHARACTERSTICS					
Rise Time (V_{CC} = 30 Vdc, I_C = 10 Adc, $I_{B1} = I_{B2}$ = 1.0 Adc)	2N4398, 2N4399 2N5745	t_r	— —	0.4 1.0	µs
Storage Time (V_{CC} = 30 Vdc, I_C = 10 Adc, $I_{B1} = I_{B2}$ = 1.0 Adc)	2N4396, 2N4399 2N5745	t_s	— —	1.5 2.0	µs
Fall Time (V_{CC} = 30 Vdc, I_C = 10 Adc, $I_{B1} = I_{B2}$ = 1.0 Adc)	2N4398, 2N4399 2N5746	t_f	— —	0.6 1.0	µs

(2) f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

SWITCHING TIME EQUIVALENT TEST CIRCUITS

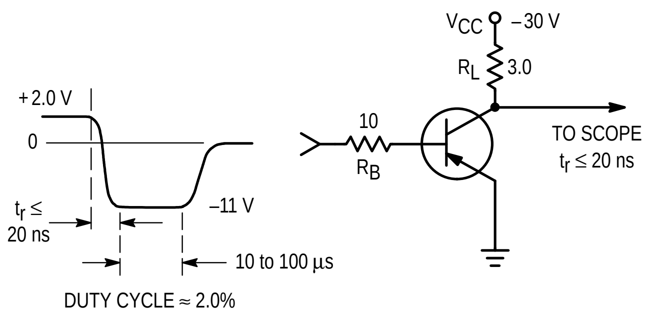


Figure 2. Turn–On Time

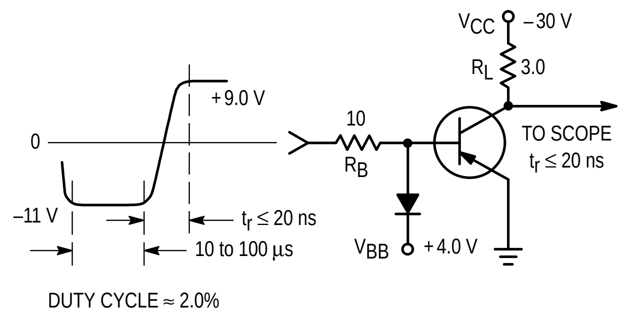


Figure 3. Turn–Off Time

TYPICAL "ON" REGION CHARACTERISTICS

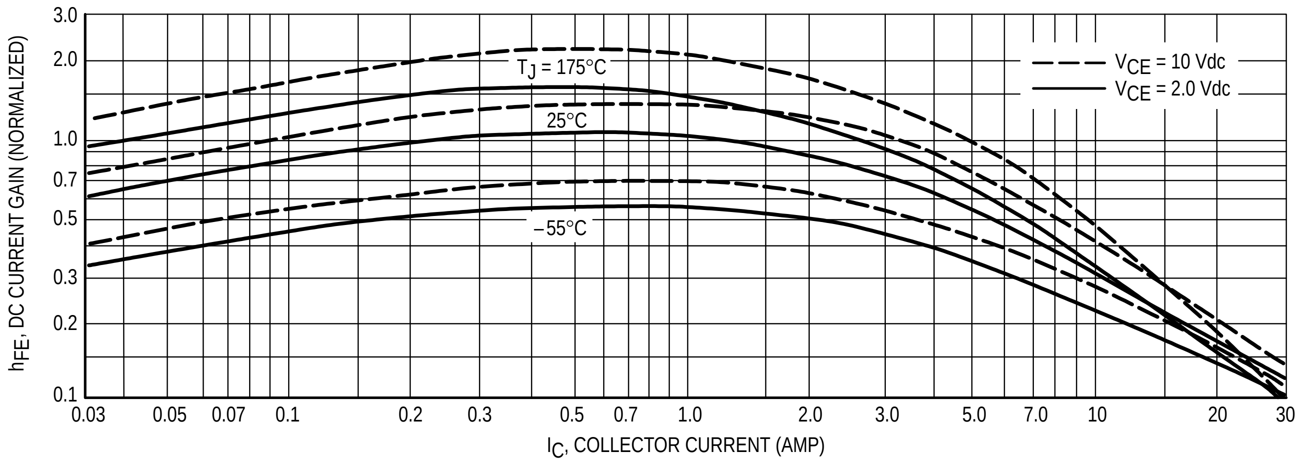


Figure 4. DC Current Gain

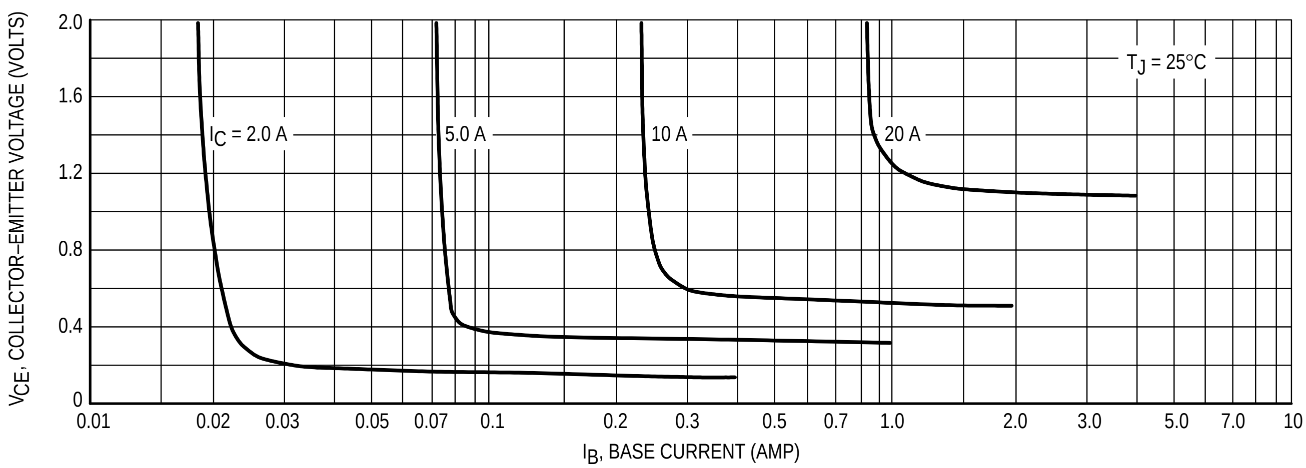


Figure 5. Collector Saturation Region

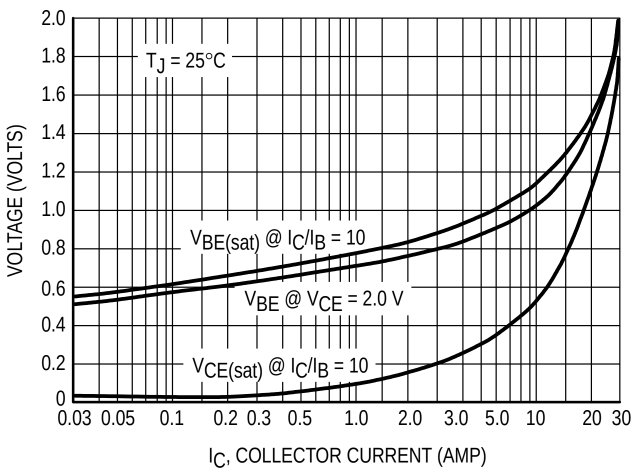


Figure 6. "On" Voltages

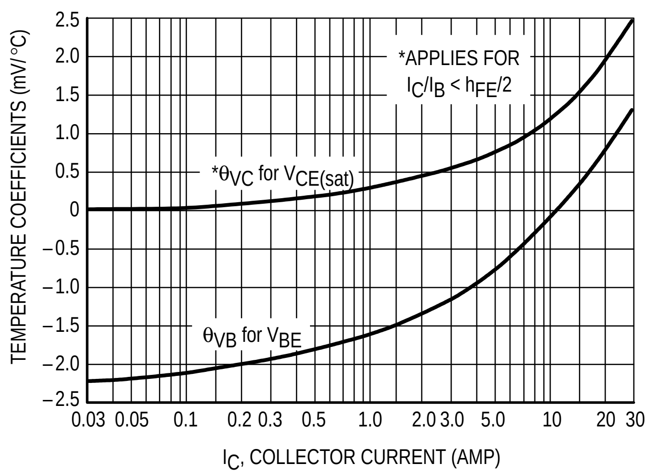


Figure 7. Temperature Coefficients

RATINGS AND THERMAL DATA

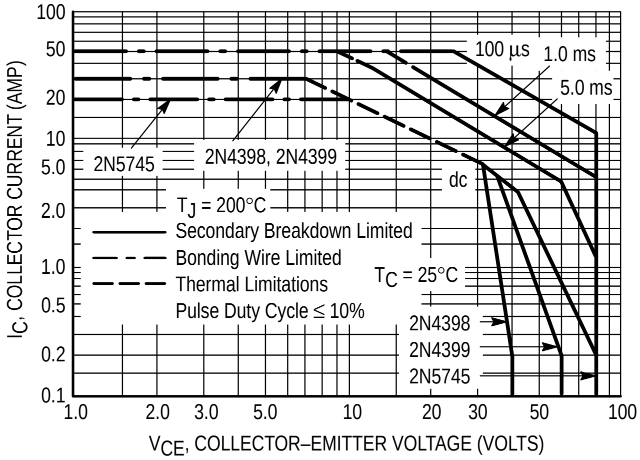


Figure 8. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 8 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ ≤ 200°C. $T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

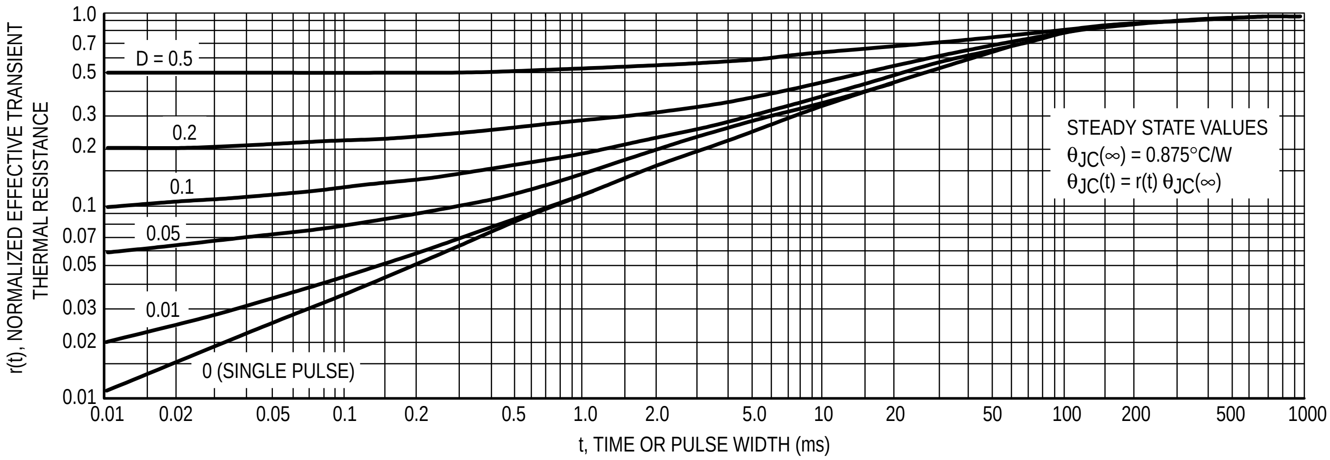
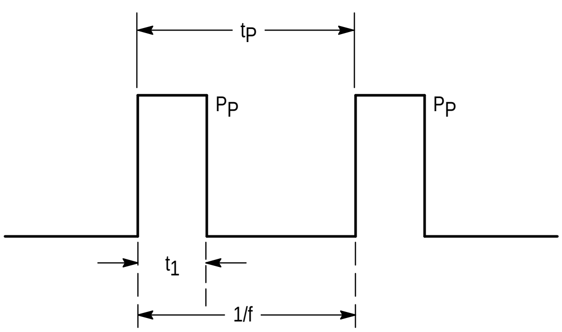


Figure 9. Thermal Response

DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA



DUTY CYCLE, $D = t_1 f - \frac{t_1}{t_P}$

PEAK PULSE POWER = P_P

A train of periodical power pulses can be represented by the model as shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 9 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 9 by the steady state value $\theta_{JC}(\infty)$.

Example:

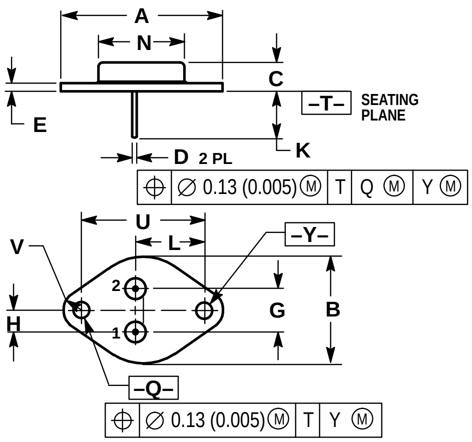
The 2N4398 is dissipating 100 watts under the following conditions: t_1 = 1.0 ms, t_P = 5.0 ms. (D = 0.2)

Using Figure 9, at a pulse width of 1.0 ms and D = 0.2, the reading of r (t) is 0.28.

The peak rise in junction temperature is therefore

$$T = r(t) \times P_P \times \theta_{JC}(\infty) = 0.28 \times 100 \times 0.875 = 24.5°C$$

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO–204AA OUTLINE SHALL APPLY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	—	1.050	—	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	—	0.830	—	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

CASE 1–07
TO–204AA (TO–3)
ISSUE Z

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