

## Standard EEPROM ICs

SLx 25C010

1 KBit (128 × 8 bit)

Serial CMOS-EEPROM with

Serial Peripheral Interface (SPI) Synchronous Bus

<b>SLx 25C010</b>		
<b>Revision History:</b>		<b>Current Version: Preliminary 1999-03-15</b>
Previous Version:		
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
7	7	Figure 2 has changed
14	14	Figure 7 has changed

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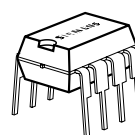
## 1 KBit (128 × 8 bit) Serial CMOS EEPROMs, Serial Peripheral Interface (SPI) Synchronous Bus

SLx 25C010

### Preliminary

#### Features

- **Serial peripheral interface (SPI) compatible, supports SPI Modes 0,0 and 1,1**
- **Page Protection Mode™** for protecting the EEPROM against unintended data changes (SLx 25C010.../P types only)
- **Low power CMOS**
- **Clock frequency up to 2.1 MHz**
- **$V_{CC} = 2.7$  to 5.5 V operation**
- **8-byte page mode**
- **Write protect ( $\overline{WP}$ ) pin and write disable instruction for both hardware and software data protection**
- **Block write protection**
  - Protect entire array
- **Filtered inputs for noise suppression with Schmitt trigger**
- **High programming flexibility**
  - Internal programming voltage
  - Self timed write cycle including erase (5 ms typical) for up to 8 bytes
  - Byte-write and page-write programming, between 1 and 8 bytes
- **High reliability**
  - Endurance  $10^6$  cycles<sup>1)</sup>
  - Data retention 40 years<sup>1)</sup>
  - ESD protection > 4000 V on all pins
- **8 pin DIP/DSO packages**
- **Available for extended temperature ranges**
  - Industrial:                    – 40 °C to + 85 °C
  - Automotive:                – 40 °C to + 125 °C  
    (– 40 °C to +150 °C on request)



P-DIP-8-3



P-DSO-8-2

<sup>1)</sup> Values are temperature dependent, for further information please refer to your Siemens sales office.

## Ordering Information

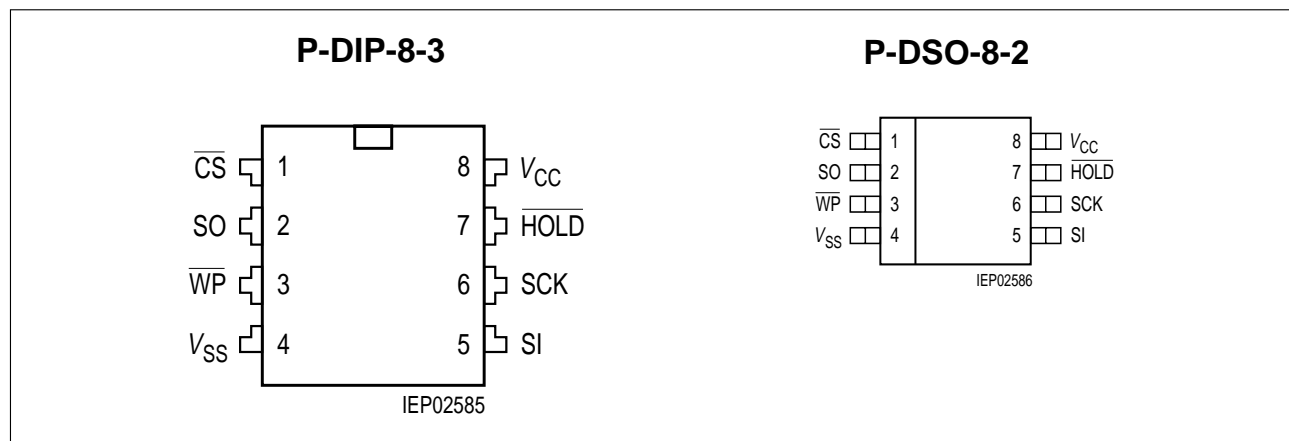
**Table 1**

Type	Ordering Code	Package	Temperature	Voltage
SLA 25C010-D SLA 25C010-D/P	on request	P-DIP-8-3	– 40 °C ... + 85 °C	2.7 V ... 5.5 V
SLA 25C010-S SLA 25C010-S/P	on request	P-DSO-8-2	– 40 °C ... + 85 °C	2.7 V ... 5.5 V
SLE 25C010-D SLE 25C010-D/P	on request	P-DIP-8-3	– 40 °C ... + 125 °C	2.7 V ... 5.5 V
SLE 25C010-S SLE 25C010-S/P	on request	P-DSO-8-2	– 40 °C ... + 125 °C	2.7 V ... 5.5 V

Other types are available on request:

- Temperature range (– 40 °C ... + 150 °C)
- Packages (TSSOP-8, die, wafer delivery)

## 1 Pin Configuration



**Figure 1**  
Pin Configuration (top view)

**Table 2**  
Pin Definitions and Functions

Pin No.	Symbol	Function
1	$\overline{\text{CS}}$	Chip select input
2	SO	Serial output
3	$\overline{\text{WP}}$	Write protection input

**Table 2**  
**Pin Definitions and Functions (cont'd)**

Pin No.	Symbol	Function
4	$V_{SS}$	Ground
5	SI	Serial input
6	SCK	Serial clock input
7	$\overline{\text{HOLD}}$	Hold input
8	$V_{CC}$	Supply voltage

## Pin Description

### Serial Input (SI)

The SI pin is an input and used to clock all instructions, byte addresses and data into the device. Input data is latched on the rising edge of the serial clock.

### Serial Output (SO)

The SO pin is an output and used to shift data out of the device. Data is clocked out by the falling edge of the serial clock.

### Serial Clock (SCK)

The SCK pin is an input and used to synchronize the communication between the master and the EEPROM.

### Chip Select ( $\overline{\text{CS}}$ )

The  $\overline{\text{CS}}$  pin is an input and used to enable or disable the device. When the  $\overline{\text{CS}}$  pin is low, the device is enabled. When the  $\overline{\text{CS}}$  pin is high, the device is disabled and, if no internal programming cycle is in process, forced into the standby mode.

After power up, a high-to-low transition of the  $\overline{\text{CS}}$  pin is required prior to the start of any operation.

A low-to-high transition of the  $\overline{\text{CS}}$  pin after a valid write or erase command starts an internal programming cycle. Independent of the  $\overline{\text{CS}}$  pin an already started programming cycle will be finished and then the device forced into the standby mode. When the device is deselected, SO goes to the high impedance state, allowing multiple parts to share the same SPI bus.

**Write Protect ( $\overline{\text{WP}}$ )**

The  $\overline{\text{WP}}$  pin is an input and used to enable or disable write operations to the status register and to the entire memory. When the  $\overline{\text{WP}}$  pin is high, write operations to the status register and to the entire memory are allowed. When the  $\overline{\text{WP}}$  pin is low, all write operations to the status register and to the entire memory are disabled.

If the internal programming cycle has already been initiated, a high to low transition of the  $\overline{\text{WP}}$  pin will have no influence on the programming cycle.

**HOLD ( $\overline{\text{HOLD}}$ )**

The  $\overline{\text{Hold}}$  pin is an input. When the device is selected with  $\overline{\text{CS}}$  pin low, the  $\overline{\text{Hold}}$  pin can be used to pause the serial communication with the master and to continue the communication later without resetting the serial sequence.

To pause the communication the  $\overline{\text{Hold}}$  pin must be brought low while the SCK pin is low. Inputs to the SI pin will be ignored and the SO pin is in the high impedance state. SCK may still toggle during  $\overline{\text{Hold}}$ . To continue the communication the  $\overline{\text{Hold}}$  pin must be brought high while the SCK pin is low.

The  $\overline{\text{Hold}}$  pin must be held high any time this function is not being used.

## 2 Description

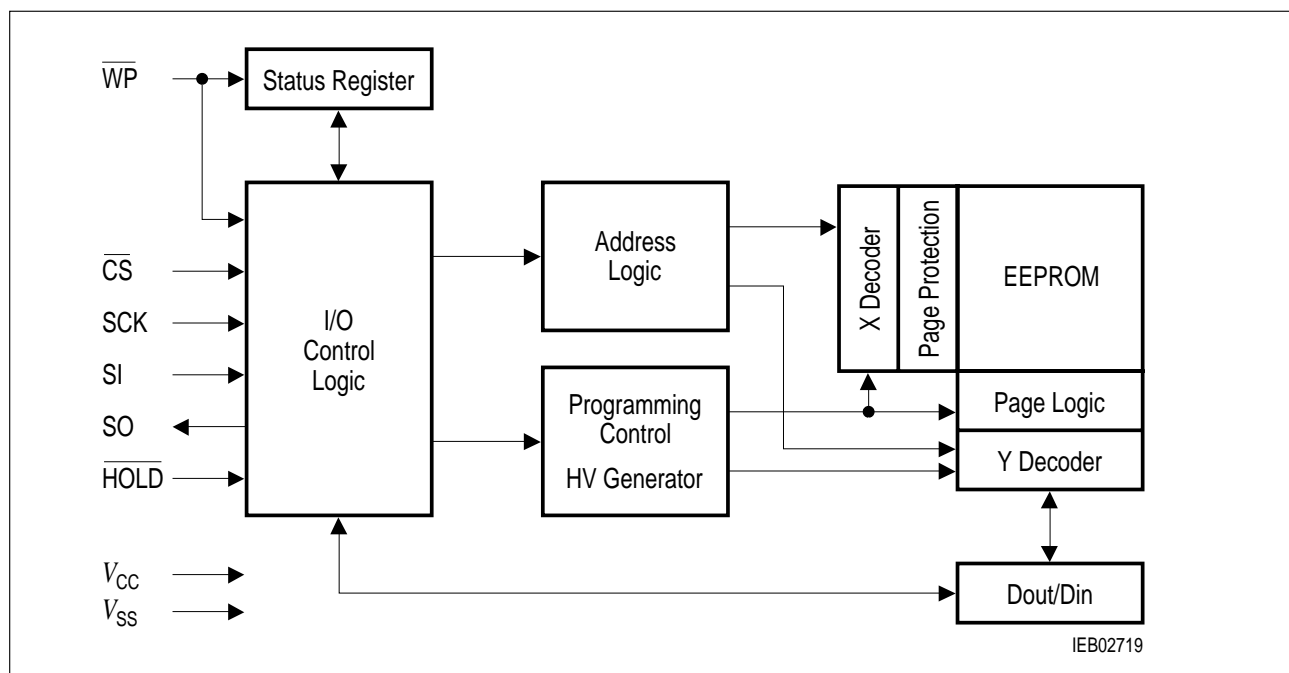
SLx 25C010 is a serial electrically erasable and programmable read only memory (EEPROM), organized as  $128 \times 8$  bit. The data memory is divided into 16 pages. Up to 8 bytes of a page can be programmed simultaneously.

The device is accessed via a Serial Peripheral Interface (SPI) compatible bus (SPI Modes 0,0 and 1,1). The required bus signals are clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through the chip select input ( $\overline{CS}$ ), allowing any number of devices to share the same bus.

For applications with high security requirements against unintended data changes devices with Page Protection Mode™ (SLx 25C010.../P types only, refer to **table 7**) are available.

Low voltage design permits operation down to 2.7 V with low active and standby currents. All devices have a minimum endurance of  $10^6$  erase/write cycles<sup>1)</sup>.

The device operates with a maximum clock frequency of 2.1 MHz, a voltage range of  $V_{CC} = 2.7 \dots 5.5$  V and is available in two temperature ranges for industrial and automotive applications. The device is available in eight-pin DIP and DSO packages; additionally the device may be purchased in die or wafer format.

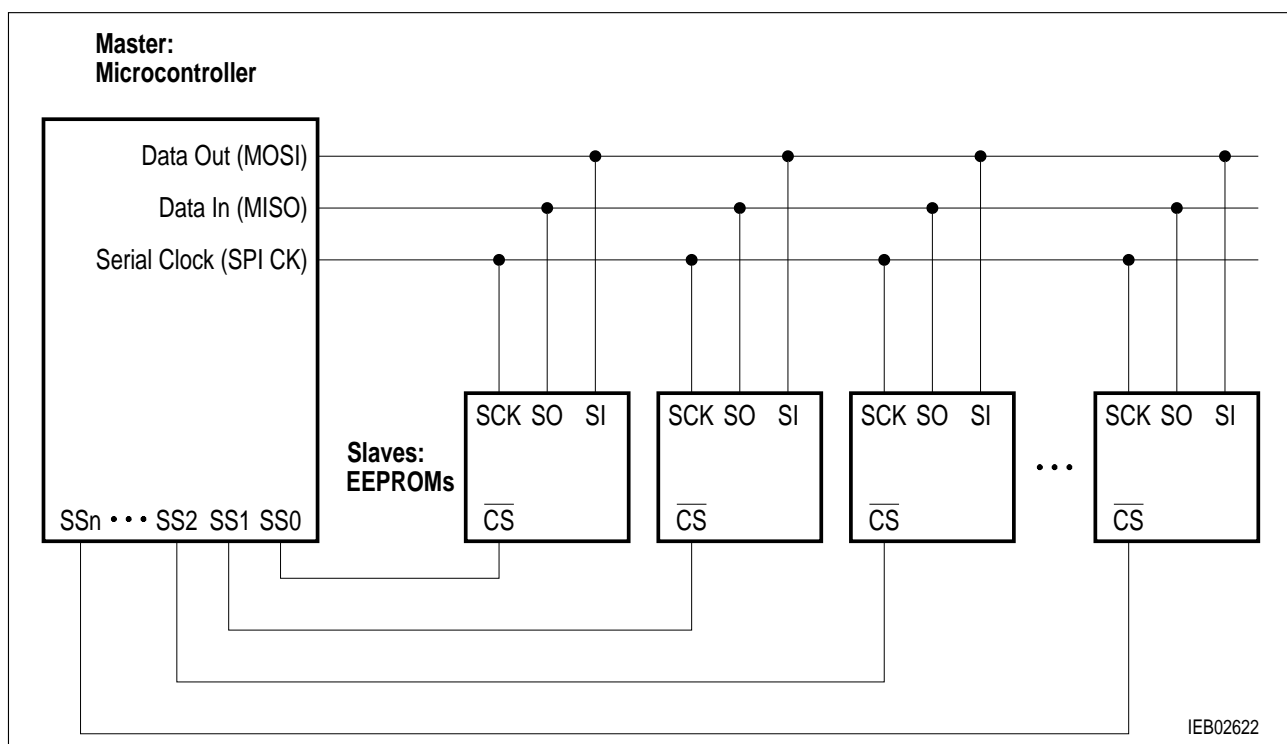


**Figure 2**  
**Block Diagram**

<sup>1)</sup> Values are temperature dependent, for further information please refer to your Siemens sales office.

## 3 SPI Bus Characteristics

Access to the SLx 25C010 device is given via the SPI bus. This bus consists of three wires: SCK for clock, SI for input data from the master to the device and SO for output data from the device to the master. The protocol is master/slave oriented, where the serial EEPROM always takes the role of a slave. The device is selected via the  $\overline{CS}$  pin.



**Figure 3**  
**Bus Configuration**

<b>Master</b>	<p>Device that initiates the transfer of data and provides the clock for transmit and receive operations.</p> <p>MOSI = Master Output Slave Input</p> <p>MISO = Master Input Slave Output</p>
<b>Slave</b>	<p>Device addressed by the master, capable of receiving and transmitting data.</p>
<b>Transmitter/Receiver</b>	<p>The SLx 25C010 has separate pins for data transmission (SO) and reception (SI).</p>



<b>SPI Modes 0,0 and 1,1</b>	SPI modes 0,0 and 1,1 means for the slave that the input data is latched on the rising edge of the serial clock and the output data clocked out by the falling edge of the serial clock.
<b>MSB</b>	The Most Significant Bit (MSB) is the first bit transmitted and received.
<b>Invalid instruction</b>	If an invalid instruction is received, the data will be ignored by the device, and the serial output pin (SO) will remain in a high impedance state until the falling edge of $\overline{CS}$ is detected again. This will reinitialize the serial communication.

#### 4 Status Register

SLx 25C010 has a status register that indicating the actual status of the device. Read operations are allowed to all bits of the status register via the command byte RDSR (Read Status Register), whereas write operations are only allowed to bit 2 and 3 (BP0, BP1) via the command byte WRSR (Write Status Register).

Bit 1 (WEL) indicates whether the device is enabled or disabled for write operations. Its status can only be changed via the command bytes WREN (Write Enable, bit 1 = “1”) and WRDI (Write Disable, bit 1 = “0”). All write operations to the status register *and* to the entire memory has to be preceded by the command byte WREN.

The definition of the status register is shown in **table 3**.

**Table 3**  
**Definition of the Status Register**

Bit	Name	Definition
0	WIP	<u>W</u> rite <u>I</u> n <u>P</u> rocess: “0” indicates the device is ready. “1” indicates that a programming cycle is in process. (bit 0: read only)
1	WEL	<u>W</u> rite <u>E</u> nable <u>L</u> atches: “0” indicates the device is <i>not</i> enabled for write operations. “1” indicates the device is enabled for write operations (bit 1: read only).
2	BP0	The <u>B</u> lock <u>P</u> rotect <u>B</u> its indicate which blocks are currently write protected (see <b>table 6</b> ) (bits 2/3: read/write).
3	BP1	
4	x	These bits are not used and always read as “1” (bits 4/5: read only).
5	x	
6	PPA	SLx 25C010... (without Page Protection Mode™): No special function, always read as “1” (bit 6: read only).  SLx 25C010.../P (with Page Protection Mode™, refer to <b>chapter 7</b> ): “0” indicates a write or erase operation of the PPM-Bits is finished successfully. “1” indicates a write or erase operation of the PPM-Bits failed or is still in process. <i>Note: After power-up PPA is read as “1” (bit 6: read only).</i>
7	x	This bit is not used and always read as “1” (bit 7: read only).

*Note: Bit 0-7 are read as “1” during an internal programming cycle.*

#### 4.1 Write Enable and Disable Instructions for Status Register and Memory

**Table 4**  
**Write Enable and Disable Instructions**

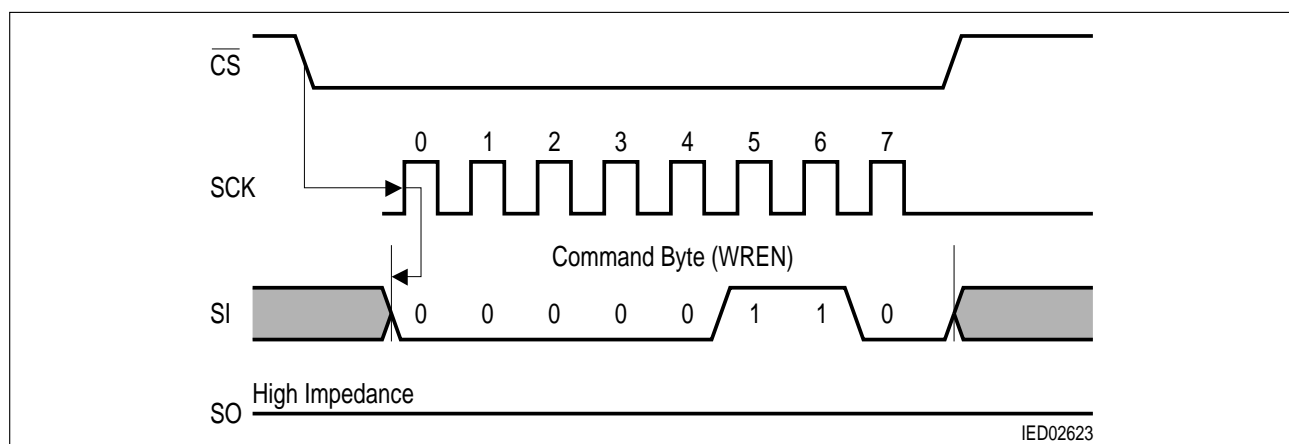
Command Byte	Definition								Function
	b7	b6	b5	b4	b3	b2	b1	b0	
WREN	0	0	0	0	0	1	1	0	Set the write enable latch (enable write operations).
WRDI	0	0	0	0	0	1	0	0	Reset the write enable latch (disable write operations).

##### Write Enable (WREN)

The device will power up in the write disable state when  $V_{CC}$  is applied. All programming commands for the status register and for the memory must therefore be preceded by the write enable command byte WREN. This command sets the WEL bit to “1”.

After the  $\overline{CS}$  line is pulled low to select the device, the command byte WREN is transmitted via the SI line. After the transmission of the command byte, the  $\overline{CS}$  pin has to be driven high.

*Note: After a programming command to the status register or to the memory, the device is automatically returned to the write disable state ( $WEL = “0”$ ).*

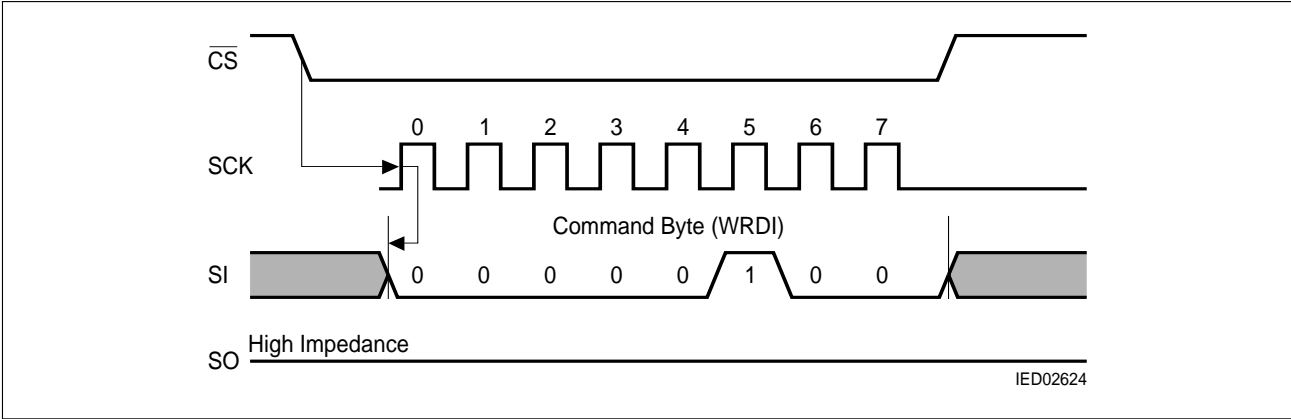


**Figure 4**  
**Write Enable (WREN) Sequence**

##### Write Disable (WRDI)

To protect the device against inadvertent writes, the command byte WRDI sets the WEL bit to “0” and therefore all programming modes are disabled.

After the  $\overline{\text{CS}}$  line is pulled low to select the device, the command byte WRDI is transmitted via the SI line. After the transmission of the command byte the  $\overline{\text{CS}}$  pin has to be driven high.



**Figure 5**  
**Write Disable (WRDI) Sequence**

**4.2 Write Operation to the Status Register**

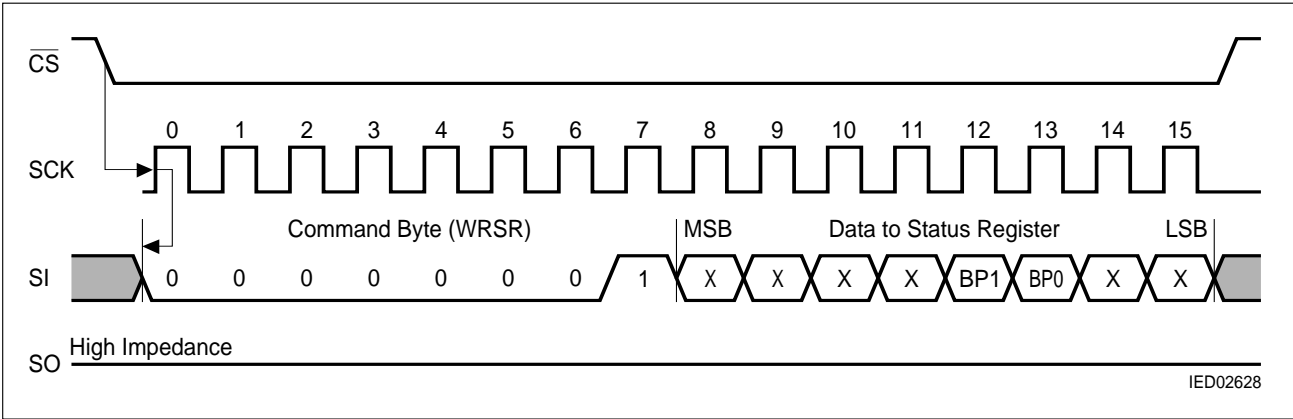
**Table 5**  
**Write Instructions for the Status Register**

Command Byte	Definition								Function
	b7	b6	b5	b4	b3	b2	b1	b0	
WRSR	0	0	0	0	0	0	0	1	Write status register

**Write Status Register (WRSR)**

The command byte WRSR allows the user to change the status of the BP0 and BP1 bits in the status register. All other bits in the status register are for read only. In order to start a write operation to the status register, two separate command bytes must be executed. First, the device must be write enabled via the write enable command byte WREN. Then the write status register command byte WRSR can be executed.

Writing to the status register via the SI input requires the following sequence. After the  $\overline{\text{CS}}$  line is pulled low to select the device, the command byte WRSR is transmitted via the SI line followed by the status register byte to be programmed (bit 7-4 and 1-0 are don't care bits). Programming will start after the  $\overline{\text{CS}}$  pin is brought high.



**Figure 6**  
**Write to Status Register (WRSR) Sequence**

Memory blocks can be protected using BP0 and BP1 according to **table 6**. Data protected in this manner can be read only.

**Table 6**  
**Block Write Protection Bits**

BP1	BP0	Array Address Protected	Protected Block
0	0	-	0
0	1	-	0
1	0	-	0
1	1	\$00-\$7F	all

**4.3 Read Operation to the Status Register**

**Table 7**  
**Read Instruction for the Status Register**

Command Byte	Definition								Function
	b7	b6	b5	b4	b3	b2	b1	b0	
RDSR	0	0	0	0	0	1	0	1	Read status register

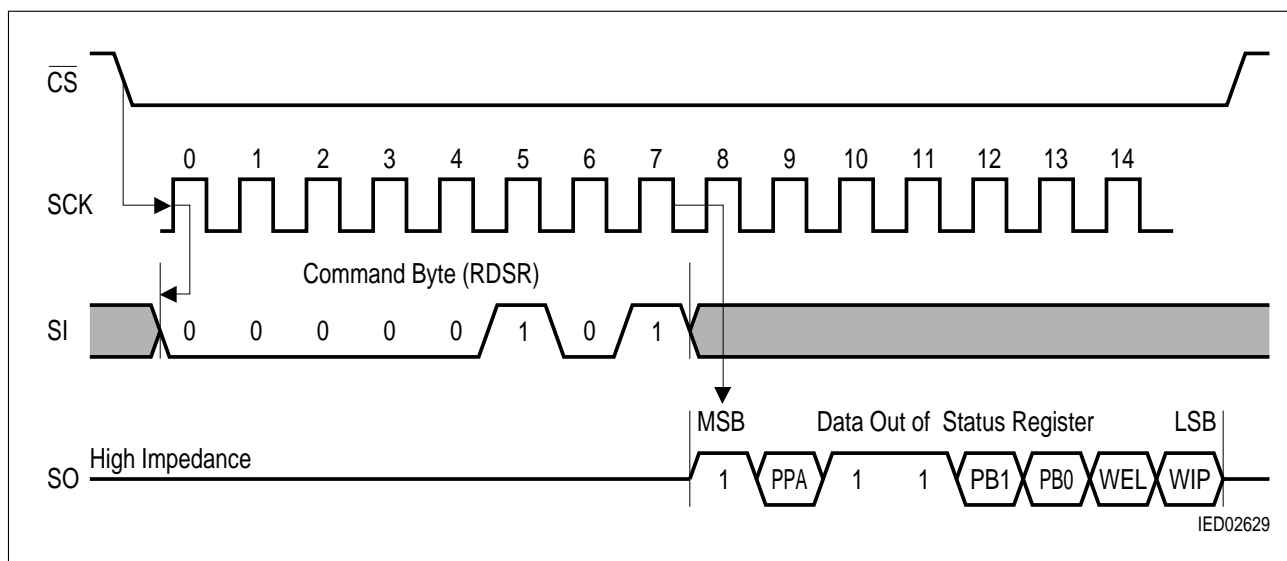
**Read Status Register (RDSR)**

The command byte RDSR provides read access to the status register. The status register can be read at any time, even during an internal programming cycle.

Reading the status register via the SO output requires the following sequence. After the  $\overline{CS}$  line is pulled low to select a device, the RDSR command byte is transmitted via the

SI line. The content of the status register is then shifted out onto the SO line. The  $\overline{CS}$  line should be driven high after data come out.

*Note: During an internal programming cycle bit 0-7 of the status register are read as "1".*



**Figure 7**  
**Read from Status Register (RDSR) Sequence**

5 Write Operations

In order to start a write operation, two separate operations must be executed. First, the device must be write enabled via the write enable command byte WREN. Then the write operation can be executed. Either one byte (Byte Write) or up to 8 byte (Page Write) can be modified in one programming procedure. During an internal programming cycle, all commands will be ignored except the command byte RDSR (read status register).

*Note: Write operations to the memory can only be executed to blocks that are not write protected by the status register bits BP0 and PB1 and to pages that are not write protected by a Page Protection bit (SLx 25C010.../P only, refer to **chapter 7**) .*

Table 8  
Write Instruction

Command Byte	Definition								Function
	b7	b6	b5	b4	b3	b2	b1	b0	
WRITE	0	0	0	0	0	0	1	0	Write data to memory array beginning at selected address

5.1 Byte Write

A write operation requires the following sequence. After the  $\overline{CS}$  line is pulled low to select the device, the command byte WRITE is transmitted via the SI line followed by the byte address (A7 is a don't care bit, A6-A0) and the data (D7-D0) to be programmed. Programming will start after the  $\overline{CS}$  pin is brought high.

The ready/busy status of the device can be determined by initiating a read to the status register with RDSR. If WIP= "0" the programming cycle is finished. After execution of the command byte WRITE the EEPROM is automatically returned to the write disable state.

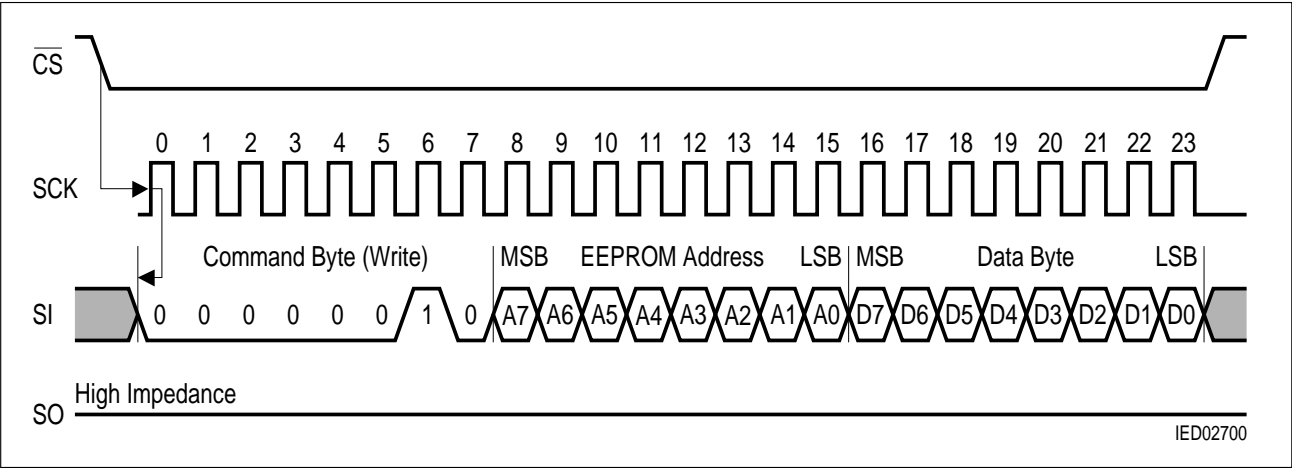


Figure 8  
Byte Write Sequence

5.2 Page Write

The page write procedure is the same as the byte write procedure up to the first data byte. In a page write procedure however, the EEPROM address byte is followed by a sequence of one to a maximum of 8 data bytes with new data to be programmed. If more than 8 bytes of data are transmitted, the address counter will roll over and the previously transmitted data will be overwritten, i.e. only the last 8 transmitted bytes will be programmed. Programming will start after the  $\overline{CS}$  pin is brought high.

The ready/busy status of the device can be determined by initiating a read to the status register with RDSR. If WIP= "0" the programming cycle is finished. After execution of the command byte WRITE the EEPROM is automatically returned to the write disable state.

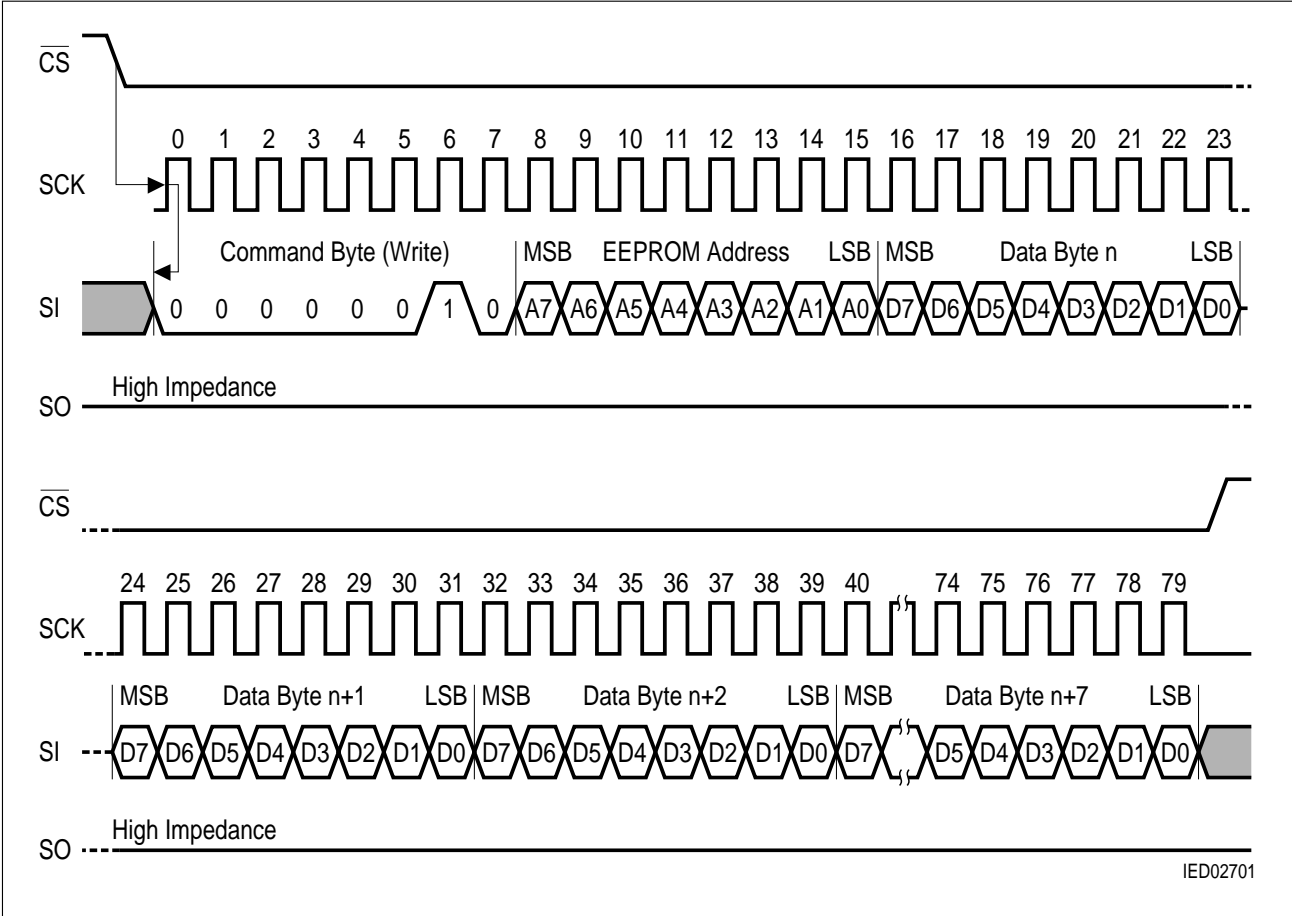


Figure 9  
Page Write Sequence



6 Read Operations

Either one byte (Byte Read) or any number of bytes up to the whole memory (Sequential Read) can be read in one sequence.

Table 9  
Read Instruction

Command Byte	Definition								Function
	b7	b6	b5	b4	b3	b2	b1	b0	
READ	0	0	0	0	0	0	1	1	Read data from memory array beginning at the selected address

6.1 Byte Read

Reading the EEPROM via the SO output requires the following sequence. After the  $\overline{CS}$  line is pulled low to select the device, the READ command byte is transmitted via the SI line followed by the address to be read (A7 is don't care, A6-A0). The data (D7-D0) at the specified address are then shifted out onto the SO line. During this time, any data on the SI line will be ignored. If only one byte is to be read, the  $\overline{CS}$  line should be driven high after data come out.

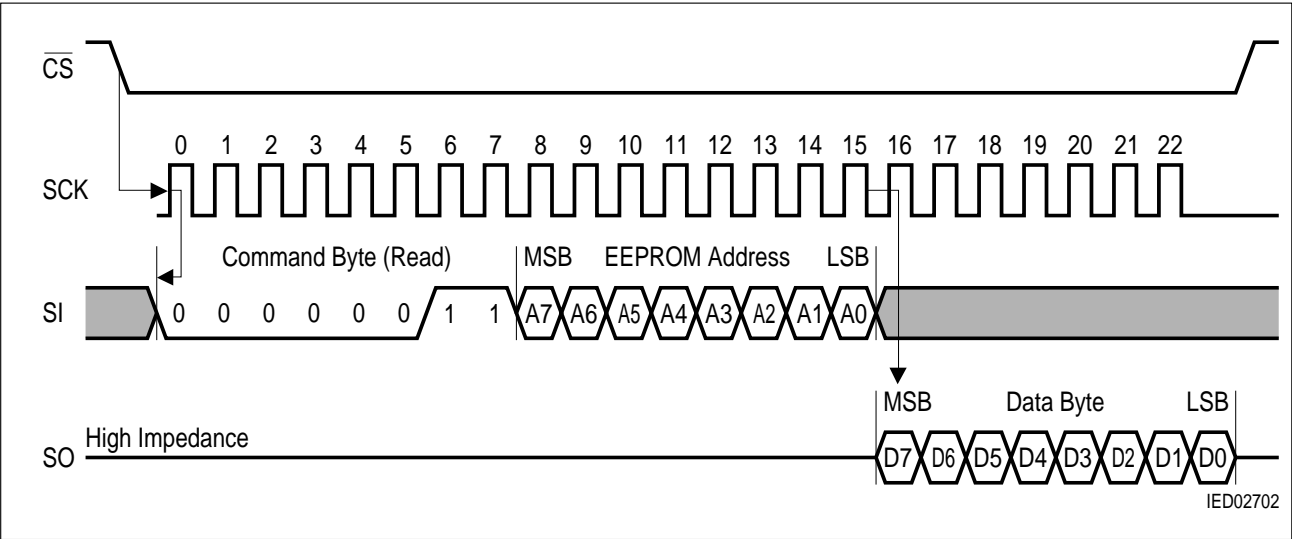


Figure 10  
Read Byte Sequence

6.2 Sequential Read

The sequential read procedure is the same as the byte read procedure up to the first data byte is shifted out on the SO line. The read can be continued since the byte address is automatically incremented and data will continue to be shifted out. The read sequence is terminated by pulling up the  $\overline{CS}$  line.

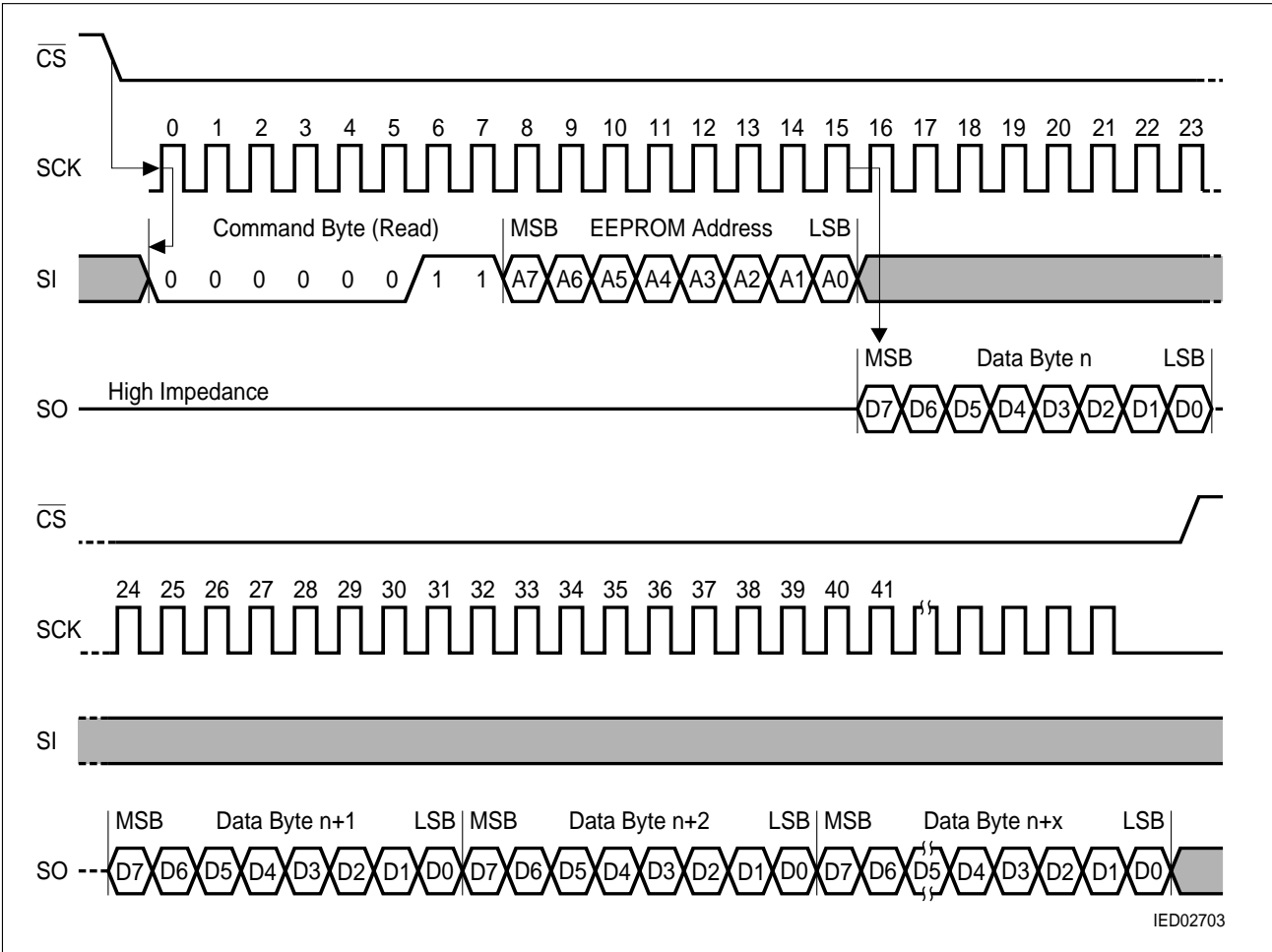


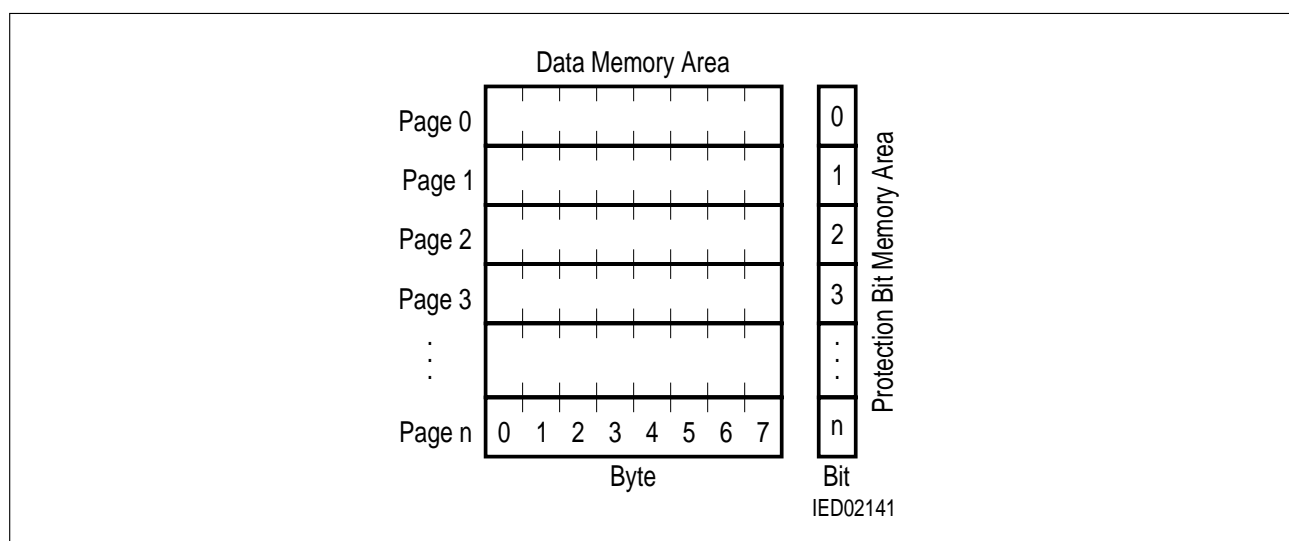
Figure 11  
Sequential Read Sequence

## 7 Page Protection Mode™

The page protection mode is supported by the SLx 25C010 .../P types only. For example SLA 25C010-D/P has the same functionality as SLA 25C010-D enhanced by page protection mode.

Each page (8 bytes) in the data memory can be protected against unintended data changes by an associated protection bit. The protection bit memory consists of an additional EEPROM of 16 bit (**figure 12**).

Data in the data memory can be modified only if the assigned protection bit is erased (logical state "1"). After writing the data bytes to a page, the protection is achieved by writing the associated protection bit (logical state "0"). Further changes of data within a protected page is possible only after erasing the protection bit.



**Figure 12**  
**Data Page and Assigned Protection Memory**

A special procedure to write or erase a protection bit guarantees proper activation or deactivation of page protection. For protection bit write or erase, all 8 data bytes of the respective page have to be entered for verification. The data then are compared internally with the data to be protected. In case of identity the protection bit is written or erased correspondingly.

## 7.1 Protection Bit Handling

The bits of the protection memory can be addressed directly for reading or programming. A protection bit address corresponds to the lowest address within the respective page (A7 is don't care, A6-A3, A2 to A0 = "0"). The status of each protection bit is sensed internally. A written state ("0") prevents programming in the associated page. If an already protected memory page is accidentally addressed for programming, the programming procedure is suppressed.

For devices with page protection mode, an additional instruction set for addressing and manipulation of protection bits is implemented. For protection bit handling there are three additional command bytes for write, erase and read of a protection bit. These three command bytes are listed below (**table 10**).

**Table 10**  
**Instructions for Protection Bit Manipulation**

Command Byte	Definition								Function
	b7	b6	b5	b4	b3	b2	b1	b0	
WRPB	0	0	1	0	0	0	1	0	Write page protection bit of selected page
ERPb	0	0	1	1	0	0	1	0	Erase page protection bit of selected page
RDPB	0	0	0	1	0	0	1	1	Read page protection bit of selected page

7.2 Protection Bit Write and Erase

For writing or erasing a protection bit, the data of the respective page have to be known by the master. The master has to present the page data as a reference for comparison by the EEPROM. A successful comparison is necessary in order to change the status of the protection bit.

The data of the page are not effected by the write or erase procedure of the protection bit. The SPI bus protocol is shown in **figure 13** for protection bit write and in **figure 14** for protection bit erase.

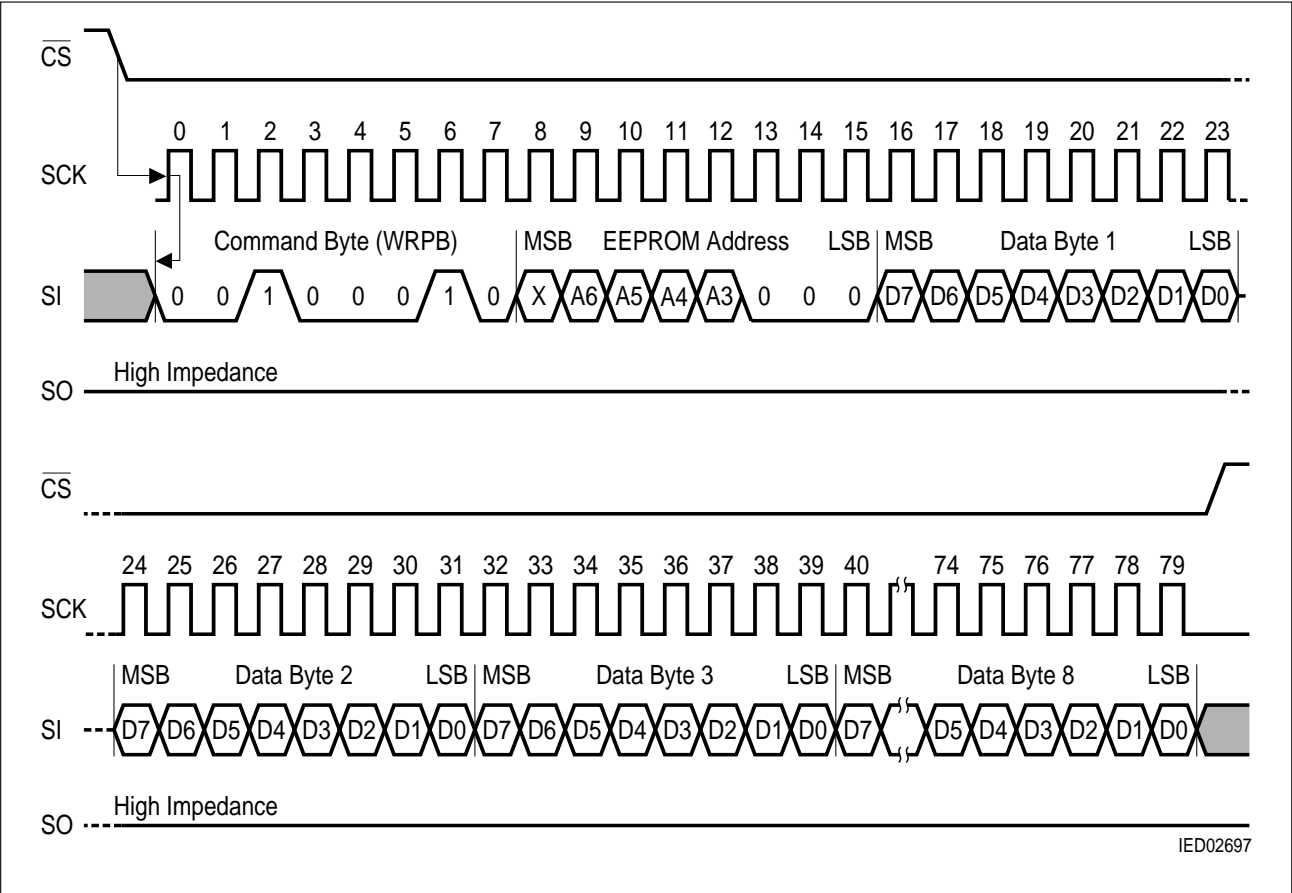
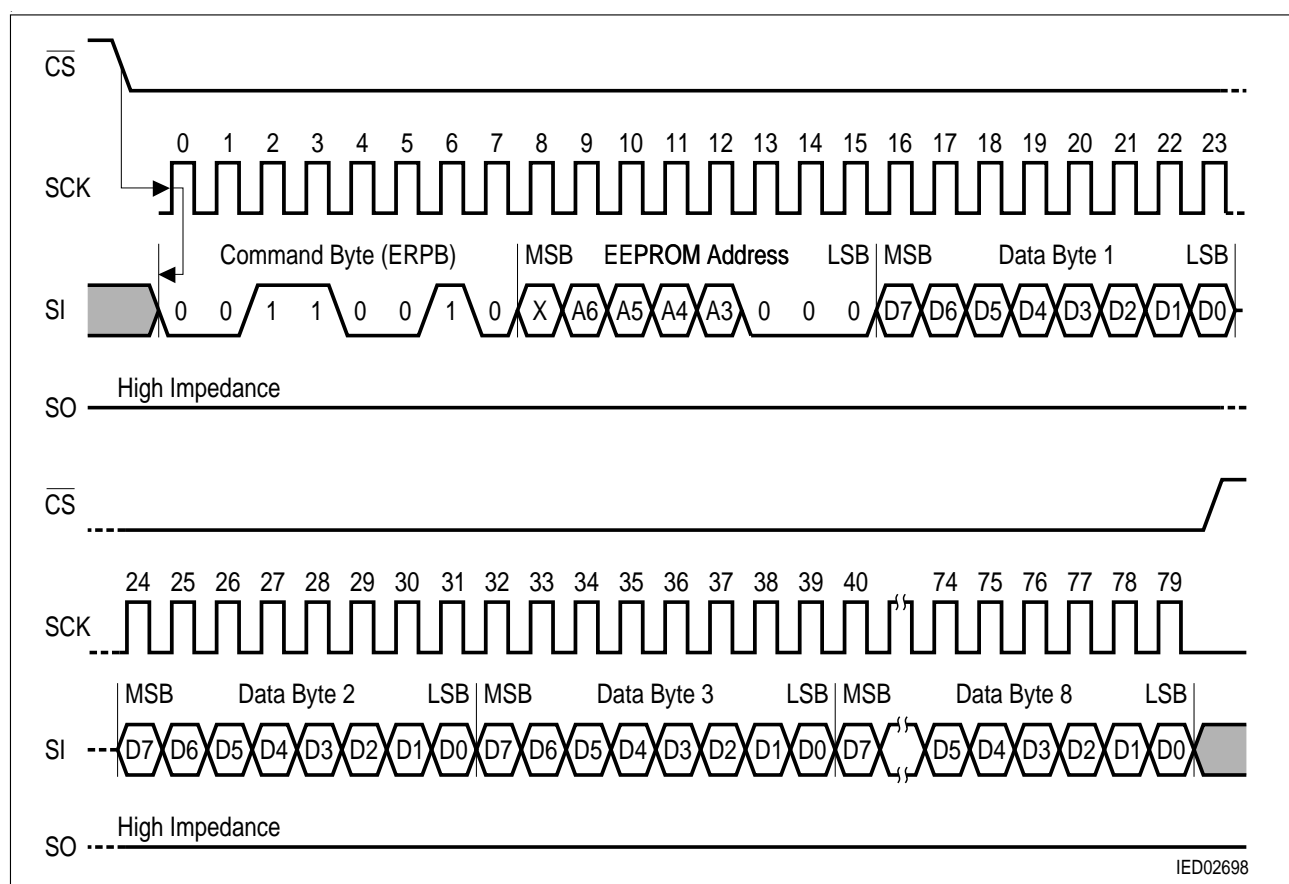


Figure 13  
Sequence for Protection Bit Write

A write or erase operation to a page protection bit requires the following sequence. After the  $\overline{CS}$  line is pulled low to select the device, the command byte WRPB for protection bit write (or ERPB for protection bit erase) is transmitted via the SI line followed by the remaining address bits (A7 is don't care, A6-A3, A2 to A0 = "0"). The address of the protection bit corresponds to the address of the first byte of the page to protect (or unprotect).

The address bits are followed by 8 parameter bytes identical to the 8 data bytes of the page to be protected or unprotected. The data of the first entered byte must be identical to the data byte stored at the lowest address of the current page.

The other 7 bytes have to be identical to the bytes stored in ascending address order within the same page. Programming will start after the  $\overline{CS}$  pin is brought high.



**Figure 14**  
**Sequence for Protection Bit Erase**

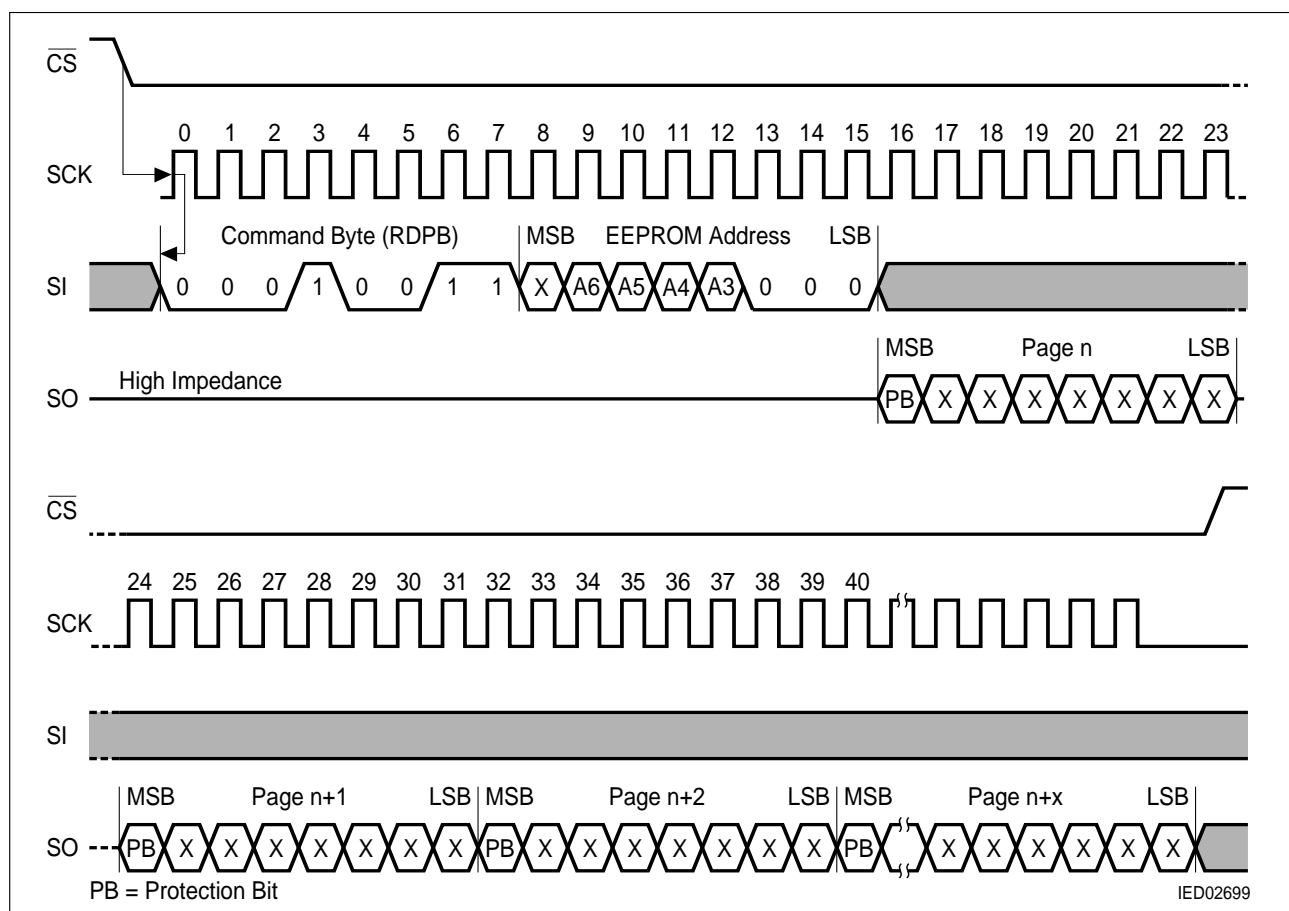
For a successful programming of a protection bit, four conditions have to be fulfilled.

1. The page must be located within a block which is *not* protected by the status register bits PB0 and PB1.
2. The device must be write enabled via the write enable instruction (WREN), before the write (WRPB) or erase (ERPB) instruction can be executed.
3. The  $\overline{WP}$  pin is high.
4. All 64 bits of a page have to be verified successfully.

A successful programming is indicated by the EEPROM by setting the PPA-bit to "0" in the status register. The write or erase cycle is finished after 2.5 ms (typical).

### 7.3 Protection Bit Read

The status of the protection bit can be requested by the master. The byte sequence for protection bit read is shown in **figure 15**.



**Figure 15**  
**Byte Sequence for Protection Bit Read**

To read the status of a protection bit the device must be selected with a high to low transition of the  $\overline{CS}$  pin, then the RDPB command has to be send followed by the remaining bits for the basis address of the respective page (A7 is don't care, A6-A2 to A0 = "0"). The first bit (MSB) of the transferred byte indicates the status of the protection bit of the addressed page. The other 7 bits are not valid. The page protection status is indicated as follows:

Protection Bit=1 : The Page Protection Mode™ is deactivated.

Protection Bit=0 : The Page Protection Mode™ is activated and data in the associated page are protected against changes.

To stop the transmission the device has to be deselected with a low to high transition of the  $\overline{CS}$  pin. If not, the address counter is incremented automatically and the device will send the protection bit status of the next page.

## 8 Electrical Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at  $T_A = 25^\circ\text{C}$  and the given supply voltage.

### 8.1 Absolute Maximum Ratings

Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this data sheet is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

**Table 11**

Parameter	Limit Values	Units
Operating temperature	range 1 (industrial)	– 40 to + 85
	range 2 (automotive)	– 40 to + 125
		(– 40 to + 150 on request)
Storage temperature	– 65 to + 150	°C
Supply voltage	– 0.3 to + 7.0	V
All inputs and outputs with respect to ground	– 0.3 to $V_{cc} + 0.5$	V
ESD protection (human body model)	> 4000	V

### 8.2 DC Characteristics

**Table 12**

Parameter	Symbol	Limit Values			Units	Test Condition
		min.	typ.	max.		
Supply voltage	$V_{CC}$	2.7		5.5	V	
Supply current <sup>1)</sup> (read)	$I_{CC}$		0.5		mA	$V_{CC} = 5\text{ V}; f_c = 2.1\text{ MHz}$
Supply current <sup>1)</sup> (write)	$I_{CC}$		1		mA	$V_{CC} = 5\text{ V}; f_c = 2.1\text{ MHz}$
Standby current <sup>2)</sup>	$I_{SB}$			3	$\mu\text{A}$	$V_{CC} = 5\text{ V}$



Table 12 (cont'd)

Parameter	Symbol	Limit Values			Units	Test Condition
		min.	typ.	max.		
Input leakage current	$I_{LI}$		0.1	3	$\mu A$	$V_{IN} = V_{CC} \text{ or } V_{SS}$
Output leakage current	$I_{LO}$		0.1	3	$\mu A$	$V_{OUT} = V_{CC} \text{ or } V_{SS}$
Input low voltage	$V_{IL}$	$-0.3$		$0.3 \times V_{CC}$	V	
Input high voltage	$V_{IH}$	$0.7 \times V_{CC}$		$V_{CC} + 0.5$	V	
Output low voltage	$V_{OL}$			0.4	V	$I_{OL} = 3 \text{ mA}; V_{CC} = 5 \text{ V}$ $I_{OL} = 2.1 \text{ mA}; V_{CC} = 3 \text{ V}$
Input/output capacitance (SI/SO)	$C_{IO}$			8 <sup>3)</sup>	pF	$V_{IN} = 0 \text{ V}; V_{CC} = 2.7 \text{ V}$
Input capacitance (other pins)	$C_{IN}$			6 <sup>3)</sup>	pF	$V_{IN} = 0 \text{ V}; V_{CC} = 2.7 \text{ V}$

<sup>1)</sup> The values for  $I_{CC}$  are maximum peak value

<sup>2)</sup> Valid over the whole temperature range

<sup>3)</sup> This parameter is characterized only

### 8.3 AC Characteristics

Table 13

Parameter	Symbol	Limit Values $V_{CC} = 2.7 - 5.5 \text{ V}$			Units
		min.	typ.	max.	
SCK clock frequency	$f_{SCK}$	0		2.1	MHz
Cycle time	$t_{CYC}$	475			ns
$\overline{CS}$ lead time	$t_{LEAD}$	250			ns
$\overline{CS}$ lag time	$t_{LAG}$	250			ns
Clock HIGH time	$t_{WH}$	200			ns
Clock LOW time	$t_{WL}$	200			ns
Data setup time	$t_{SU}$	100			ns

Table 13 (cont'd)

Parameter	Symbol	Limit Values $V_{CC} = 2.7 - 5.5 V$			Units
		min.	typ.	max.	
Data hold time	$t_H$	100			ns
Clock rise time	$t_{RI}$			2	$\mu s$
Clock fall time	$t_{FI}$			2	$\mu s$
$\overline{Hold}$ setup time	$t_{HD}$	100			ns
$\overline{Hold}$ hold time	$t_{CD}$	100			ns
$\overline{CS}$ deselect time	$t_{CS}$	500			ns
Output disable time	$t_{DIS}$			250	ns
Output valid from Clock LOW	$t_V$			200	ns
Output hold time	$t_{HO}$	0			ns
Output rise time	$t_{RO}^{(1)}$			200	ns
Output fall time	$t_{FO}^{(1)}$			200	ns
Rising edge of $\overline{Hold}$ to output out of Z	$t_{LZ}$			100	ns
Falling edge of $\overline{Hold}$ to output on Z	$t_{HZ}$			100	ns
SI/SO and SCK spike suppression time at constant inputs	$t_I$		50		ns

<sup>1)</sup> This parameter is characterized only

## 8.4 Erase and Write Characteristics

Table 14

Parameter	Symbol	Limit Values $V_{CC} = 2.7 - 5.5 V$		Units
		typ.	max.	
Erase + write cycle (per page)	$t_{WC}$	5	8	ms
Erase page protection bit		2.5	4	ms
Write page protection bit		2.5	4	ms

8.5 Timing Diagrams

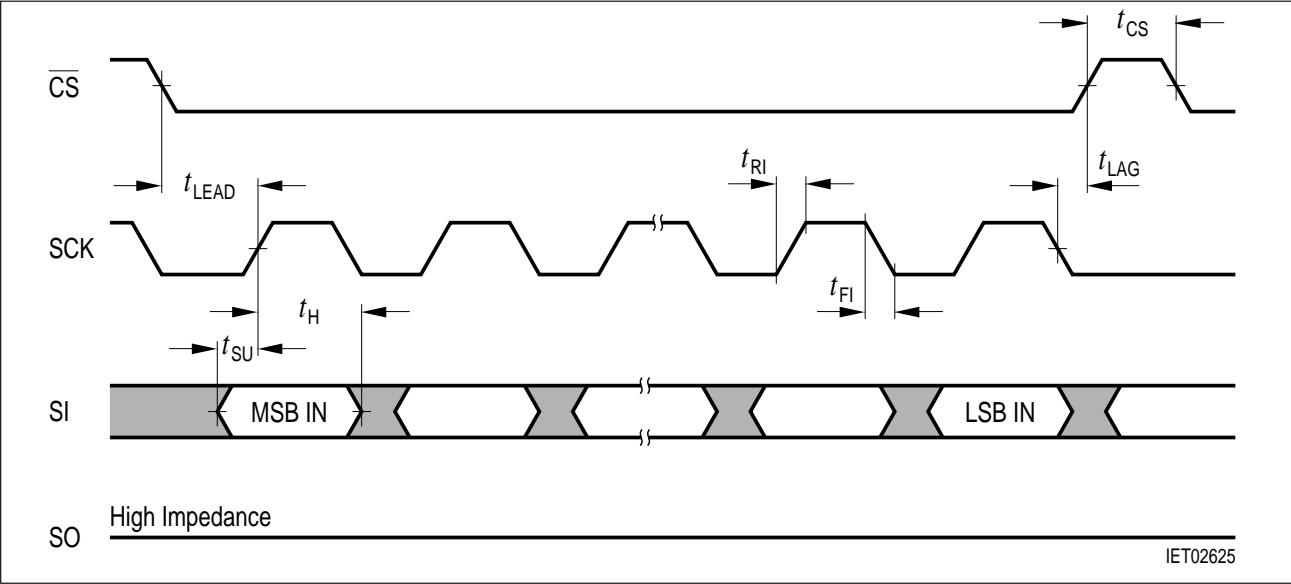


Figure 16  
Bus Timing for Serial Input

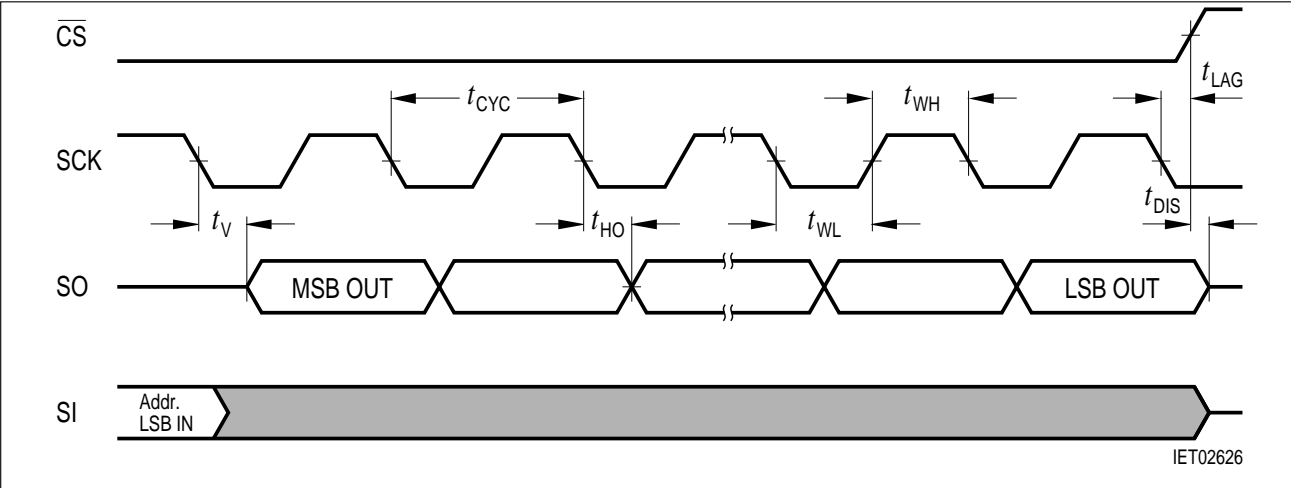
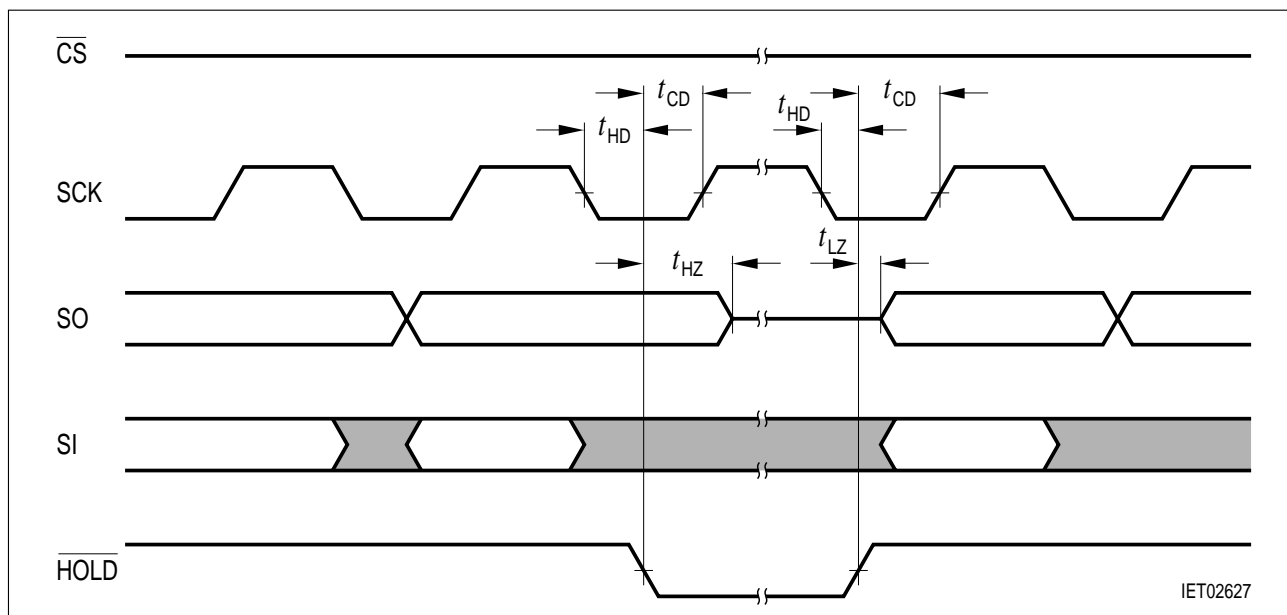


Figure 17  
Bus Timing for Serial Output

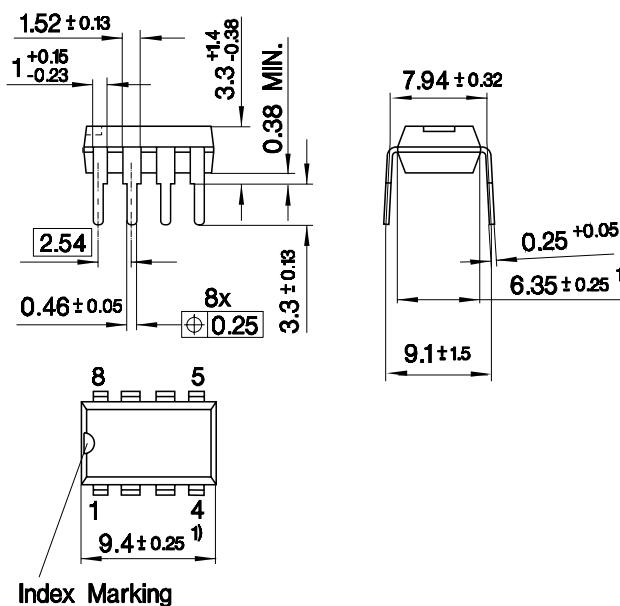


**Figure 18**  
**Hold Timing**

## 9 Package Outlines

### P-DIP-8-3

(Plastic Dual In-line Package)

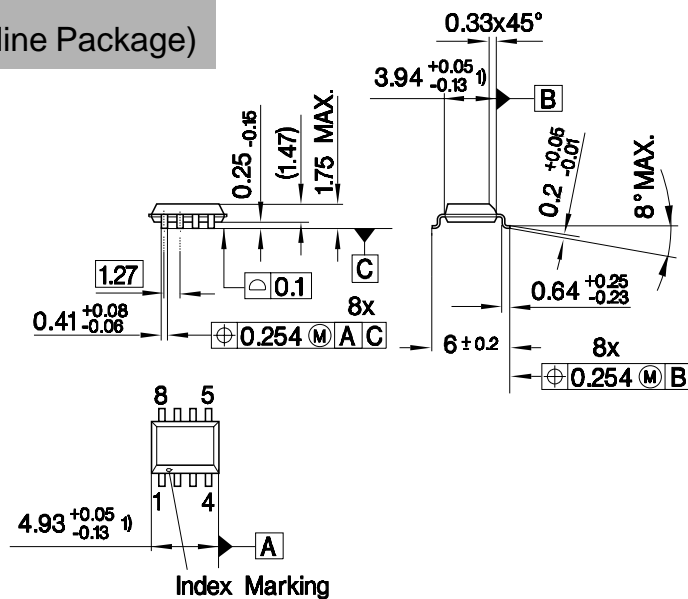


1) Does not include plastic or metal protrusion of 0.25 max. per

GPD05696

### P-DSO-8-2

(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side

GPS05473

### Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm