IS24C64

65,552-BIT SERIAL ELECTRICALLY ERASABLE PROM

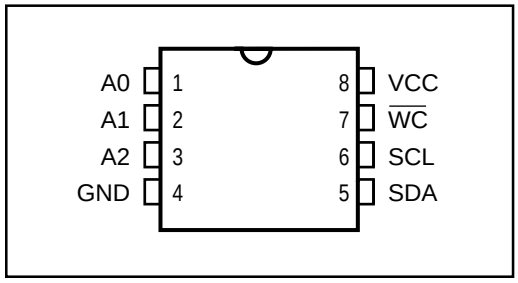
ADVANCE INFORMATION
OCTOBER 1997

FEATURES

- 400 KHz (5V) Compatibility
- Low power CMOS
  – Active current less than 3.0 mA
  – Standby current less than 35 µA
- Operating voltage: 4.5V to 5.5V
- Hardware write protection
  – Write control pin
- Internally organized: 8192 x 8
- 32 byte page write mode (partial page writes allowed)
- Two-wire serial interface
- Bidirectional data transfer protocol
- Self timed write cycles (10 ms max)
- High-reliability
  – Endurance: 1 million cycles per byte
  – Data retention: 100 years
- Industrial temperature available
- 8-pin PDIP or SOIC packages

PIN CONFIGURATION

8-Pin DIP and SOIC



PIN DESCRIPTIONS

A0-A2	Address Inputs (No connection)
SDA	Serial Data I/O
SCL	Serial Clock Input
$\overline{WC}$	Write Control Input
Vcc	Power
GND	Ground

OVERVIEW

The IS24C64 provides 65,536 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 8197 words of 8 bits each. It is fabricated using *ISSI*'s advanced CMOS EEPROM technology and operates from a single supply.

The IS24C64 is internally organized as 256 pages of 32 bytes each. Random word addressing requires 12/13 bit data word address bank. The IS24C64 cascadable feature allows up to 8 devices to share a common 2-wire bus. Included is a bidirectional serial data bus synchronized by a clock offering flexible byte write and a faster 32-byte page write. A write protect pin can protect data in the upper quadrant of memory.

PIN DESCRIPTIONS

Serial Clock (SCL) - The SCL input is used to positive edge clock all data into the device. In the READ mode, data is clocked out on the falling edge of SCL.

Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW. It is an open-drain output, and may be wire-ORed with any number of open-drain or open-collector outputs.

Device/Page Addresses (A0, A1, and A2):

The A2, A1 and A0 pins are device address inputs that are hard wired or left not connected for hardware compatibility with IS24C64. When the pins are hardwired, as many as eight 64K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). When the pins are not hardwired, the default A2, A1 and A0 are zero.

Write Control ($\overline{WC}$) - The Write Control input is used to disable any attempt to write to the memory. When HIGH, the upper quadrant (16K bits)of array is protected against write operations; when LOW, the write function is normal. The part can be read independent of the state of $\overline{WC}$ pin. When not connected this pin will be pulled LOW.

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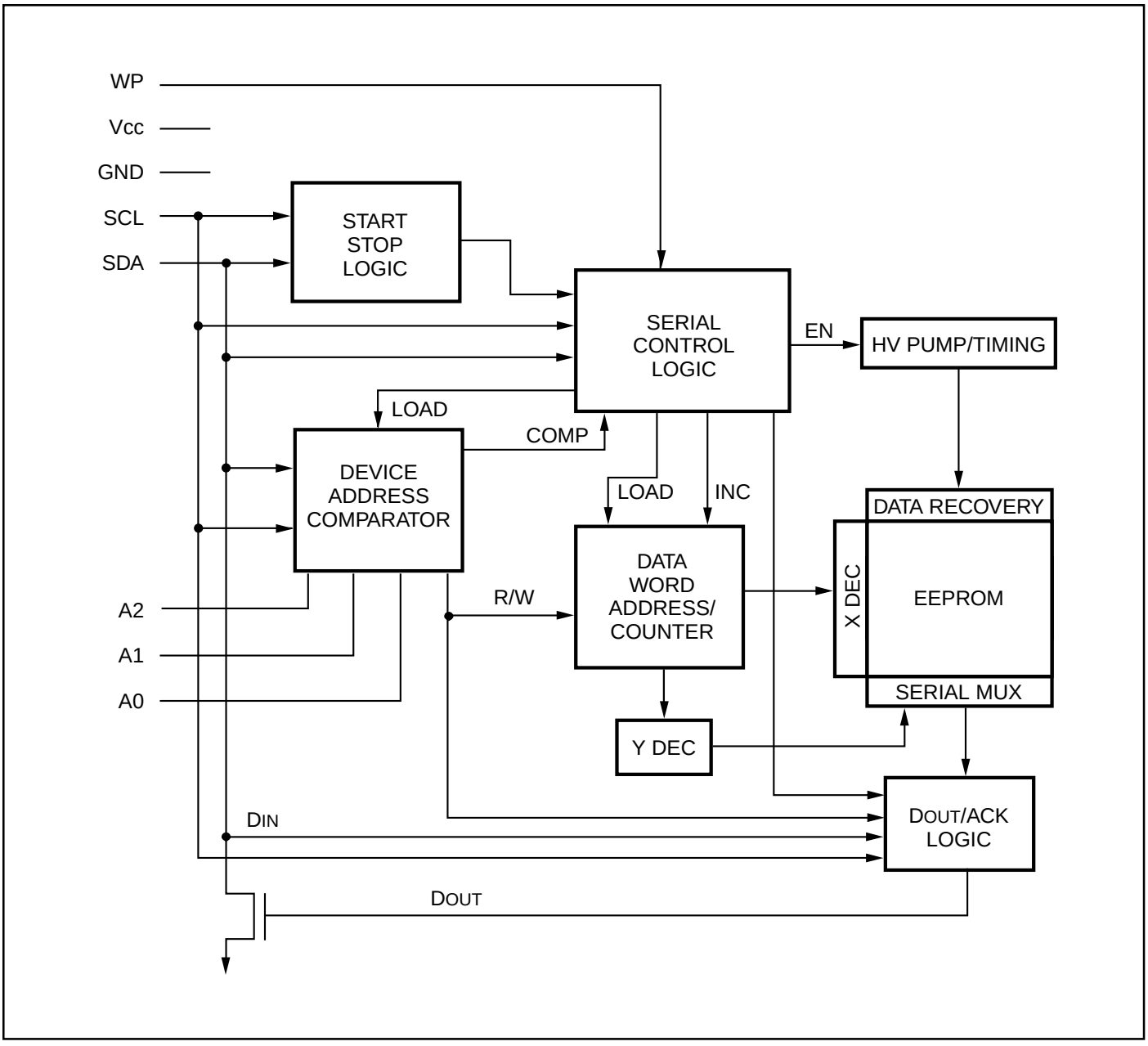
BLOCK DIAGRAM



GENERAL DESCRIPTION

Device Addressing

The IS24C64 requires an 8 bit device address word following a start condition to enable the chip for a read or write operation (See Figure 4). The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all 2-wire EEPROM devices.

The IS24C64 uses the three device address bits A2, A1, A0 to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins. The A2, A1, and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the rea/write operation select bit. A read operation is initiated if this bit is HIGH and a write operation is initiated if this bit is LOW.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the device will return to standby state.

Noise Protection

Special internal circuitry placed on the SDA and SCL pins prevent small noise spikes from activating the device. A low-V_{CC} detector resets the device to prevent data corruption in a noisy environment.

Data Security

The IS24C64 has a hardware data protection scheme that allows the user to write protect the upper quadrant (16K bits) of memory when the WP pin is at V_{CC}.

DEVICE OPERATION

CLOCK and DATA Transitions

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (See Figure 3). Data changes during SCL high periods will indicate a start or stop condition as defined below.

Start Condition

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (See Figure 2).

Stop Condition

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (See Figure 2).

Acknowledge

All addresses and data words are serially transmitted to and from the EEPROM in 8 bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

Standby Mode

The IS24C64 features a low power standby mode which is enabled:

- upon power-up
- after the receipt of the STOP bit and the completion of any internal operations

WRITE OPERATIONS

Byte Write

A write operation requires two 8 bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8 bit data word. Following receipt of the 8 bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (See Figure 5).

Page Write

The IS24C64 EEPROM is capable of 32-byte page writes.

A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 31 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (See Figure 6).

The data word address lower 5 bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. If more than 32 data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

Acknowledge Polling

Once the internal write cycle has started and the IS24C64 inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the Device Address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has been completed will the IS24C64 respond with a zero allowing the read or write sequence to continue.

READ OPERATION

READ operations are initiated in the same manner as WRITE operations, except that the read/write bit of the device address word is set to “1”. There are three READ operation options: current address read, random address read and sequential read.

Current Address Read

The IS24C64 contains an internal address counter which maintains the address of the last data word accessed, incremented by one. This address stays valid between operations as long as the address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page, to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (See Figure 7).

Random Read

A random READ requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (See Figure 8).

Sequential Read

Sequential Reads can be initiated as either a Current Address Read or Random Address Read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words.

When memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (See Figure 9).

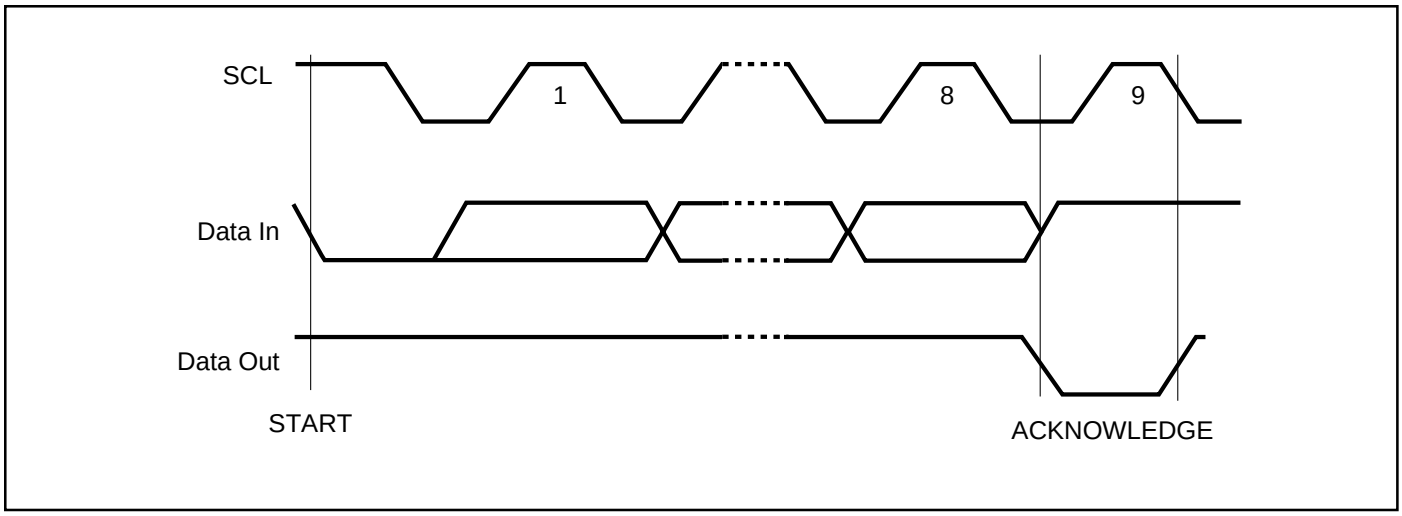


Figure 1. Output Acknowledge

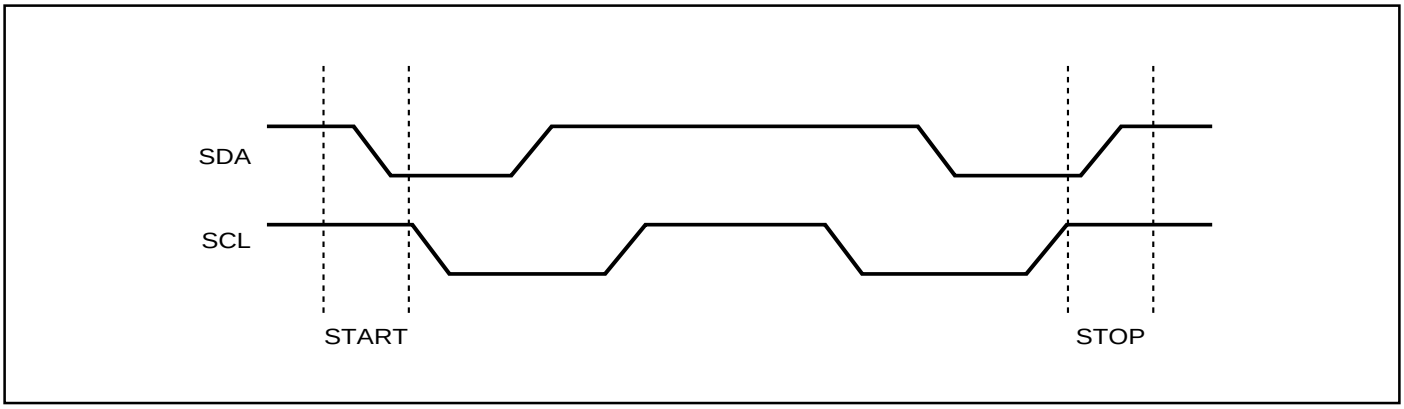


Figure 2. START and STOP Conditions

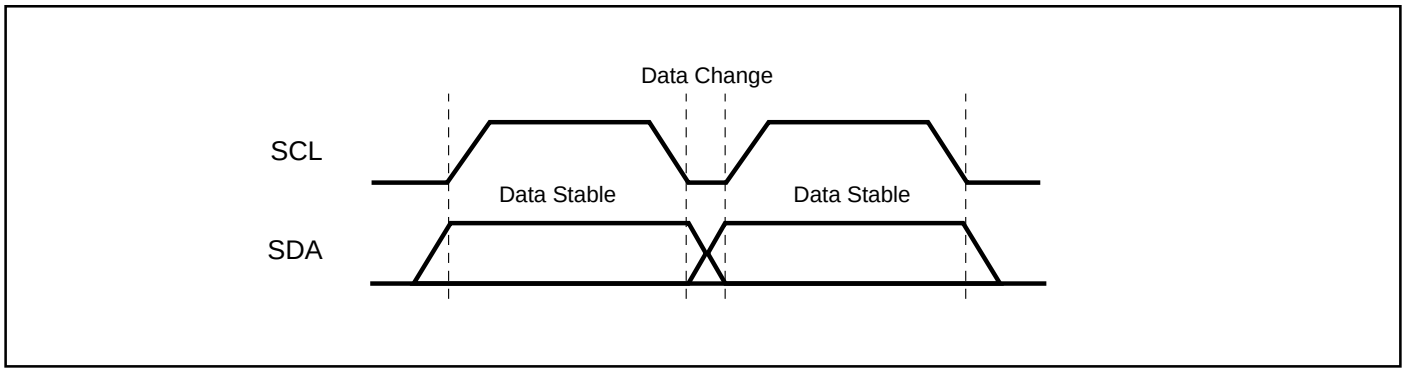


Figure 3. Data Validity Protocol

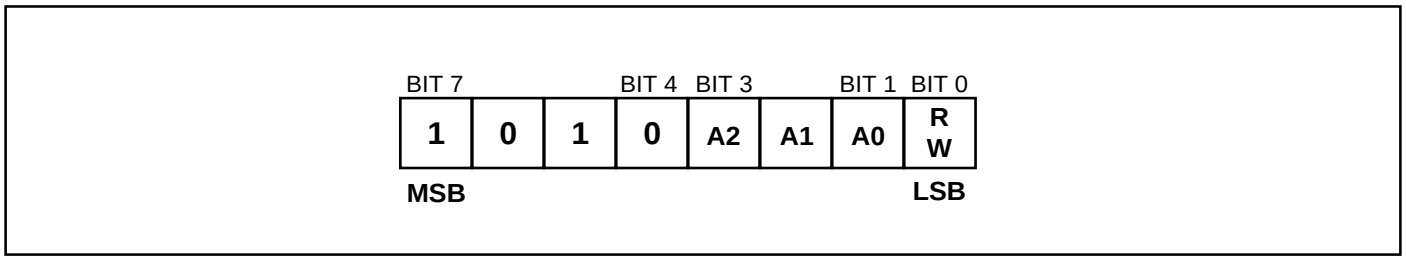


Figure 4. Device Addressing

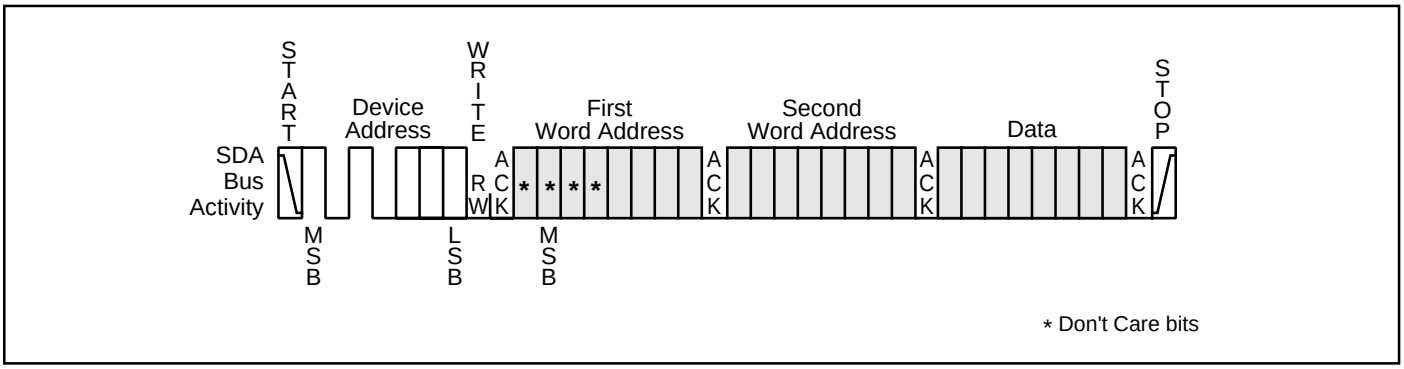


Figure 5. Byte Write

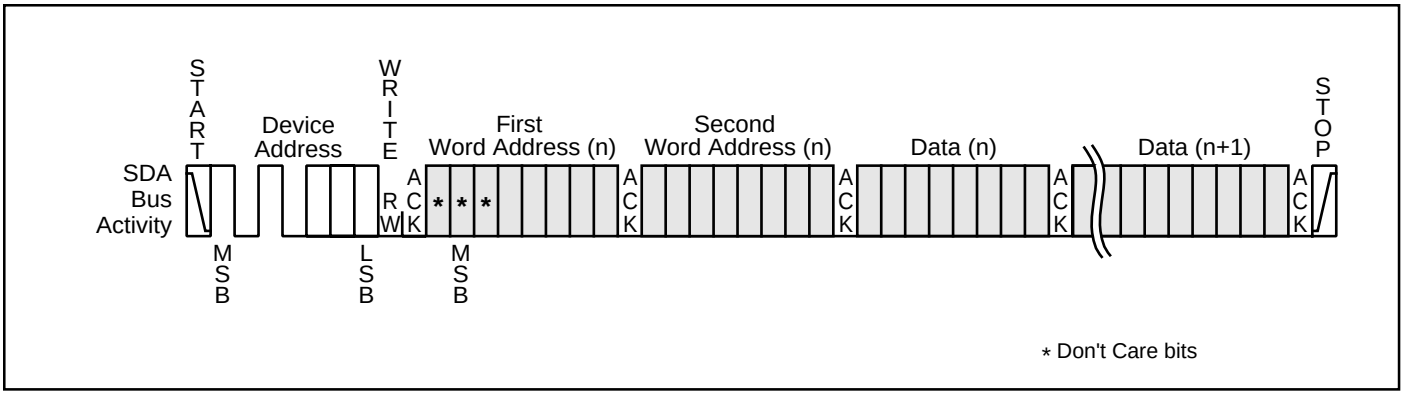


Figure 6. Page Write

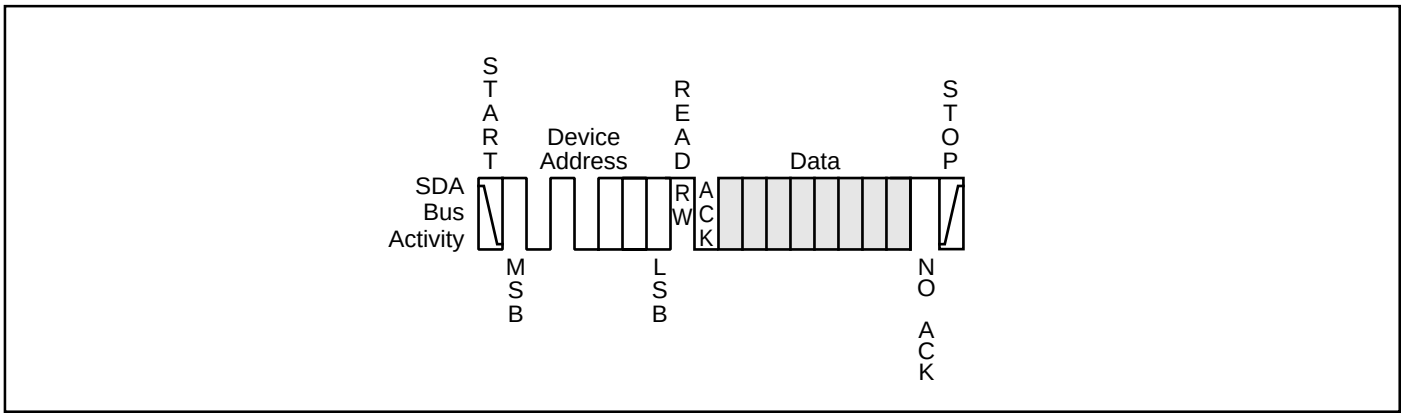


Figure 7. Current Access Read

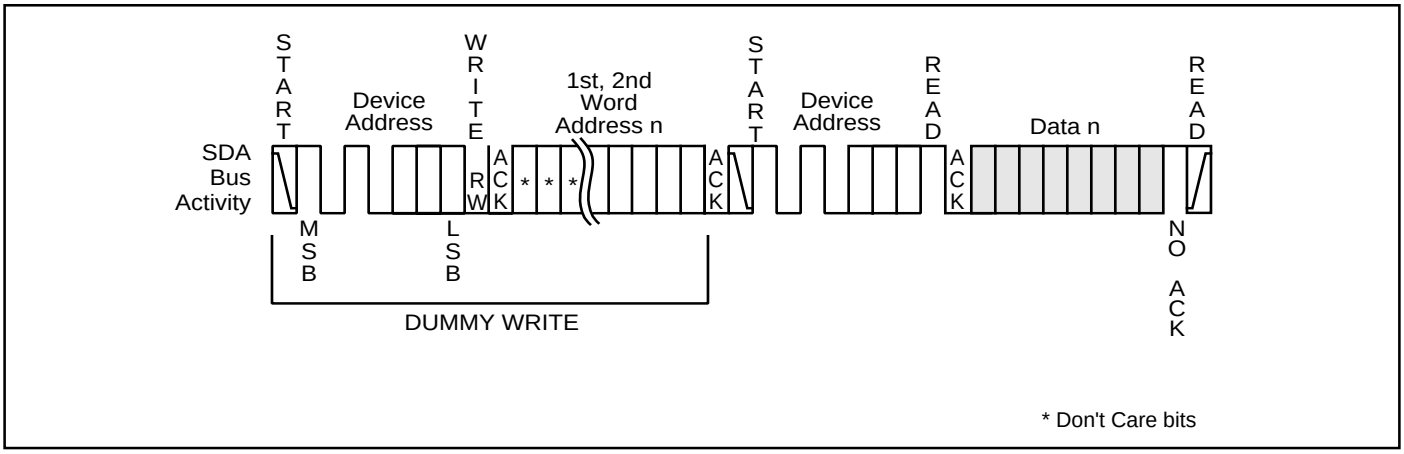


Figure 8. Random Access Read

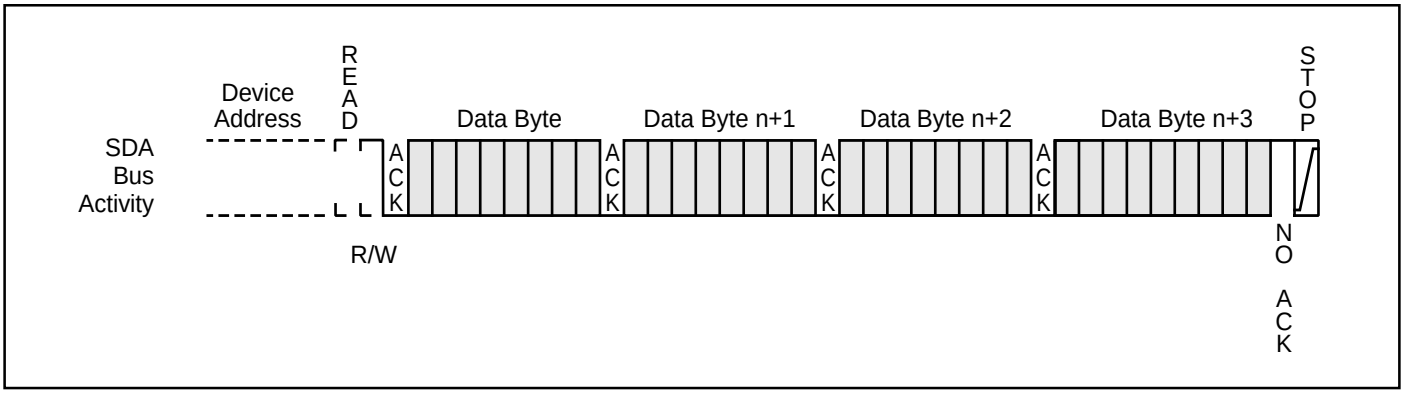


Figure 9. Sequential Read

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	2.7 to +5.5	V
V_P	Voltage on Any Pin	–0.5 to Vcc + 0.5	V
T_{BIAS}	Temperature Under Bias	–40 to +85	°C
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Output Current	5	mA

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

CAPACITANCE(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance (SDA)	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters and not 100% tested.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 5.0V.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for IS24C64 and –40°C to +85°C for IS24C64-I, Vcc = 4.5V to 5.5V. (Unless Otherwise Noted.)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OL1}	Output LOW Voltage	V_{CC} = 2.7V., I_{OL} = 0.15 mA	—	0.25	V
V_{OL2}	Output LOW Voltage	V_{CC} = 3.0V., I_{OL} = 2.1 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		—	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage		–1.0	—	V
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} max.	—	3	µA
I_{LO}	Output Leakage Current		—	3	µA

POWER SUPPLY CHARACTERISTICS

T_A = 0°C to +70°C for IS24C64 and –40°C to +85°C for IS24C64-I, Vcc = 4.5V to 5.5V.

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{CC1}	Vcc Operating Current Vcc = 5.0V	READ at 100 KHz	—	1.0	mA
I_{CC2}	Vcc Operating Current Vcc = 5.0V	WRITE at 100 KHz	—	3.0	mA
I_{SB1}	Standby Current	Vcc = 4.5V, V_{IN} = V_{CC} or GND	—	20	µA
I_{SB2}	Standby Current	Vcc = 5.5V, V_{IN} = V_{CC} or GND	—	35	µA

AC ELECTRICAL CHARACTERISTICS

Applicable Over Recommended Operating Range From: T_A = –40°C to +85°C, Vcc = 5.0 ± 10%, CL = ITTL Gate and 100pF (Unless Otherwise Noted)

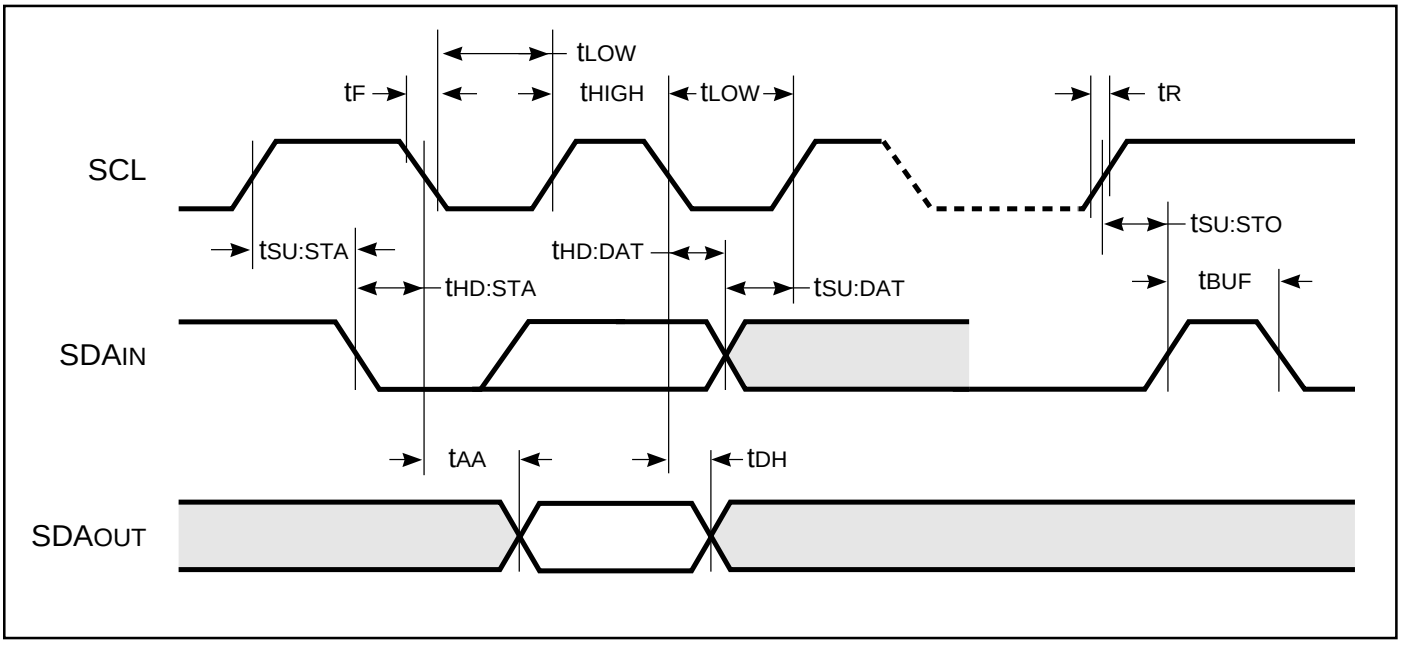
Symbol	Parameter	Test Conditions	5.5V Min.	5.5V Max.	Unit
f_{SCL}	SCL Clock Frequency		0	400	KHz
t_I	Noise Suppression Time(1)		—	50	ns
t_{LOW}	Clock LOW Period		1.2	—	µs
t_{HIGH}	Clock HIGH Period		0.6	—	µs
t_{BUF}	Bus Free Time Before New Transmission(1)		1.2	—	µs
$t_{SU:STA}$	Start Condition Setup Time		0.6	—	µs
$t_{SU:STO}$	Stop Condition Setup Time		0.6	—	µs
$t_{HD:STA}$	Start Condition Hold Time		0.6	—	µs
$t_{HD:STO}$	Stop Condition Hold Time		0.6	—	µs
$t_{SU:DAT}$	Data In Setup Time		100	—	ns
$t_{HD:DAT}$	Data In Hold Time		0	—	µs
t_{DH}	Data Out Hold Time	SCL LOW to SDA Data Out Change	50	—	ns
t_{AA}	Clock to Output	SCL LOW to SDA Data Out Valid	0.1	0.9	µs
t_R	SCL and SDA Rise Time(1)		—	300	ns
t_F	SCL and SDA Fall Time(1)		—	300	ns
t_{WR}	Write Cycle Time		—	10	ms

Note:

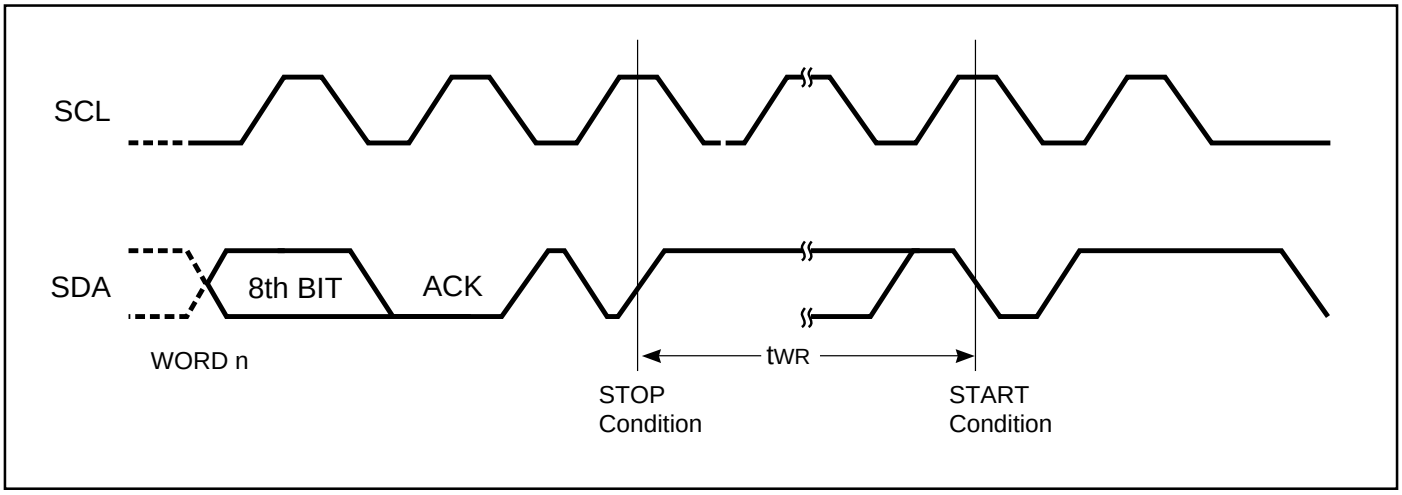
1. This parameter is characterized but not 100% tested.

AC WAVEFORMS

BUS TIMING



WRITE CYCLE



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Frequency	Order Part Number	Package
400 KHz	IS24C64-P	300-mil Plastic DIP
400 KHz	IS24C64-G	Small Outline (JEDEC STD)

ORDERING INFORMATION

Industrial Range: –40°C to +85°C

Frequency	Order Part Number	Package
400 KHz	IS24C64-PI	300-mil Plastic DIP
400 KHz	IS24C64-GI	Small Outline (JEDEC STD)

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