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20V MOSFETs for DC-DC Converters in Desktop Computers and Servers

Dragan Mariæ and Ralph Monteiro
International Rectifier
233 Kansas Street
El Segundo, CA 90245

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Abstract - *The challenge for distributed power supply engineers is to design a fast switching DC-DC converter with improved transient response, while still maintaining or increasing efficiency. This has to be achieved in the tight thermal envelope required for reliable system operation and at minimal cost. This paper discusses the use of 20V MOSFETs for the economical design of high efficiency DC-DC converters, replacing more expensive 30V MOSFETs in desktop computers and servers.*

I. INTRODUCTION

Computers constitute one of the most competitive and rapidly evolving markets in the world. Worldwide PC shipments reached nearly 130 million units in 2001 and are expected to reach more than 200 million by 2004, consuming more electronic components than any other application [1]. While growth in the PC market continues to be driven by additional features, data storage capacity and improved user friendliness, a new sub-$1000 PC market is growing, making cost effectiveness more important than ever before. At the same time, with each introduction of new faster GHz class processors from Intel or AMD for desktop and server computers, higher frequency DC-DC converters are required to meet the transient response requirements of the new processors. The challenge for distributed power supply engineers is to design efficient switching DC-DC converters with fast transient response. This has to be achieved in the tight thermal envelope required for reliable system operation and at minimal cost. This paper discusses the use of 20V MOSFETs for the economical design of high efficiency DC-DC converters, replacing more expensive 30V MOSFETs in desktop computers and servers. The discussion includes an example of MOSFET selection for a synchronous buck circuit and an evaluation of in-circuit efficiency and thermal performance of the new MOSFETs against the current commercial solutions. The ruggedness and reliability of the new 20V MOSFET technology is also discussed.

II. UNDERSTANDING POWER LOSSES IN DC-DC BUCK CONVERTERS

Latest CPU voltage-regulator specifications from Intel and AMD call for load current slew rates of 400A/µs and peak currents in excess of 100A [2]. The core supply voltage of the CPU must remain within its specified tolerance even when the processor performs a current-load step from a low current "sleep mode" to a high current "active mode" in a single clock cycle. In order to achieve fast transient response circuit designers tend to increase operating frequency. Maintaining or increasing power supply efficiency while increasing frequency is a daunting task that has to be achieved by meticulous design. Understanding power losses in a synchronous buck converter is a necessary step to design a high performance DC-DC converter.

The desktop power management system uses a distributed architecture. An AC-DC power supply is used to convert the AC line voltage (85-265V) down to 12VDC. This 12V regulated DC voltage is then converted down to the voltage required by the CPU using a 12V input, sub 2-volt output synchronous buck converter.

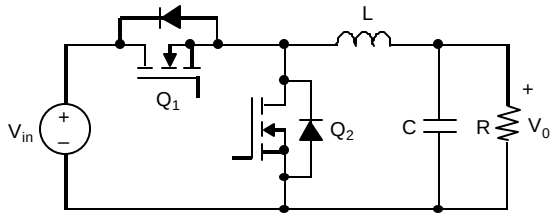


Fig. 1. Synchronous Buck Converter Block-Diagram.

Depending on the current level required, a single or multiphase buck converter is used. Fig. 1 shows a synchronous buck converter, where Q1 is the control FET and Q2 is the synchronous FET.

As shown in Fig. 2, power MOSFETs account for more than half the power loss in a buck converter – an important fact in an application that is critically dependent on efficiency. After further examination, losses can be divided into two FETs, control (Q1) and synchronous (Q2), then calculated using the following approximate equations [3]:

$$P_{loss\ Q1} = (I_{rms}^2 \times R_{DS(on)}) + (I \times Q_{sw}/I_g \times V_{in} \times f) + (Q_g \times V_g \times f) + (Q_{oss}/2 \times V_{in} \times f) \quad \ldots (1)$$

$P_{loss\ Q1}$ = (conduction) + (Switching) + (Gate Drive) + (Output capacitance)

$$P_{loss\ Q2} = (I_{rms}^2 \times R_{DS(on)}) + (Q_g \times V_g \times f) + (Q_{oss}/2 \times V_{in} \times f) + (Q_{rr} \times V_{in} \times f) \quad \ldots (2)$$

$P_{loss\ Q2}$ = (conduction) + (Gate Drive) + (Output capacitance) + (Body Diode Reverse Recovery losses)

Q1 affects the switching speed, and as such, imposes very critical requirement to minimize the switching charge Q_{sw} and the gate resistance R_g, while maintaining a reasonable on-

resistance $R_{DS(on)}$. Ideally, optimum efficiency is best achieved when the switching loss and the conduction loss are approximately the same, giving equal weight to $R_{DS(on)}$ and Q_{sw}..

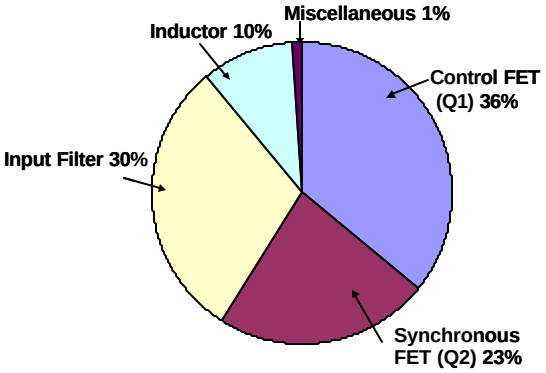


Fig. 2. Power Losses Of A Buck Converter; $12V_{IN}$, sub-$2V_{OUT}$ 300 kHz

The losses in the synchronous FET, Q2 are dominated by conduction losses. Therefore $R_{DS(on)}$ is the most important parameter for the synchronous FET. In practice, the lower the $R_{DS(on)}$ the better the efficiency, but this typically comes with increased cost. However, as the switching frequency approaches 1MHz, we need to keep in mind the power dissipated in the driver [4]. Therefore, low total gate charge Q_g of the synchronous FET offers a noticeable advantage.

III. SELECTING A MOSFET

In order to examine low voltage MOSFET technologies, efficiency measurements were made in a two-phase synchronous buck converter on Intel's DB850GB, one of the newer commercially available Pentium-4 motherboards [5]. This DC-DC converter design has a 12-volt input and 40 Amp, 1.7-volt output. The buck converter was designed using two D-Pak 30 volt devices in the synchronous FET socket and a single 25V device in a D^2Pak in the control FET socket. A number of tests was performed to compare 20V MOSFETs with 30V MOSFETs using the same silicon technology as well as commercially available 30V MOSFETs. Specifications for the MOSFETs are shown in Table I.

TABLE I: SPECIFICATION COMPARISON.

Component	BV_{DSS} V	$R_{DS(on)}$ mΩ	Q_G nC	Q_{GD} nC	Q_{GS} nC	Q_{SW} nC
IRFR3704	20	9	19	6.4	8.1	8
IRFR3711	20	6.5	29	8.9	7.3	10.4
IRFR3707	30	12.5	19	6.3	8.2	7.9
IRLR8103V	30	7.9	27	9.7	6.7	11
*Current Solution CTRL FET	25	12	26	11	7.6	12.5
Current Solution SYNC. FET	30	7	70	10	16	13.2

* Note: D^2Pak Device, all others D-Pak

Since the control MOSFET Q1 is used to regulate the output voltage by adjusting its duty cycle, it must be capable of fast switching and have low charge parameters. The IRFR3704 was designed using advanced planar technology [6] to meet the control FET socket requirements as can be seen from Table 1. Similarly, the advanced planar process was used to design a low $R_{DS(on)}$ IRFR3711 for the synchronous FET socket. In-circuit comparison was made using the following combinations of MOSFETs to validate the above analysis:

1. Current competitor's solution
2. IRFR3707 with IRLR8103V
3. IRFR3707 with IRFR3711
4. IRFR3704 with IRFR3711
5. IRFR3704 with IRFR3704

The efficiency curves are shown in Fig. 3. A careful selection of matched pairs of the control and synchronous MOSFETs significantly increases converter efficiency. Replacing the original devices with a 30-volt device pair, which uses the advanced planar technology, increases efficiency by 3%. An additional gain of 0.5% can be achieved by replacing the 30-volt synchronous FET with a 20-volt device which has a lower $R_{DS(on)}$. Replacing the 30V control MOSFET with a 20V MOSFET increases efficiency by additional 0.8%. The combination with the IRFR3704 in

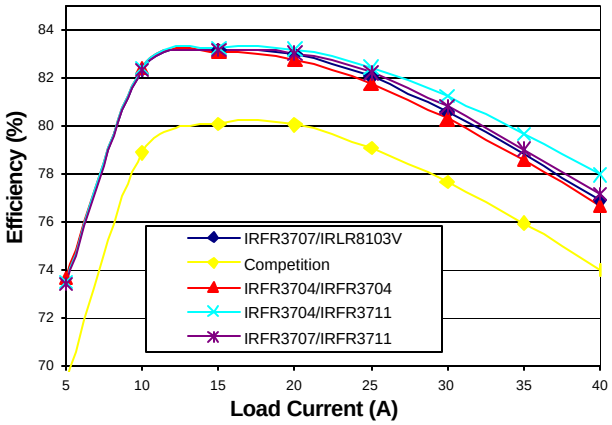


Fig. 3: Efficiency for the device pairs at 220 kHz operating frequency.

all sockets was included since designers sometimes prefer to use the same MOSFET as a control FET and a synchronous FET. This confirms that the best performance is obtained using the IRFR3704 as the control FET and two IRFR3711s as synchronous FETs to achieve efficiency improvements by over 4% at 220kHz compared to the original devices in the circuit.

The efficiency improvement is even more significant at higher switching frequencies. Fig. 4 below shows these same

MOSFET combinations but at almost double the switching frequency (410 KHz vs. 220 KHz). It should be noted that the 20-volt device efficiency still increased by 1.5% vs our 30-volt devices while the currently used devices went into thermal runaway.

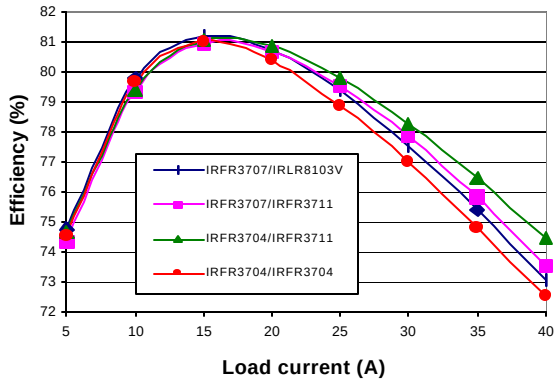


Fig. 4: Efficiency for the device pairs. 410 kHz operating frequency.

IV. THERMAL CONSIDERATIONS

Higher operating frequencies are required to improve transient response and to enable high current solutions in a compact footprint. As the size of the power supply shrinks, thermal management becomes increasingly difficult, as there is less and less area to dissipate the heat generated by the various components. As passives shrink in size, most of the power losses in a DC-DC converter are generated in the power semiconductors making them the major contributor to power losses. Increased silicon efficiency can improve the performance of the converter while reducing solution footprint. For example, a D-Pak MOSFET with more efficient silicon requires a smaller copper pad area on the PCB board to act as a heat sink, thus reducing board space.

Each of the device pairs mentioned above were run at the 40 amps maximum current in the 2-phase DC-DC converter at 220 kHz and, again, at 440 kHz. The best performing devices are the IRFR3704 and the IRFR3711 combination. Infrared camera photographs at 220kHz are shown in Fig. 5. for the 20V pair and in Fig. 6. for the original MOSFETs. As can be seen, a 12°C drop in juntion temperature can be achieved when using 20V devices instead of the currently used 30V devices. This can contribute to improved efficiency and longer life as board temperature is reduced.

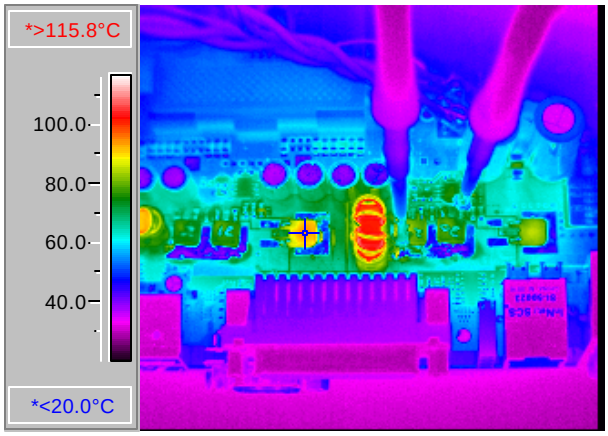


Fig 5: Infrared camera photograph, IRFR3704 with two IRFR3711, f_{SW}=220KHz, I_{out}=40A: max. case 94.2°C, max. lead 81.2°C.

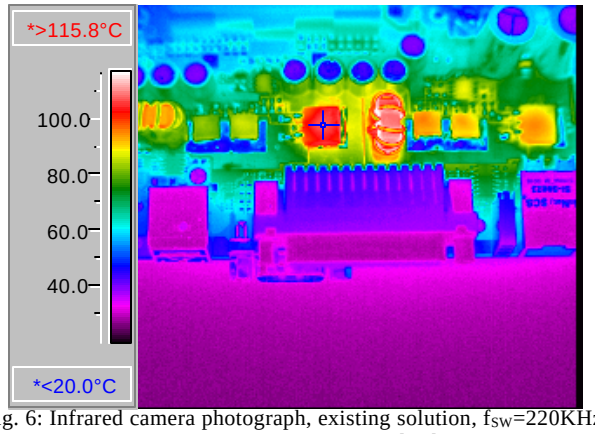


Fig. 6: Infrared camera photograph, existing solution, f_{SW}=220KHz, I_{out}=40A: max. case 106.7°C, max. lead 90.4°C.

V. RELIABILITY OF 20V MOSFET TECHNOLOGY

20V MOSFETs provide the necessary breakdown voltage when 12V bus is used. However when the synchronous FET Q2 is turned off, as the drain to source voltage rises fast, some ringing is observed that could go above the 12V. Comparisons of V_{DS} and V_{GS} waveforms were made to monitor the ringing when using a 20V MOSFET vs. using a 30V MOSFET. Measurements were made at full load of 40A. Fig. 7. shows the V_{DS} and V_{GS} waveforms for the sync. FET IRFR3711 with IRFR3704 as the control FET. Fig. 8. shows those for the originally used competitor's 30V devices. Comparing V_{DS} waveforms in Figs. 7. and 8, we can see that there is no increased ringing and the maximum voltage is about 15V, which is well within the 20V breakdown voltage for the IRFR3711. The high side control FET will not see a voltage higher than 5-10% over 12V, which is well within the reverse blocking capability of the MOSFET. Thus the new 20V MOSFET pair can be used reliably in desktop CPU power supplies.

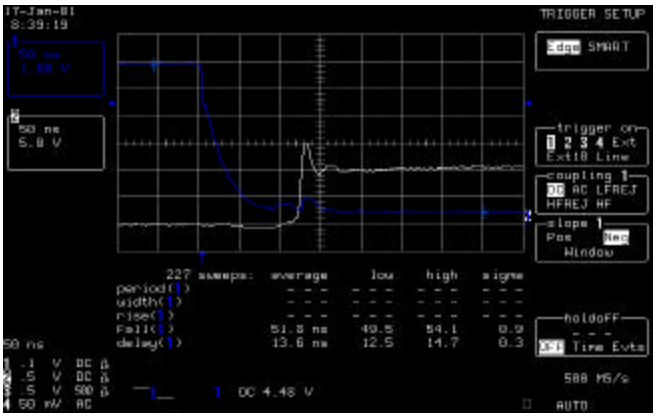
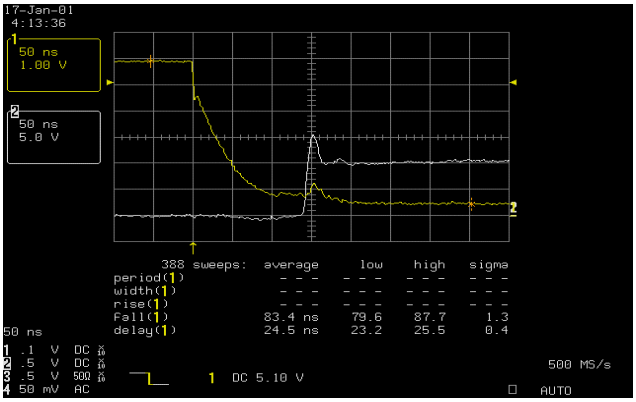


Fig. 7: V_{DS} and V_{GS} for synchronous switch, IRFR3711, with IRFR3704.



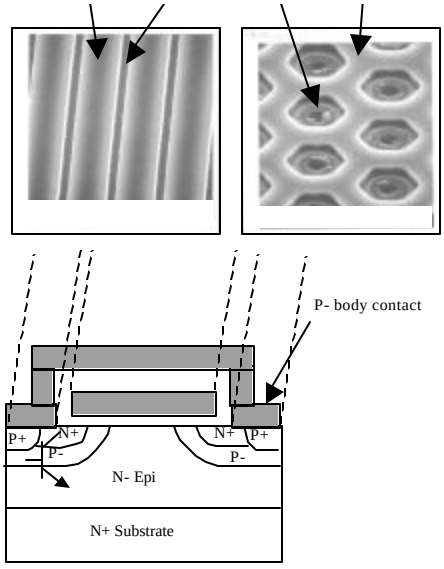


Fig. 9. Photo of the novel planar versus older cell topology and cross-section of power MOSFET showing parasitic bipolar transistor.

Our new 20V MOSFETs are manufactured using an advanced planar process that is extremely rugged. This new process provides much higher ruggedness compared to older cell topology. The novel approach results in the immunity of the parasitic bipolar transistor from undesirable turn-on by minimizing the parasitic base resistance R_b under the N+ source and also ensuring the source is always shorted to the P- body. This implies a significantly higher avalanche rating when compared to the trench technology and conventional cellular structures. For example, the single pulse avalanche rating of the IRFR3704 is 216mJ while that of the competitor's 25V control FET is 60mJ.

The 20V gate rating also contributes to the ruggedness of the design. The new stripe planar versus cell structure for the two technologies is shown in Fig. 9, along with a cross-section of a power MOSFET illustrating the inherent parasitic bipolar transistor [6].

The finer geometry of the new planar technology contributes to an increase in channel width per unit area (optimized W/L), which ensures lower $R_{DS(on)}$ values achievable. The geometry also results in lower gate charge when compared to cellular geometries, which becomes increasingly critical as the operating frequency goes up.

VI. Conclusion

Improved efficiency and better thermals are the goals of all power supply designers. Choosing the best MOSFET is a very important task, more so with many new devices available and the cost/performance tradeoff. We developed robust 20 volt rated components to deliver significantly higher efficiency and lower temperatures than the components currently used on flagship motherboard designs. New 20-volt MOSFETs based on our advanced novel process deliver excellent performance along with higher current capabilities. Combined with additional cost savings these devices are an excellent alternative to the current 30-volt devices for the price sensitive, performance driven DC-DC converters for computers.

Acknowledgement

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