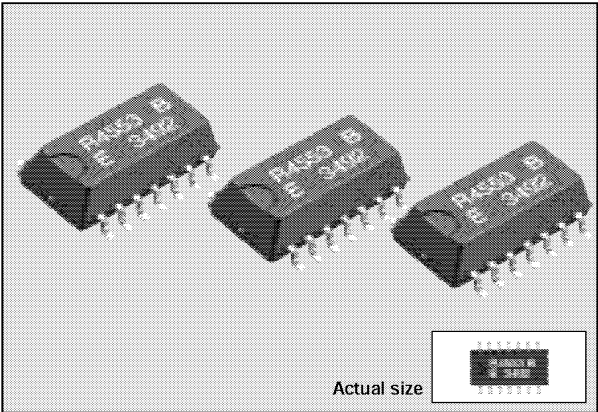


Real time clock module

SERIAL-INTERFACE REAL TIME CLOCK MODULE

RTC-4553

- Built-in crystal unit allows adjustment-free efficient operation.
- The small package makes high-density mounting possible. (SOP 14-pin)
- Automatic calendar function (year, month, day, day of the week, hour, minute, second).
- Automatic leap year correction. (up to 2099)
- Built-in 30 x 4-bit S-RAM.
- High-speed access.
- Reference pulse output. (1024 Hz, 1/10 Hz)
- Low current consumption. (1 μ A typical)
- Similar mounting method to that used for universal type SMD IC.



Specifications (characteristics)

Absolute Max. rating

Item	Symbol	Condition	Min.	Max.	Unit
Supply voltage	V _{DD}	V _{DD} -GND	-0.3	+6.0	V
Input voltage	V _{IN}	S _{IN} , S _{CK} , WR, CS ₀ , CS ₁		V _{DD} +0.3	
Output voltage	V _{OUT}	S _{OUT} , T _{POUT}			
Storage temperature	T _{STG}	Stored without tape & reel	-55	+125	°C
Soldering conditions	T _{SOL}		Twice at under 260°C within 10 sec. or under 230°C within 3 min.		

Operating range

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	V_{DD}	—	2.7	5.0	5.5	V
Operating temperature	T_{OPR}		-30	—	+70	$^{\circ}$ C

Frequency characteristics

Item	Symbol	Condition		Range	Unit
Frequency tolerance	$\Delta f/f_0$	Ta=25°C, VDD=5V	AA	5±5	ppm
			A	5±10	
			B	5±20	
Frequency temperature characteristics	T _{op}	Ta=-10 to 70°C, VDD=5V Reference at 25°C		+10 -120	ppm/ year
Frequency voltage characteristics	f _v	Ta=Fix, VDD=2 to 5.5V Reference at 5V		±5	
Aging	f _a	Ta=25°C, VDD=5V, first year			

DC characteristics

● $V_{DD}=5V\pm10\%$ (GND=0V, $T_a=-30^{\circ}$ C to +70 $^{\circ}$ C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Data holding voltage	V_{DH}	—	2.0	—	5.5	V
Current consumption	I_{DD1}	$S_{CK}=500$ kHz	—	—	100	μ A
	I_{DD2}	$S_{CK}=0$ Hz	—	1.0	3.0	
Output voltage	V_{OH}	$I_{OH}=-400\mu$ A $V_{DD}-0.4$	—	—	—	V
	V_{OL}	$I_{OL}=1.6$ mA	—	—	0.4	
Off leak current	I_{OZH}	$V_{OUT}=5.5$ V	-2.0	—	2.0	μ A
	I_{OZL}	$V_{OUT}=0$ V	—	—	—	
Input voltage	V_{IH}	—	4/5 V_{DD}	—	—	V
	V_{IL}	—	—	—	1/5 V_{DD}	
Input current	I_{IH}	$V_{IN}=5.5$ V	-2.0	—	2.0	μ A
	I_{IL}	$V_{IN}=0$ V	—	—	—	
Oscillation start-up time	T_{OSC}	$T_a=25^{\circ}$ C	—	—	3.0	s

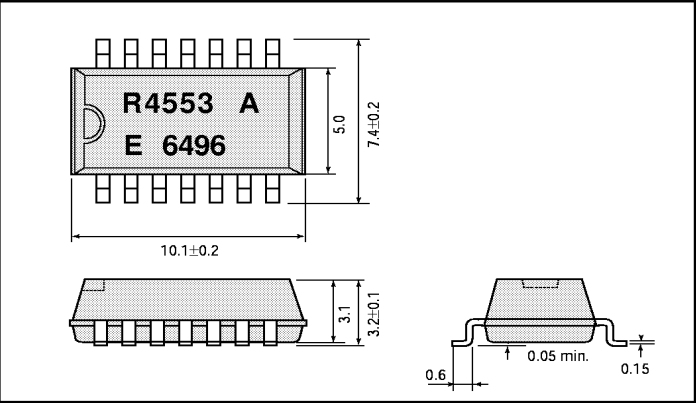
Terminal connection

No.	Pin terminal	No.	Pin terminal
1	GND	14	TP_{OUT}
2	$\overline{WR}$	13	S_{OUT}
3	S_{IN}	12	CS_1
4	S_{CK}	11	CS_0
5	L1	10	L5
6	L2	9	L4
7	L3	8	V_{DD}

L1 to L5 are test pin. Do not connect them to any terminals.

External dimensions

(Unit: mm)



● $V_{DD}=3V\pm10\%$ (GND=0V, $T_a=-30^{\circ}$ C to +70 $^{\circ}$ C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Data holding voltage	V_{DH}	—	2.0	—	3.3	V
Current consumption	I_{DD1}	$S_{CK}=300$ kHz	—	—	100	μ A
	I_{DD2}	$S_{CK}=0$ Hz	—	1.0	3.0	
Output voltage	V_{OH}	$I_{OH}=-400\mu$ A $V_{DD}-0.4$	—	—	—	V
	V_{OL}	$I_{OL}=1.6$ mA	—	—	0.4	
Off leak current	I_{OZH}	$V_{OUT}=3.3$ V	-2.0	—	2.0	μ A
	I_{OZL}	$V_{OUT}=0$ V	—	—	—	
Input voltage	V_{IH}	—	4/5 V_{DD}	—	—	V
	V_{IL}	—	—	—	1/5 V_{DD}	
Input current	I_{IH}	$V_{IN}=3.3$ V	-2.0	—	2.0	μ A
	I_{IL}	$V_{IN}=0$ V	—	—	—	
Oscillation start-up time	T_{OSC}	$T_a=25^{\circ}$ C	—	—	3.0	s

Register table

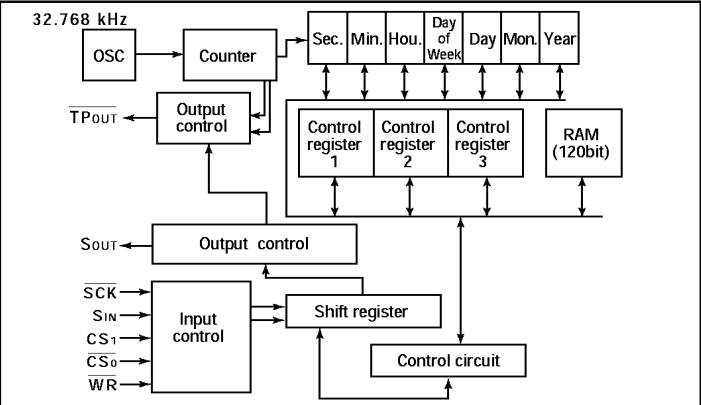
Address					MODE 0						MODE 1				MODE 2			
					Register symbol	Counter control register					User RAM Domain 1				User RAM Domain 2			
						D ₃	D ₂	D ₁	D ₀	Register name	D ₃	D ₂	D ₁	D ₀	D ₃	D ₂	D ₁	D ₀
0	0	0	0	0	S ₁	S ₈	S ₄	S ₂	S ₁	1-second digit register	RA ₃	RA ₂	RA ₁	RA ₀	RA ₆₃	RA ₆₂	RA ₆₁	RA ₆₀
1	0	0	0	1	S ₁₀	0	S ₄₀	S ₂₀	S ₁₀	10-second digit register	RA ₇	RA ₆	RA ₅	RA ₄	RA ₆₇	RA ₆₆	RA ₆₅	RA ₆₄
2	0	0	1	0	MI ₁	mi ₈	mi ₄	mi ₂	mi ₁	1-minute digit register	RA ₁₁	RA ₁₀	RA ₉	RA ₈	RA ₇₁	RA ₇₀	RA ₆₉	RA ₆₈
3	0	0	1	1	MI ₁₀	0	mi ₄₀	mi ₂₀	mi ₁₀	10-minute digit register	RA ₁₅	RA ₁₄	RA ₁₃	RA ₁₂	RA ₇₅	RA ₇₄	RA ₇₃	RA ₇₂
4	0	1	0	0	H ₁	h ₈	h ₄	h ₂	h ₁	1-hour digit register	RA ₁₉	RA ₁₈	RA ₁₇	RA ₁₆	RA ₇₉	RA ₇₈	RA ₇₇	RA ₇₆
5	0	1	0	1	H ₁₀	PM/AM	0	h ₂₀	h ₁₀	10-hour digit register	RA ₂₃	RA ₂₂	RA ₂₁	RA ₂₀	RA ₈₃	RA ₈₂	RA ₈₁	RA ₈₀
6	0	1	1	0	W	0	w ₄	w ₂	w ₁	Day of the week digit register	RA ₂₇	RA ₂₆	RA ₂₅	RA ₂₄	RA ₈₇	RA ₈₆	RA ₈₅	RA ₈₄
7	0	1	1	1	D ₁	d ₈	d ₄	d ₂	d ₁	1-day digit register	RA ₃₁	RA ₃₀	RA ₂₉	RA ₂₈	RA ₉₁	RA ₉₀	RA ₈₉	RA ₈₈
8	1	0	0	0	D ₁₀	0	0	d ₂₀	d ₁₀	10-day digit register	RA ₃₅	RA ₃₄	RA ₃₃	RA ₃₂	RA ₉₅	RA ₉₄	RA ₉₃	RA ₉₂
9	1	0	0	1	MO ₁	mo ₈	mo ₄	mo ₂	mo ₁	1-month digit register	RA ₃₉	RA ₃₈	RA ₃₇	RA ₃₆	RA ₉₉	RA ₉₈	RA ₉₇	RA ₉₆
A	1	0	1	0	MO ₁₀	0	0	0	mo ₁₀	10-month digit register	RA ₄₃	RA ₄₂	RA ₄₁	RA ₄₀	RA ₁₀₃	RA ₁₀₂	RA ₁₀₁	RA ₁₀₀
B	1	0	1	1	Y ₁	y ₈	y ₄	y ₂	y ₁	1-year digit register	RA ₄₇	RA ₄₆	RA ₄₅	RA ₄₄	RA ₁₀₇	RA ₁₀₆	RA ₁₀₅	RA ₁₀₄
C	1	1	0	0	Y ₁₀	y ₈₀	y ₄₀	y ₂₀	y ₁₀	10-year digit register	RA ₅₁	RA ₅₀	RA ₄₉	RA ₄₈	RA ₁₁₁	RA ₁₁₀	RA ₁₀₉	RA ₁₀₈
D	1	1	0	1	C ₁	TPS	30ADJ	CNTR	24/12	Control register 1	RA ₅₅	RA ₅₄	RA ₅₃	RA ₅₂	RA ₁₁₅	RA ₁₁₄	RA ₁₁₃	RA ₁₁₂
E	1	1	1	0	C ₂	BUSY	PONC	—	*	Control register 2	RA ₅₉	RA ₅₈	RA ₅₇	RA ₅₆	RA ₁₁₉	RA ₁₁₈	RA ₁₁₇	RA ₁₁₆
F	1	1	1	1	C ₃	SYSR	TEST	MS ₁	MS ₀	Control register 3	Same as MODE 0				Same as MODE 0			

Note: * TEST bit should be "0".

Switching characteristics (Ta=-30°C to +70°C, VDD=5V±10%, GND=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK input frequency	f _{SCK}	—	—	—	500	kHz
SCK "L" time	t _{WSCKL}	—	—	—	—	—
SCK "H" time	t _{WSCKH}	—	1.0	—	—	—
SCK pause time	t _{PS}	—	—	—	—	—
CS ₀ setup time	t _{SCS}	—	0	—	—	μs
CS ₀ hold time	t _{HCS}	—	0.5	—	—	μs
S _{IN} data setup time	t _{SD}	—	0.2	—	—	μs
S _{IN} data Hold time	t _{HD}	—	—	—	—	μs
WR setup time	t _{SWR}	—	1.0	—	—	μs
WR hold time	t _{HWR}	—	0.5	—	—	μs
S _{OUT} delay time	t _{DSO}	—	—	150	500	ns
CS ₀ and CS ₁ enable to S _{OUT} output	t _{DSZ1}	C _L =100pF	—	—	100	ns
CS ₀ disable to S _{OUT} high Z	t _{DSZ2}	—	—	—	—	ns
CS ₁ enable to S _{OUT} output	t _{DPZ1}	—	—	—	—	ns
CS ₁ enable to S _{OUT} high Z	t _{DPZ2}	—	—	—	—	ns

Block diagram



Timing chart

