2.0 Programming Description

2.1 MICROWIRE™ Interface

The MICROWIRE™ interface is comprised of an 18 bit shift register, a R register and a N register. The shift register consists of a 17 bit DATA field and a 1 bit address (ADDR) field as shown below. When Latch Enable transitions HIGH, data stored in the shift register is loaded into either the R or N register depending on the ADDR bit as described in Table 2.1.1. The data is loaded MSB first. The DATA field assignment for the R and N registers are shown in Table 2.1.2 below.

MSB		LSB
DATA [16:0]		ADDR
17	1	0

2.1.1 Address bit Truth Table

When LE is transitioned high, data is transferred from the 18-bit shift register into either the 14-bit R register, or the 17 bit N register depending upon the state of the ADDR bit.

ADDR	DATA Location
0	N register
1	R register

2.1.2 Register Content Truth Table

	First Bit					SHIFT REGISTER BIT LOCATION											Last Bit
	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
N register	NB_CNTR										NA_CNTR					CTL_WORD		0
R register	X	X	X	TEST	RS	PD_POL	CP_TRI	R_CNTR										1

2.2 R REGISTER

If the Address Bit (ADDR) is 1, when LE is transitioned high data is transferred from the 18-bit shift register into the 14-bit R register. The R register contains a latch which sets the PLL 10-bit R counter divide ratio. The divide ratio is programmed using the bits R_CNTR as shown in Table 2.2.1. The ratio must be ≥ 2. The PD_POL, CP_TRI and TEST bits control the phase detector polarity, charge pump tri-state, and test mode respectively, as shown in Table 2.2.2 . The RS bit is reserved and should always be set to zero. X denotes a don't care condition.

First Bit					SHIFT REGISTER BIT LOCATION												Last Bit
17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	TEST	RS	PD_POL	CP_TRI	R_CNTR[9:0]										1

2.2.1 10-BIT PROGRAMMABLE REFERENCE DIVIDER RATIO (R COUNTER)

R_CNTR										
Divide Ratio	9	8	7	6	5	4	3	2	1	0
2	0	0	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	0	0	1	1
•	•	•	•	•	•	•	•	•	•	•
1,023	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio: 2 to 1,023 (Divide ratios less than 2 are prohibited)
R_CNTR - These bits select the divide ratio of the programmable reference dividers

2.2.2 R Register Truth Table

BIT	LOCATION	FUNCTION	0	1
CP_TRI	R[11]	Charge Pump TRISTATE	Normal operation	TRISTATE
PD_POL	R[12]	Phase Detector Polarity	Negative	Positive
TEST	R[14]	Test mode bit	Normal operation	Test mode

If the test mode is NOT activated (R[14]=0), the charge pump is active when CP_TRI is set LOW. When CP_TRI is set HIGH, the charge pump output and phase comparator are forced to a TRI-STATE condition. This bit must be set HIGH if the test mode is ACTIVATED (R[14]=1).
If the test mode is NOT activated (R[14]=0), PD_POL sets the VCO characteristics to positive when set HIGH. When PD_POL is set LOW, the VCO exhibits a negative characteristic where the VCO frequency decreases with increasing control voltage.
If the test mode is ACTIVATED (R[14]=1), the outputs of the N and R counters are directed to the CPo output to allow for testing. The PD_POL bit selects which counter output according to Table 2.2.3.

2.2.3 Test mode truth table (R[14] = 1)

CPo Output	CP_TRI R[11]	PD_POL R[12]
R divider output	1	0
N divider output	1	1

2.3 N REGISTER

If the address bit is LOW (ADDR=0), when LE is transitioned high, data is transferred from the 18-bit shift register into the 17-bit N register. The N register consists of the 5-bit swallow counter (A counter), the 10 bit programmable counter (B counter) and the control word. Serial data format is shown below in tables 2.3.1 and 2.3.2. The pulse swallow function which determines the divide ratio is described in section 2.3.3.

First Bit	SHIFT REGISTER BIT LOCATION																Last Bit
17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NB_CNTR [9:0]										NA_CNTR[4:0]					CTL_WORD[1:0]		0

2.3.1 5-BIT SWALLOW COUNTER DIVIDE RATIO (A COUNTER)

Swallow Count	NA_CNTR				
(A)	4	3	2	1	0
0	0	0	0	0	0
1	0	0	0	0	1
•	•	•	•	•	•
31	1	1	1	1	1

Notes: Swallow Counter Value: 0 to 31

NB_CNTR ≥ NA_CNTR

2.3.2 10-BIT PROGRAMMABLE COUNTER DIVIDE RATIO (B COUNTER)

	NB_CNTR									
Divide Ratio	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•
1023	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio: 3 to 1,023(Divide ratios less than 3 are prohibited)

NB_CNTR ≥ NA_CNTR

2.3.3 PULSE SWALLOW FUNCTION

The N divider counts such that it divides the VCO RF frequency by (P+1) A times, and then divides by P(B-A) times. The B value (NB_CNTR) must be ≥ 3. The continuous divider ratio is from 992 to 32,767. Divider ratios less than 992 are achievable as long as the binary counter value is greater than the swallow counter value (NB_CNTR ≥ NA_CNTR).

$fvco = N \times (fosc / R)$

$N = (P \times B) + A$

- fvco: Output frequency of external voltage controlled oscillator (VCO)
- fosc: Output frequency of the external reference frequency oscillator
- R: Preset divide ratio of binary 10-bit programmable reference counter (2 to 1023)
- N: Preset divide ratio of main 15-bit programmable integer N counter (992 to 32,767)
- B: Preset divide ratio of binary 10-bit programmable B counter (3 to 1023)
- A: Preset value of binary 5-bit swallow A counter ($0 \le A \le 31$, $A \le B$)
- P: Preset modulus of dual modulus prescaler (P=32)

2.3.4 CTL_WORD

MSB **LSB**

N1	N0
CNT_RST	PWDN

2.3.4.1 Reserve Word Truth Table

CE	CNT_RST	PWDN	FUNCTION
1	0	0	Normal Operation
1	0	1	Synchronous Powerdown
1	1	0	counter reset
1	1	1	Asynchronous Powerdown
0	X	X	Asynchronous Powerdown

Notes:

X denotes don't care.

1. The **Counter Reset** bit when activated allows the reset of both N and R counters. Upon powering up the N counter resumes counting in "close" alignment with the R counter. (The maximum error is one prescalar cycle).

2. Both synchronous and asynchronous **power down** modes are available with the LMX2322 to be able to adapt to different types of applications. The MICROWIRE control register remains active and capable of loading and latching in data during all of the powerdown modes

Synchronous Power down Mode

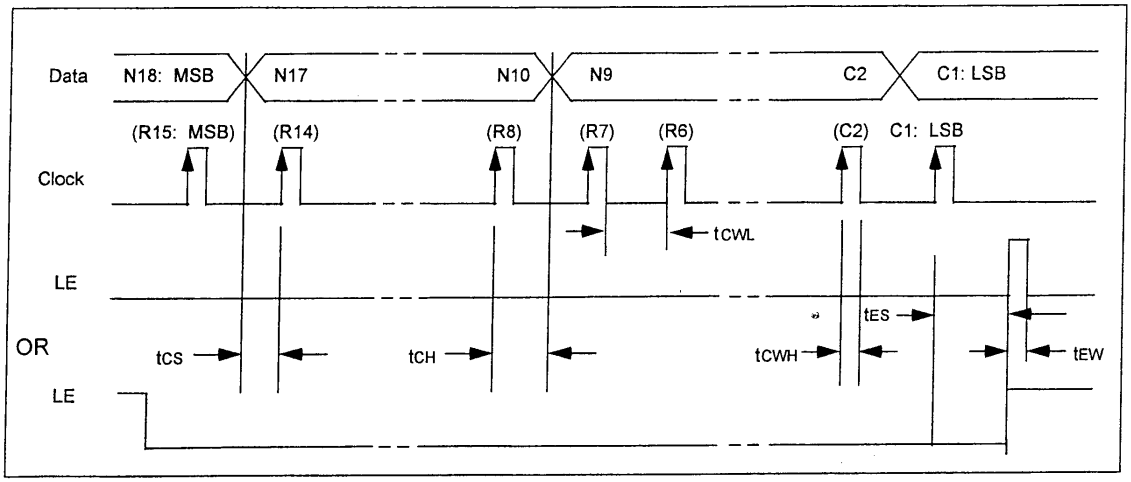
The PLL loops can be synchronously powered down by setting the counter reset mode bit to LOW (N[1] = 0) and its power down mode bit to HIGH (N[0] = 1). The power down function is gated by the charge pump. Once the power down mode and counter reset mode bits are loaded, the part will go into power down mode upon the completion of a charge pump pulse event.

Asynchronous Power down Mode

The PLL loops can be asynchronously powered down by setting the counter reset mode bit to HIGH (N[1] = 1) and its power down mode bit to HIGH(N[0] = 1). The power down function is NOT gated by the charge pump. Once the power down and counter reset mode bits are loaded, the part will go into power down mode immediately.

The R and N counters are disabled and held at load point during the synchronous and asynchronous power down modes. This will allow a smooth acquisition of the RF signal when the PLL is programmed to power up. Upon powering up, both R and N counters will start at the 'zero' state, and the relationship between R and N will not be random.

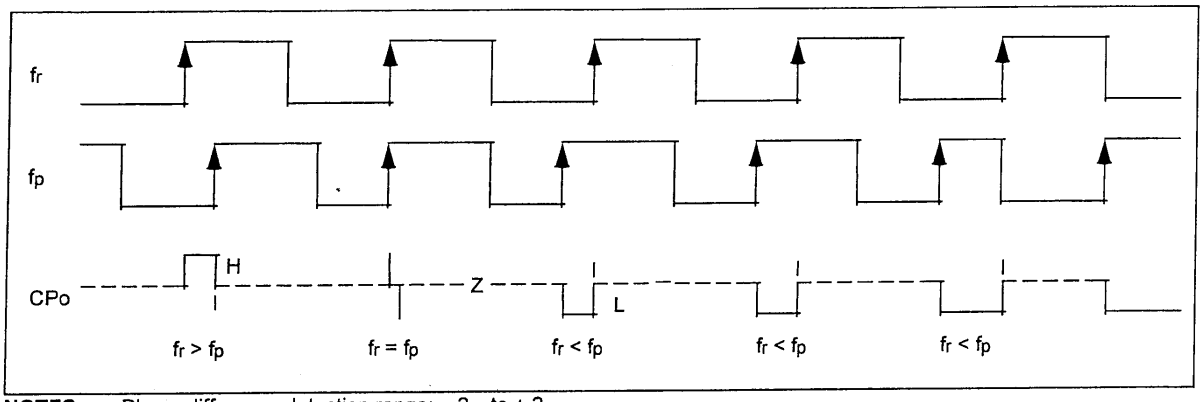
SERIAL DATA INPUT TIMING



NOTES: Parenthesis data indicates programmable reference divider data.
Data shifted into register on clock rising edge.
Data is shifted in MSB first.

TEST CONDITIONS: The Serial Data Input Timing is tested using a symmetrical waveform around Vcc/2. The test waveform has an edge rate of 0.6 V/nsec with amplitudes of 2.2V @ Vcc=2.7 V and 2.6V @ Vcc = 3.9 V.

PHASE COMPARATOR AND INTERNAL CHARGE PUMP CHARACTERISTICS



NOTES: Phase difference detection range: -2π to $+2\pi$
The minimum width pump up and pump down current pulses occur at the CPo pin when the loop is locked.
PD_POL = 1
f_R: Phase comparator input from the R Divider
f_P: Phase comparator input from the N divider
CPo: Charge pump output