

SANYO

No. 2169C

LC7537N, 7537AN, 7537NE

Electronic Volume Control System for Audio Equipment

Overview

The LC7537N is an electronic control LSI capable of electronically controlling the volume, balance, loudness, fader, bass, and treble functions individually with fewer externally connected component parts.

Features

- Enables controlling the below-listed functions with 3-line serial data, including CE, DI, and CLK. Also, due to 0 V to 5 V swing of the serial data input voltage, permits the use of a general purpose microcomputer.

Volume : Separately controls the Lch and Rch volume levels across 81 positions over the 0 dB to -79 dB (in 1 dB steps) range and $-\infty$, and consequently also serves balance control purposes.

Loudness : By virtue of a center tap provided at the -20 dB position of the volume controlling ladder resistors, permits loudness to be controlled with externally connected CR components.

Fader : By varying only the rear or front output level across 16 positions, provides fader functions (in 2 dB steps over the 0 dB to -20 dB range, and 5 dB steps over the -20 dB to -45 dB range, and at $-\infty$, for a total of 16 positions).

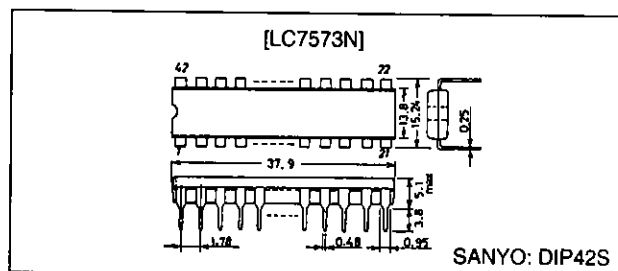
Bass/Treble : With CR components externally connected, forms an NF type tone control circuit (Baxandall type) to exercise control across 15 positions over both the bass and treble functions in 2 dB steps.

- By virtue of its CMOS structure, the LSI operates under a broad power supply voltage range from +4.5 V to +15 V, permitting the use of either a single or a dual $\pm$ power supply, whichever is preferred.

Package Dimensions

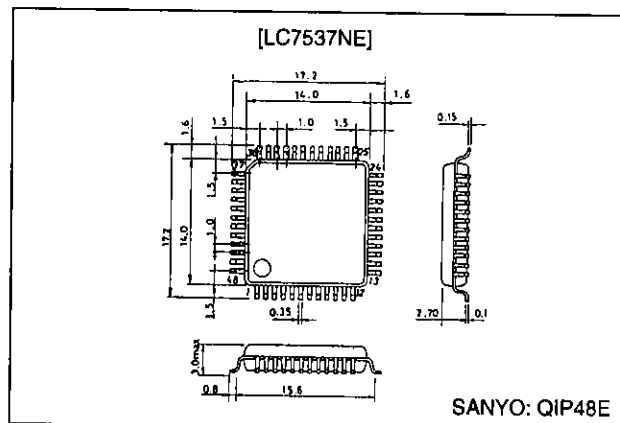
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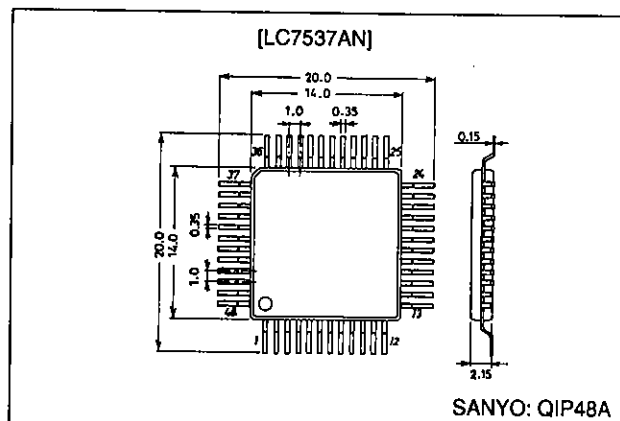
unit : mm

3156-QFP48E



unit : mm

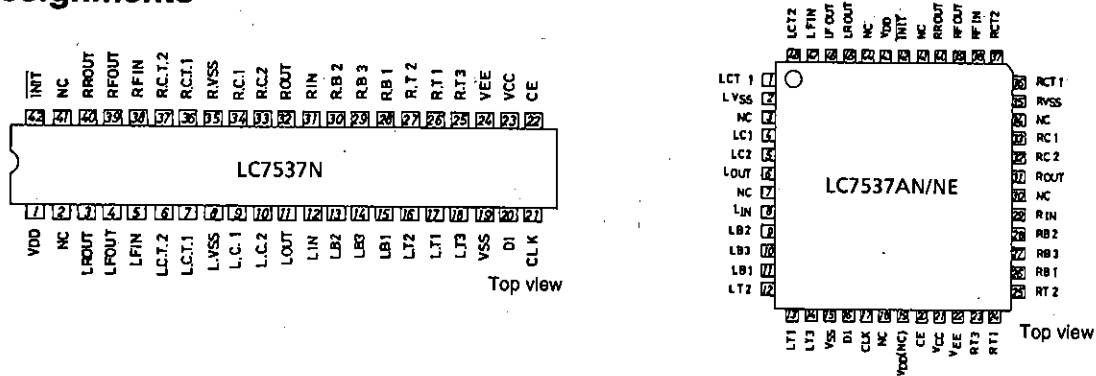
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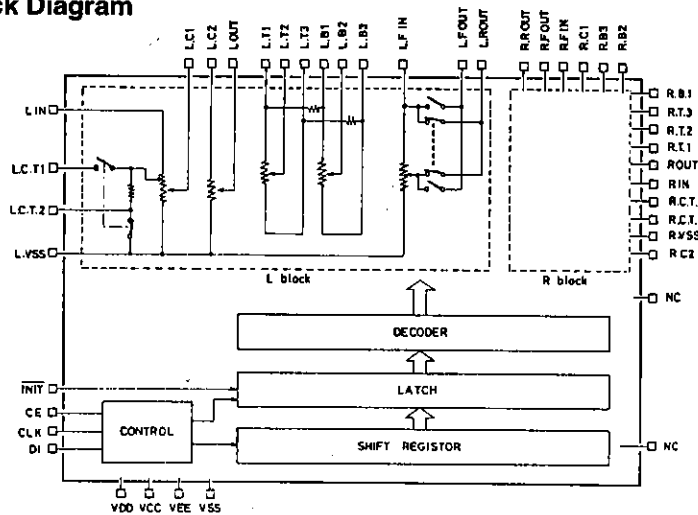
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Pin Assignments



Equivalent Circuit Block Diagram



Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$, $V_{DD} \geq V_{CC} > V_{SS} \geq V_{EE}$

Item	Symbol	Condition	Rating	Unit
Maximum supply voltage	$V_{DD} - V_{EE} \text{ max}$	$V_{DD}, V_{EE} : V_{EE} \geq -8\text{ V}$	16	V
	$V_{CC} \text{ max}$	$V_{CC} : V_{DD} \geq V_{CC}$	$V_{SS} - 0.3 \text{ to } V_{SS} + 7$	V
Input supply voltage	V_{I1}	DI, CLK, CE	$V_{SS} - 0.3 \text{ to } V_{DD} + 0.3$	V
	V_{I2}	INIT	$V_{SS} - 0.3 \text{ to } V_{DD} + 0.3$	V
Allowable power dissipation	$P_d \text{ max}$	$T_a \leq 85^\circ\text{C}$, (LC7537N, 7537AN)	200	mW
		$T_a \leq 85^\circ\text{C}$, (LC7537NE)	300	mW
Operating temperature	T_{opr}		$-40 \text{ to } +85$	$^\circ\text{C}$
Storage temperature	$T_{stg} *3$		$-50 \text{ to } +125$	$^\circ\text{C}$

Allowable Operating Conditions at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$, $V_{DD} \geq V_{CC} > V_{SS} \geq V_{EE}$

Item	Symbol	Condition	Rating	Unit
Supply voltage *1	$V_{DD} - V_{EE}$	$V_{EE} \geq -7.5\text{ V}$	4.5 to 15	V
	V_{CC}		4.5 to 5.5	V
Input high-level voltage	$V_{IH1} *2$	DI, CLK, CE	$0.8 V_{CC} \text{ to } V_{CC}$	V
	V_{IH2}	INIT	$0.8 (V_{DD} - V_{EE}) + V_{EE} \text{ to } V_{DD}$	V
Input low-level voltage	$V_{IL1} *2$	DI, CLK, CE	$V_{SS} \text{ to } 0.2 V_{CC}$	V
	V_{IL2}	INIT	$V_{EE} \text{ to } 0.2 (V_{DD} - V_{EE}) + V_{EE}$	V
Input signal amplitude	V_{IN}		$V_{EE} \text{ to } V_{DD}$	V_{p-p}
Input pulse width	t_{ow}		1 min	μs
setup time	$t_{set up}$		1 min	μs
Hold time	t_{hold}		1 min	μs
Operating frequency	f_{opg}		up to 330	kHz

Note: 1. A1000 pF or larger capacitor should be added on between each individual power supply terminal and V_{SS} .

2. When the microcomputer side control signals rise faster than V_{DD} for the LC7537, a 2 k Ω or higher resistor should be inserted midway on each of the DI, CLK, and CE lines.

3. When mounting the QIP package on the board, do not dip the entire package in solder. Only the LC7537NE may be dipped directly in solder during mounting.

LC7537N, 7537AN, 7537NE

Electrical Characteristics at Ta = 25°C, V_{DD} = +7.5 V, V_{EE} = -7.5 V, V_{CC} = +5 V

Item	Symbol	Condition	Rating			
			min	typ	max	Unit
Total harmonic Distortion	THD(1)	V _{IN} = 1 V, f = 1 kHz, all flat overall		0.005	0.01	%
	THD(2)	V _{IN} = 1 V, f = 20 kHz, all flat overall	0.006	0.02	%	
Crosstalk	CT	V _{IN} = 1 V, f = 1 kHz, all flat, R _g = 1 kΩ	60	95		dB
	V _{omin} (1)	V _{IN} = 1 V, f = 1 kHz, MAIN, VR = ∞, FADER VR = ∞	80	90		dB
Maximum attenuation output	V _{omin} (2)	V _{IN} = 1 V, f = 1 kHz, MAIN, VR = ∞, V _{DD} = 8 V, FADER VR = ∞, V _{EE} = V _{SS} = 0 V, C between V _{SS} and GND of L/R = 1000 μF	70	80		dB
VR resistance voltage	R _{VOL} (1)	5 dB-step	12	20	28	kΩ
	R _{VOL} (2)	1 dB-step	12	20	28	kΩ
	R _{BASS}		12	20	28	kΩ
	R _{TREBLE}		12	20	28	kΩ
	R _{FADER}		12	20	28	kΩ
Output noise	V _N (1)	All flat overall (I _{HFA}) R _g = 1 kΩ		2	10	μV
	V _N (2)	R _g = 1 kΩ, V _{DD} = 8 V, V _{EE} = V _{SS} = 0 V		2	10	μV
Current drain	I _{DD}	V _{DD} - V _{EE} = 15 V			1	mA
	I _{CC}	V _{CC} = 5 V			1	mA

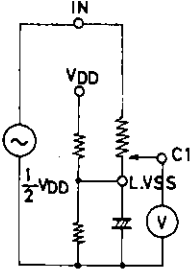
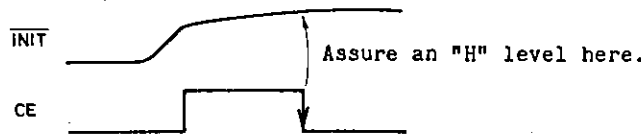
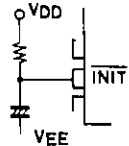
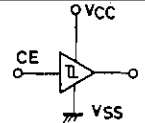
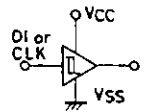
Pin Description () : LC7537AN, 7537NE

Pin No.	Symbol	Description of Functions	Remarks
12(8)	L.IN	Main volume control block 5 dB-step attenuator input terminals. These pins should be driven at a low impedance.	
31(29)	R.IN		
9(4)	L.C1	Main volume control block 5 dB-step attenuator output terminals. Having been designed to be open, the step positions will develop errors if at low acceptor impedances, so that as high load impedances as possible should be provided.	VR resistance : 20 kΩ
34(33)	R.C1		
10(5)	L.C2	Main volume control block 1 dB-step attenuator input terminals. These pins should be driven at a low impedance.	
33(32)	R.C2		
11(6)	L.OUT	Main volume control block 1 dB-step attenuator output terminals. Due to the step positions designed to be open, load impedances as high as possible should be provided to them, similar to those for the LC1 and RC1.	VR resistance : 20 kΩ
32(31)	R.OUT		
5(47)	L.FIN	Fader functions employing mode input terminals. These pins should be driven at a low impedance.	
38(38)	R.FIN		
4(46)	L.FOUT	Fader block output terminals. These pins permit the front and rear sides to be faded out independently of each other. Attenuations exercised on Lch will be the same as on Rch. Due to the step positions designed to be open, acceptor impedances as high as possible should be provided to them.	VR resistance : 20 kΩ
3(45)	L.ROUT		
39(39)	R.ROUT		
40(40)	R.ROUT		
15(11)	L.B1	Bass tone control block terminals. A total of 15 positions have been provided in 2 dB steps	VR resistance : 20 kΩ
16(9)	L.B2		
14(10)	L.B3		
28(26)	R.B1		
27(28)	R.B2		
29(27)	R.B3		
17(13)	L.T1	Treble tone control block terminals. A total of 15 positions have been provided in 2 dB steps. The VR resistance value is 20 kΩ.	VR resistance : 20 kΩ
16(12)	L.T2		
18(14)	L.T3		
26(24)	R.T1		
27(25)	R.T2		
25(23)	R.T3		
7(1)	LCT1	Loudness dedicated terminals. A high-frequency-range correcting C should be put between CT1 and IN, and low-frequency-range correcting C between CT2 and L-V _{SS} (R-V _{SS}).	
6(48)	LCT2		
36(36)	RCT1		
37(37)	RCT2		

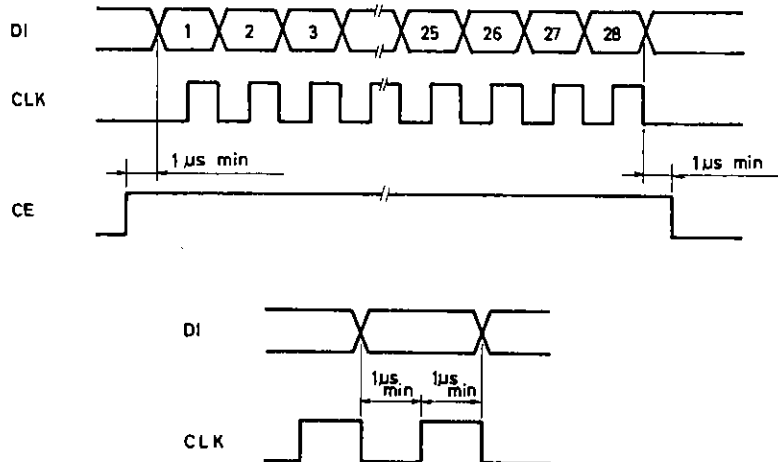
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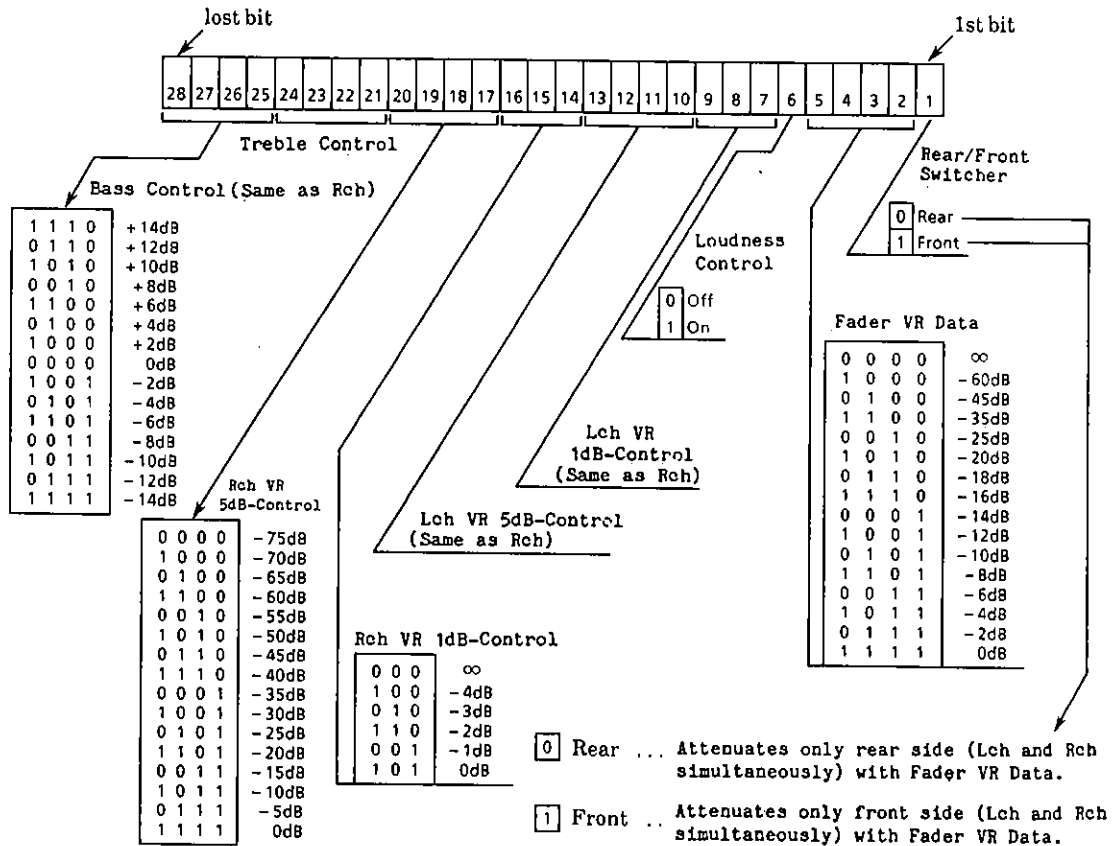
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Pin No.	Symbol	Description of Functions	Remarks
8(2)	L-V _{SS}	Main volume control block fader control common terminals. The impedance of pattern connected to these pins should be as low as possible. Since L-V _{SS} (R-V _{SS}) and V _{SS} have not been connected inside the LSI, they should be connected together on the outside in conformance with their individual specifications. Particular attenuation should be paid to the capacitance assigned to the capacitors put between L-V _{SS} (R-V _{SS}) and V _{SS} , which will emerge as a residual resistive component when control is turned down for maximum attenuation.	
35(35)	R-V _{SS}		
42(42)	INIT	intra-IC latch resetting terminal  Control-setting data at the internal latch will be indeterminate when power has just been switched on, so that by engaging the "L" level of this pin at power-on, the fader control may be set at its $-\infty$ position and muting behaviour is engaged (Note: V_{DD} to V_{EE} Level).	
22(20)	CE	Chip enable terminal. When this pin is made "H" to "L", data is written in the internal latch, activating the various analog switches. When the "H" level is then restored, transfer of the data will be enabled.	
20(16)	DI	Input terminals for serial data and clock that serve control purposes.	
21(17)	CLK		
1(43) 23(21) 19(15) 24(22)	V _{DD} V _{CC} V _{SS} V _{EE}	These pins are connected to the relevant power supplies. Exercise caution against V _{CC} rising earlier than V _{DD} .	
2(3, 7) 41(18, 30, 34, 41, 44)	NC	No connect pins. Absolutely nothing should be connected here.	
(19)	V _{DD} (NC)	V _{DD} subterminal. Connected to V _{DD} or left open.	LC7537AN and LC7537NE only

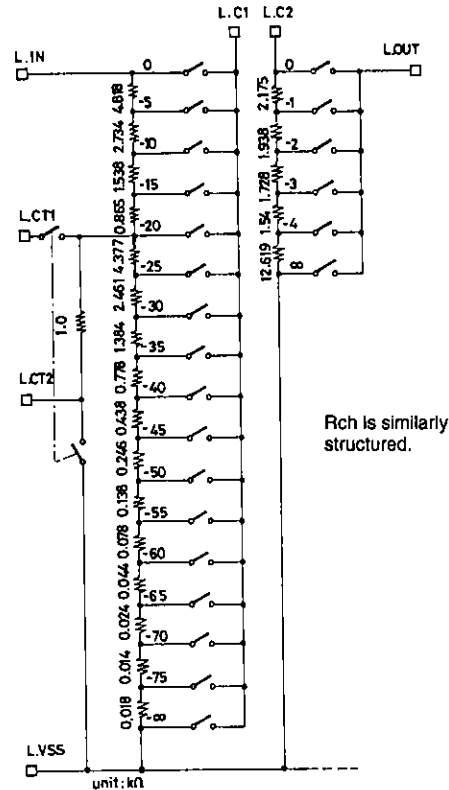
Control Timing



Data Format

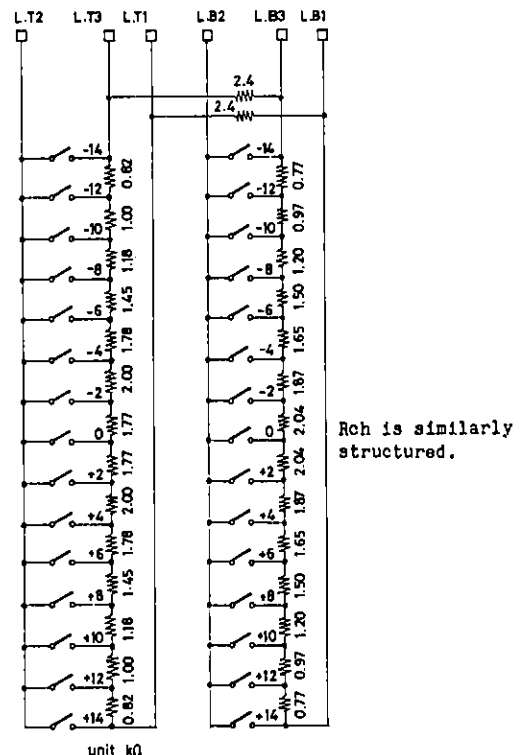
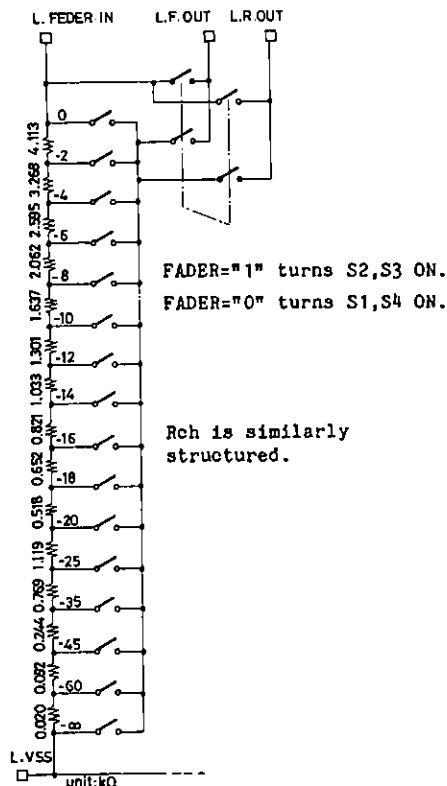


Main Volume Control Block Equivalent Circuit



Fader Volume Control Block Equivalent Circuit

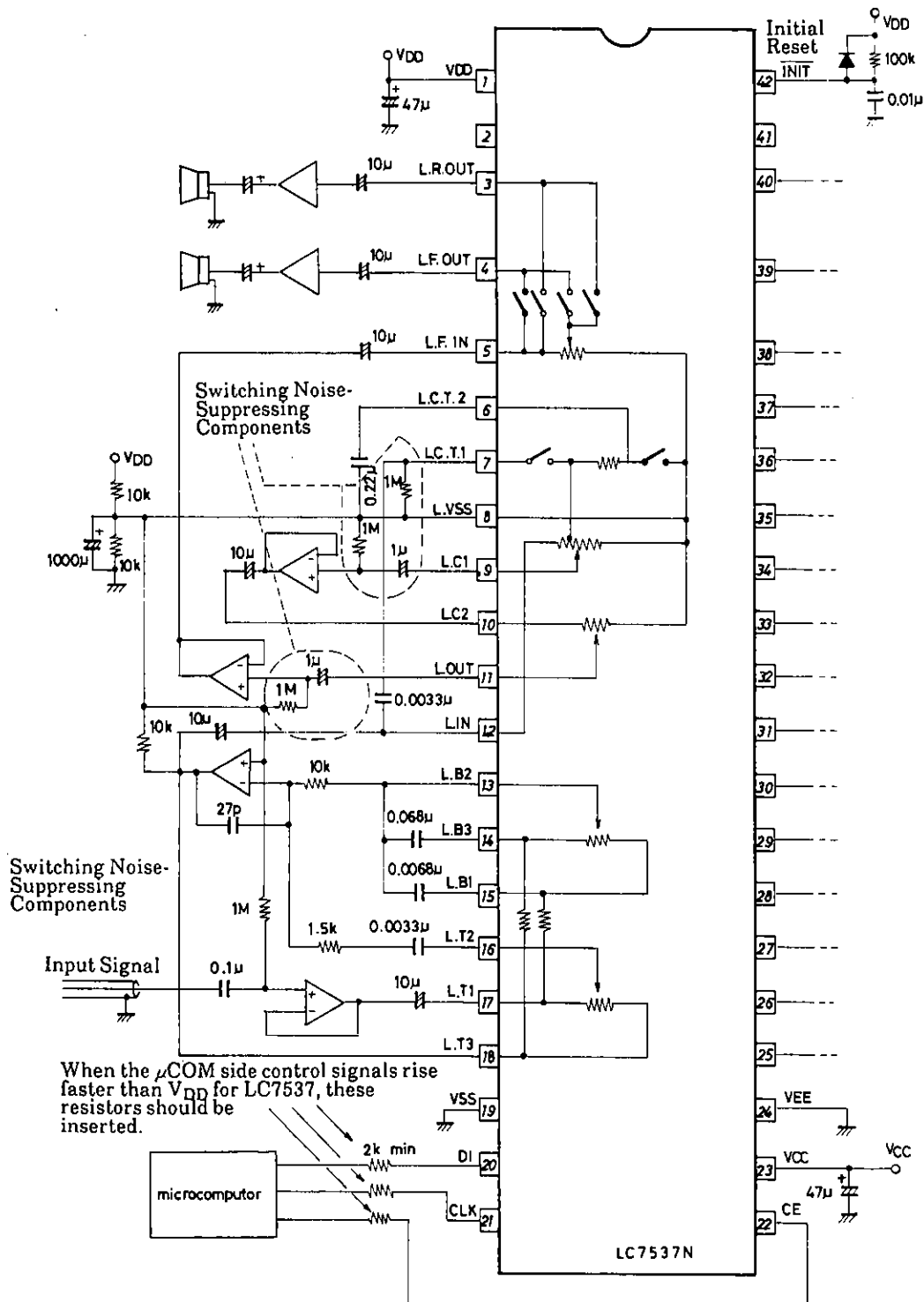
Tone Control Block Equivalent Circuit



When data of -001s is transferred to main volume control 1dB STEP, S1,S2 are brought to open state and S3,S4 are turned ON simultaneously.

Sample Application Circuits

Single Power Supply

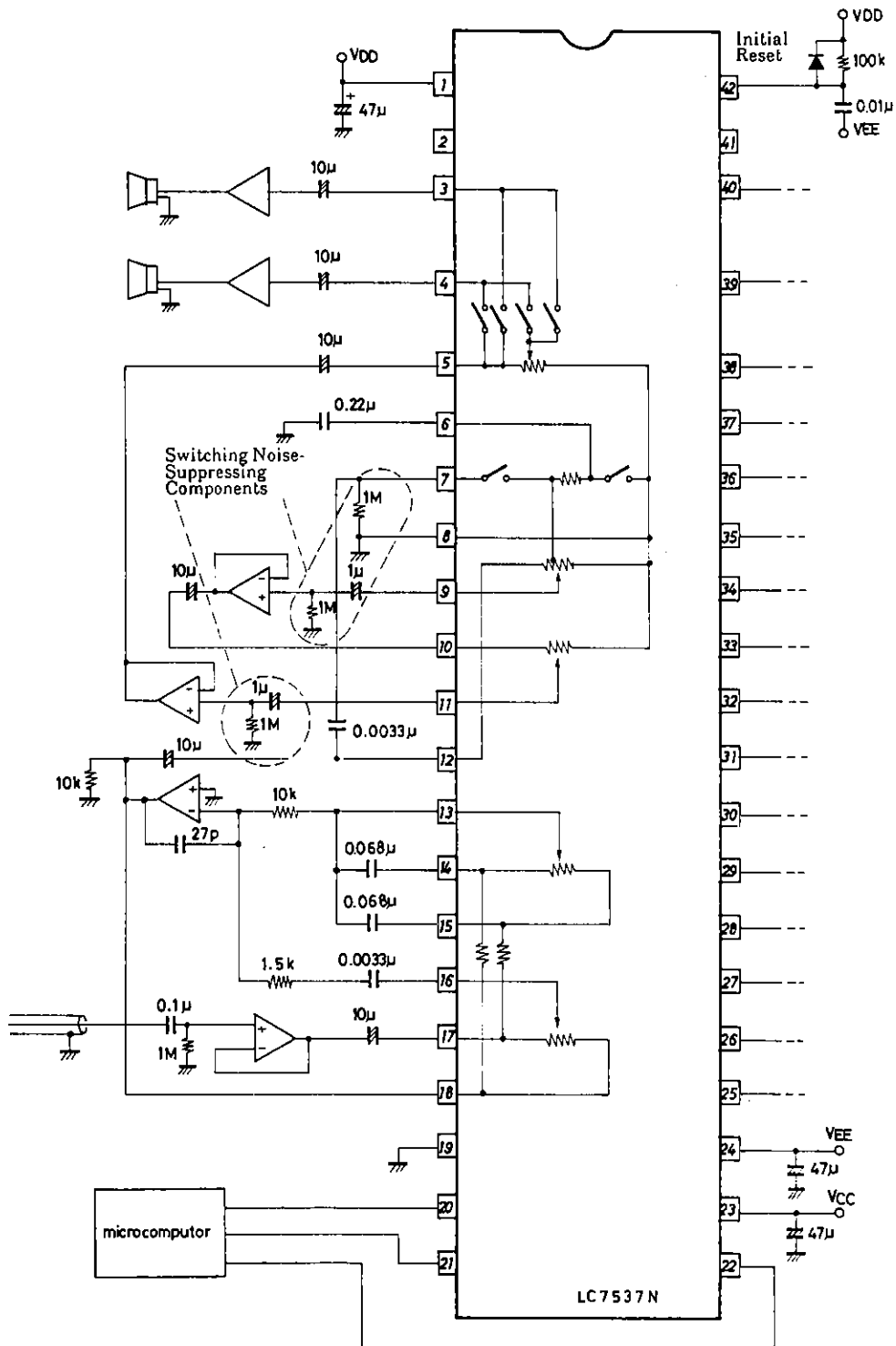


Unit (resistance: Ω , capacitance: F)

Note: Bipolar electrolytic capacitors should preferably be employed where no polarity has been indicated.

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Dual $\pm$ Power Supply

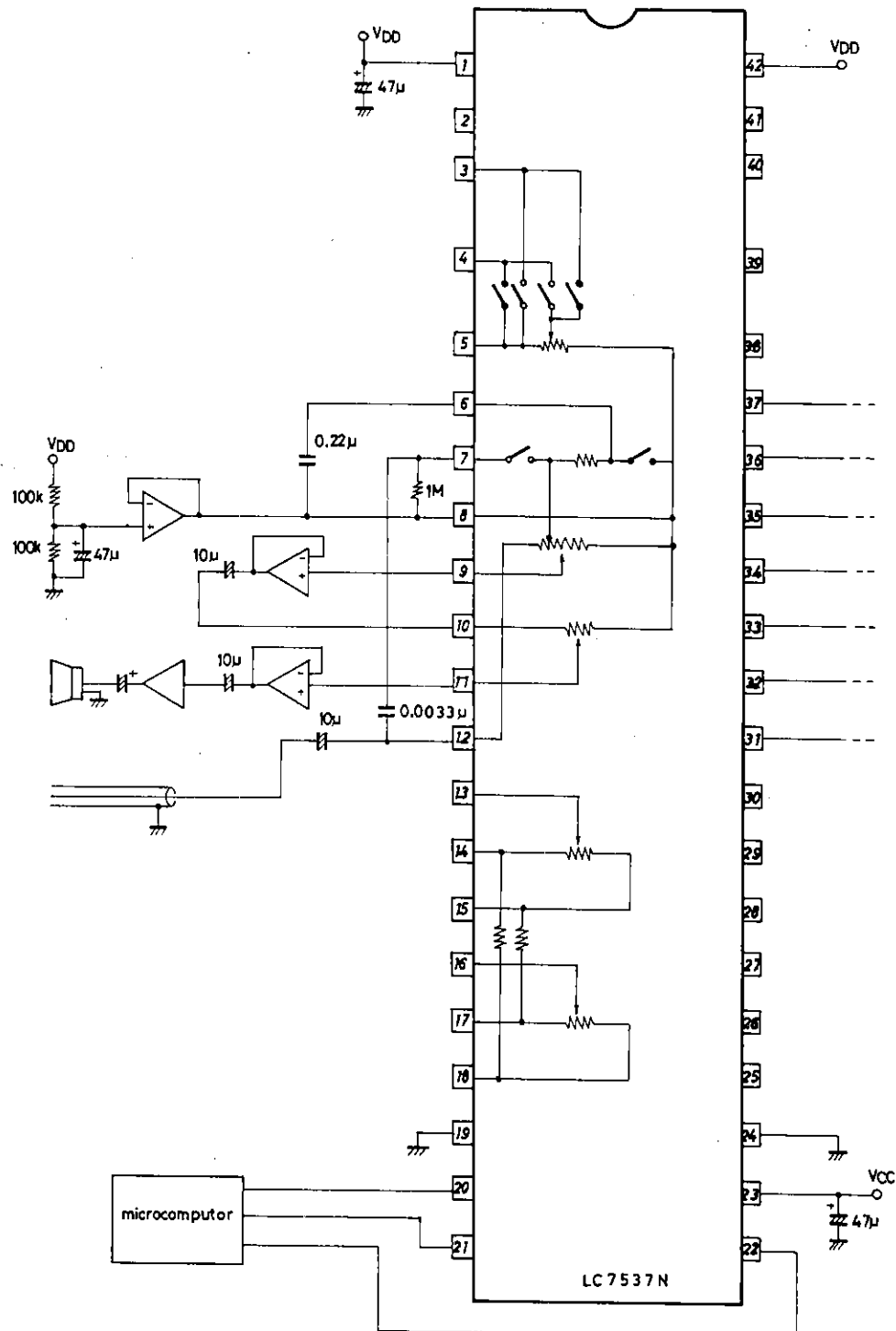


Unit (resistance: Ω , capacitance: F)

Note: Bipolar electrolytic capacitors should preferably be employed where no polarity has been indicated.

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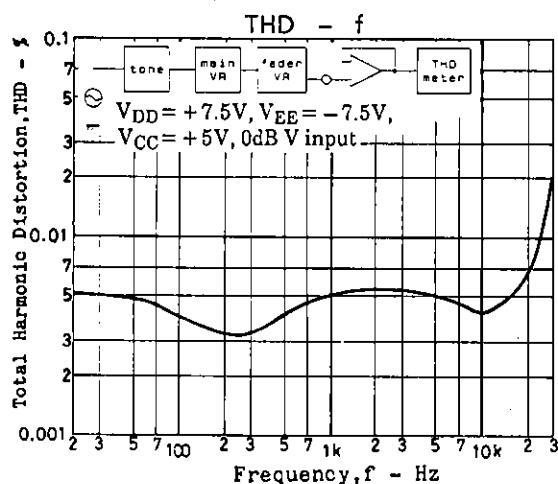
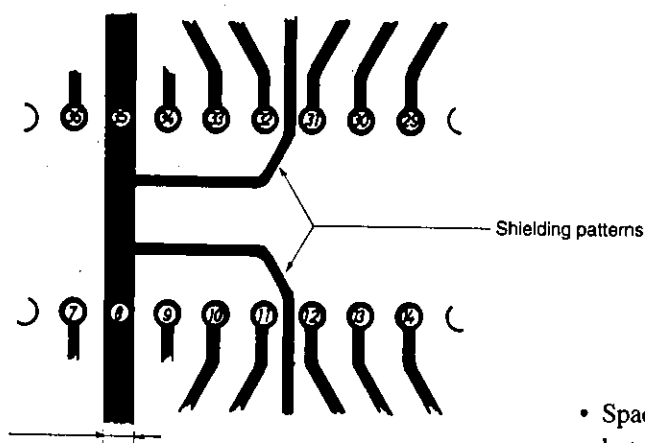
Single Power Supply



Unit (resistance: Ω, capacitance: F)

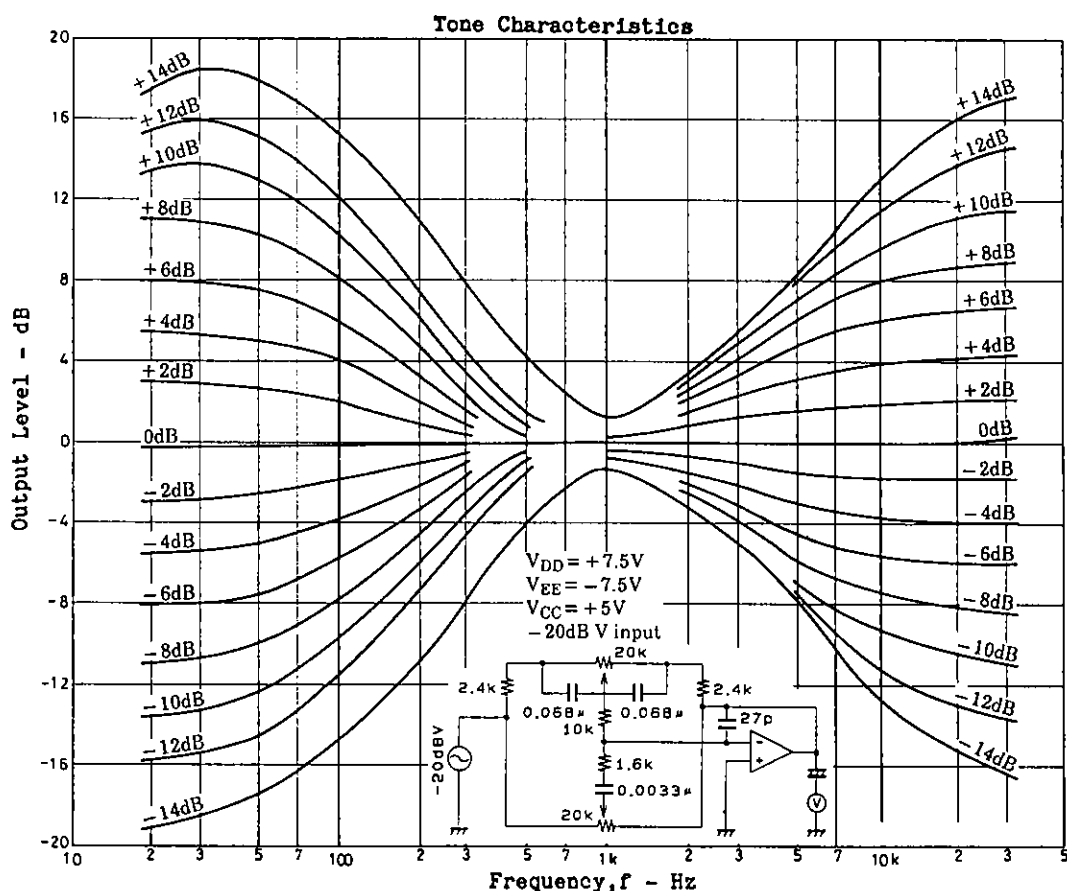
Note: Bipolar electrolytic capacitors should preferably be employed where no polarity has been indicated.

Caution for Pattern Designing

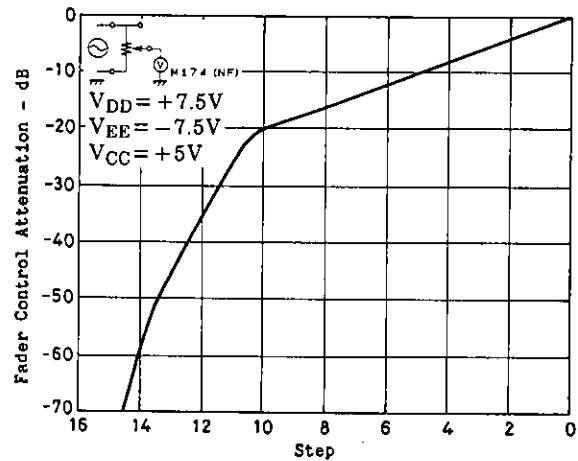
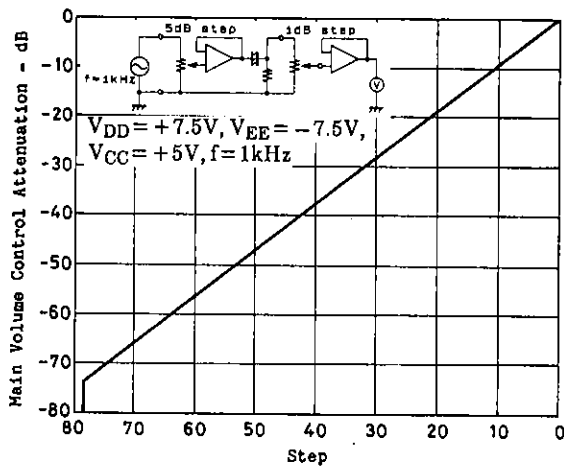


- Space the patterns between L.IN and L.OUT and those between R.IN and R.OUT as far apart as possible. When forced to design them close together, provide shielding patterns between as illustrated. They will be effective at the maximum attenuated level (with 10 kHz and higher frequencies). (DIP42S)

- Make the L-V_{SS} and R-V_{SS} as broad as possible.



Unit (resistance: Ω, capacitance: F)



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