National Semiconductor

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MM54C173/MM74C173 TRI-STATE® Quad D Flip-Flop

General Description

The MM54C173/MM74C173 TRI-STATE quad D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. The four D-type flip-flops operate synchronously from a common clock. The TRI-STATE output allows the device to be used in bus-organized systems.

The outputs are placed in the TRI-STATE mode when either of the two output disable pins are in the logic ''1'' level. The input disable allows the flip-flops to remain in their present states without disrupting the clock. If either of the two input disables are taken to a logic ''1'' level, the Q outputs are fed back to the inputs and in this manner the flip-flops do not change state.

Clearing is enabled by taking the input to a logic ''1'' level. Clocking occurs on the positive-going transition.

Features

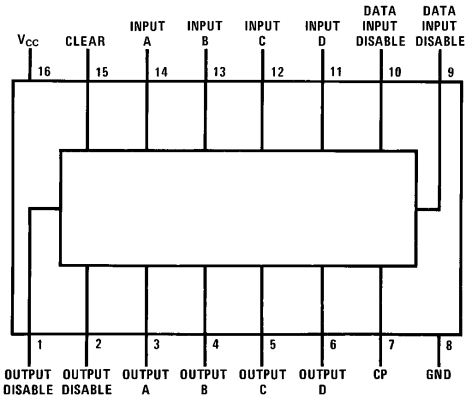
- Supply voltage range — 3V to 15V
- Tenth power TTL compatible — Drive 2 LPTTL loads
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power
- Medium speed operation
- High impedance TRI-STATE
- Input disable without gating the clock

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

Connection Diagram

Dual-In-Line Package



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Top View

Order Number MM54C173 or MM74C173

Truth Table

(Both Output Disables Low)

t_n		t_{n+1}
Data Input Disable	**Data Input**	**Output**
Logic ''1'' on One or Both Inputs	X	Q_n
Logic ''0'' on Both Inputs	1	1
Logic ''0'' on Both Inputs	0	0

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C173	−55°C to +125°C
MM74C173	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum V_{CC} Voltage	18V
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V V_{CC} = 10V	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V V_{CC} = 10V			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V V_{CC} = 10V	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V V_{CC} = 10V			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current		−1.0	0.005		μA
I_{OZ}	Output Current in High Impedance State	V_{CC} = 15V, V_O = 15V V_{CC} = 15V, V_O = 0V	 −1.0	0.001 0.001	1.0	μA μA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	mA
LOW POWER TTL/CMOS INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.5V	V_{CC}−1.5 V_{CC}−1.5			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, V_{CC} = 4.5V, I_O = −360 μA 74C, V_{CC} = 4.75V, I_O = −360 μA	2.4 2.4			V V
$V_{OUT(1)}$	Logical "0" Output Voltage	54C, V_{CC} = 4.5V, I_O = 360 μA 74C, V_{CC} = 4.75V, I_O = 360 μA			0.4 0.4	V V
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		500		ns
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current	V_{CC} = 5V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	−1.75			mA
I_{SOURCE}	Output Source Current	V_{CC} = 10V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	−8.0			mA
I_{SINK}	Output Sink Current	V_{CC} = 5V, $V_{IN(1)}$ = 5V T_A = 25°C, V_{OUT} = V_{CC}	1.75			mA
I_{SINK}	Output Sink Current	V_{CC} = 10V, $V_{IN(1)}$ = 10V T_A = 25°C, V_{OUT} = V_{CC}	8.0			mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Output	$V_{CC} = 5V$ $V_{CC} = 10V$		220 80	400 200	ns ns
t_S	Input Data Set-up Time	$V_{CC} = 5V$ $V_{CC} = 10V$		40 15	80 30	ns ns
t_H	Input Data Hold Time	$V_{CC} = 5V$ $V_{CC} = 10V$		0 0	0 0	ns ns
t_S	Input Disable Set-up Time, $t_{S\ DISS}$	$V_{CC} = 5V$ $V_{CC} = 10V$		100 35	200 70	ns ns
t_H	Input Disable Hold Time, $t_{H\ DISS}$	$V_{CC} = 5V$ $V_{CC} = 10V$		0 0	0 0	ns ns
t_{1H}, t_{0H}	Delay from Output Disable to High Impedance State (from Logical "1" or Logical "0" Level)	$V_{CC} = 5V$, $R_L = 10k$ $V_{CC} = 10V$, $R_L = 10k$		170 70	340 140	ns ns
t_{H1}	Delay from Output Disable to Logical "1" Level (from High Impedance State)	$V_{CC} = 5V$ $V_{CC} = 10V$		170 70	340 140	ns ns
t_{H0}	Delay from Output Disable to Logical "0" Level (from High Impedance State)	$V_{CC} = 5V$ $V_{CC} = 10V$		170 70	340 140	ns ns
t_{pd0}, t_{pd1}	Propagation Delay from Clear to Output	$V_{CC} = 5V$ $V_{CC} = 10V$		240 90	490 180	ns ns
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5V$ $V_{CC} = 10V$	3 7.0	4 12		MHz MHz
t_W	Minimum Clear Pulse Width	$V_{CC} = 5V$ $V_{CC} = 10V$		150 70		ns ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5V$ $V_{CC} = 10V$	10 5			μs μs
C_{IN}	Input Capacitance	(Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)				

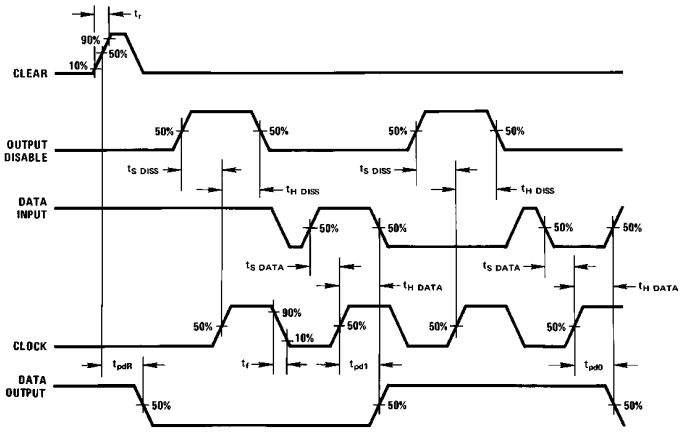
*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guarantee.d Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Switching Time Waveforms



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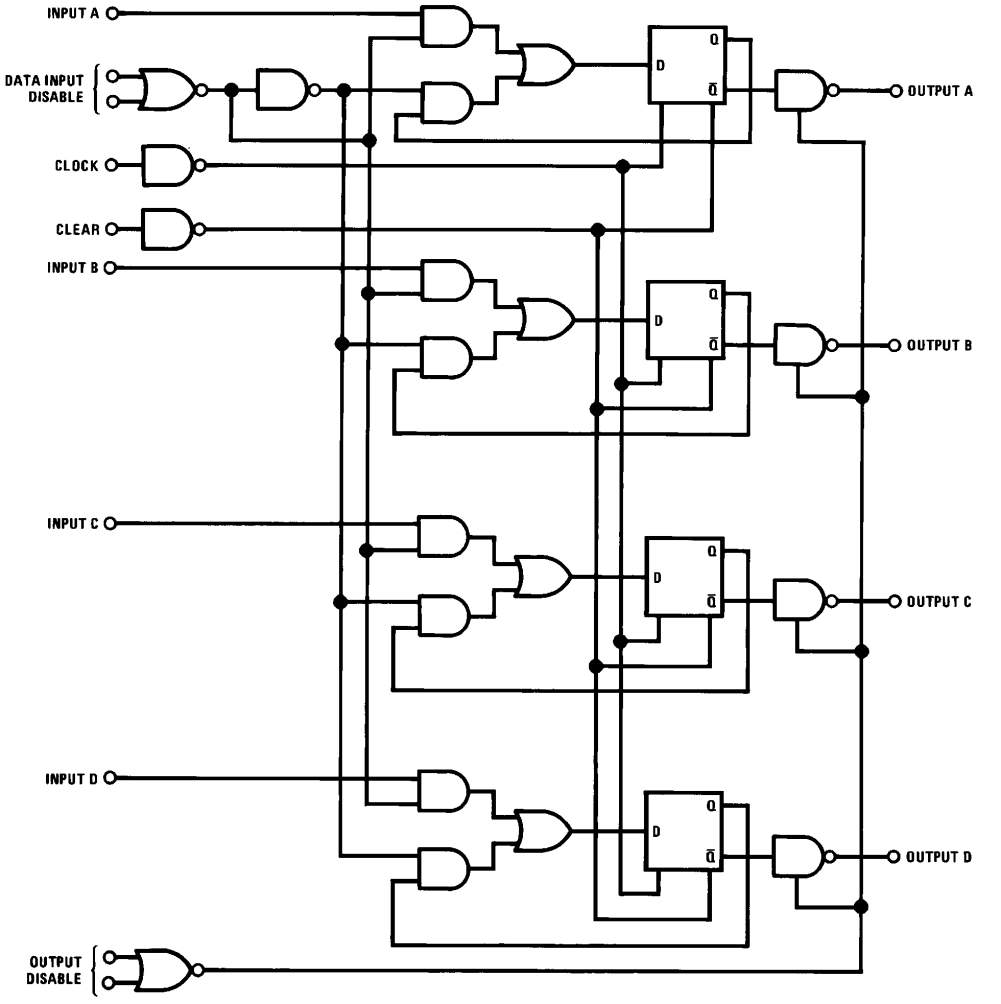
Logic Diagram



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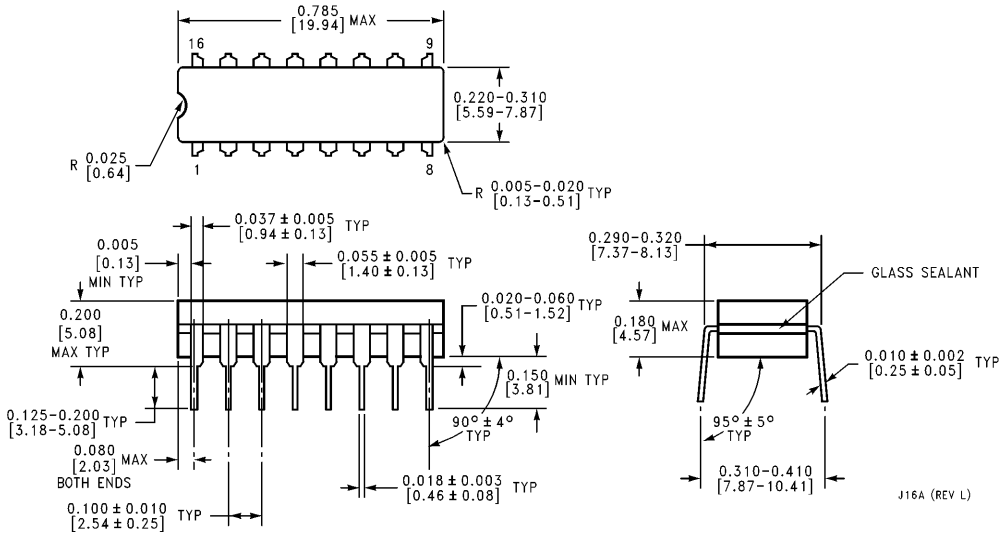
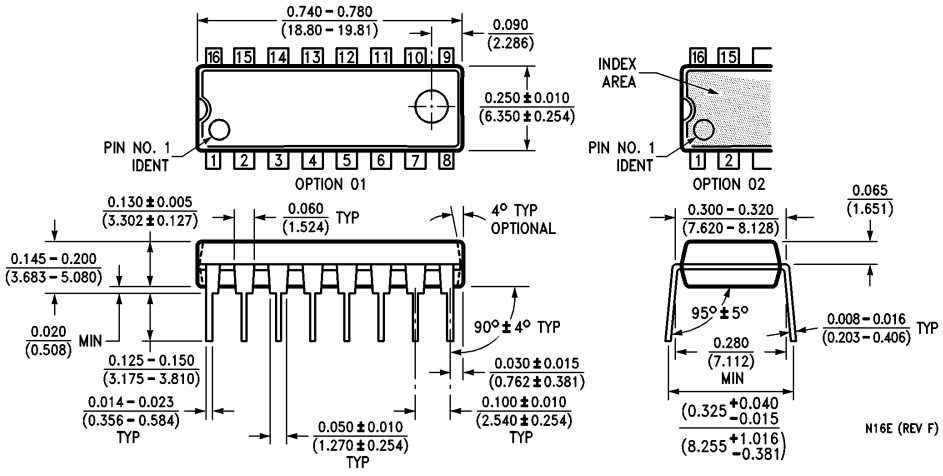
Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number MM54C173J or MM74C173J
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number MM54C173N or MM74C173N
NS Package Number N16E

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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