

## LMX2335U/LMX2336U

### PLLatinum™ Ultra Low Power Dual Frequency Synthesizer for RF Personal Communications

**LMX2335U      1.2 GHz/1.2 GHz**

**LMX2336U      2.0 GHz/1.2 GHz**

#### General Description

The LMX2335U and LMX2336U devices are high performance frequency synthesizers with integrated dual modulus prescalers. The LMX2335U and LMX2336U devices are designed for use in applications requiring two RF phase-locked loops.

A 64/65 or a 128/129 prescale ratio can be selected for each RF synthesizer. Using a proprietary digital phase locked loop technique, the LMX2335U and LMX2336U devices generate very stable, low noise control signals for the RF voltage controlled oscillators. Both RF synthesizers include a two-level programmable charge pump. The RF1 synthesizer has dedicated Fastlock circuitry.

Serial data is transferred to the devices via a three wire interface (Data, LE, Clock). Supply voltages from 2.7V to 5.5V are supported. The LMX2335U and the LMX2336U feature very low current consumption:

LMX2335U (1.2 GHz)– 3.0 mA, LMX2336U (2.0 GHz)– 3.5 mA at 3.0V.

The LMX2335U device is available in 16-pin TSSOP, and 16-pin Chip Scale Package (CSP) surface mount plastic packages. The LMX2336U device is available in 20-Pin TSSOP, 24-Pin CSP, and 20-Pin UTCSP surface mount plastic packages.

#### Features

- Ultra Low Current Consumption
- Upgrade and Compatible to the LMX2335L and LMX2336L devices
- 2.7V to 5.5V operation
- Selectable Synchronous or Asynchronous Powerdown Mode:  
I<sub>CC-PWDN</sub> = 1 µA typical at 3.0V
- Selectable Dual Modulus Prescaler  
RF1: 64/65 or 128/129  
RF2: 64/65 or 128/129
- Selectable Charge Pump TRI-STATE® Mode
- Programmable Charge Pump Current Levels  
RF1 and RF2: 0.95 or 3.8 mA
- Selectable Fastlock™ Mode for the RF1 Synthesizer
- Push-Pull Analog Lock Detect Mode
- LMX2335U is available in 16-Pin TSSOP and 16-Pin CSP
- LMX2336U is available in 20-Pin TSSOP, 24-Pin CSP, and 20-Pin UTCSP

#### Applications

- Mobile Handsets  
(GSM, GPRS, W-CDMA, CDMA, PCS, AMPS, PDC, DCS)
- Cordless Handsets (DECT, DCT)
- Wireless Data
- Cable TV Tuners

Thin Shrink Small Outline Package (MTC16)



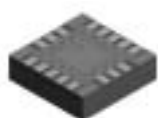
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Thin Shrink Small Outline Package (MTC20)



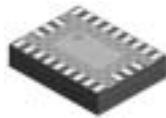
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Chip Scale Package (SLB16A)



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Chip Scale Package (SLB24A)



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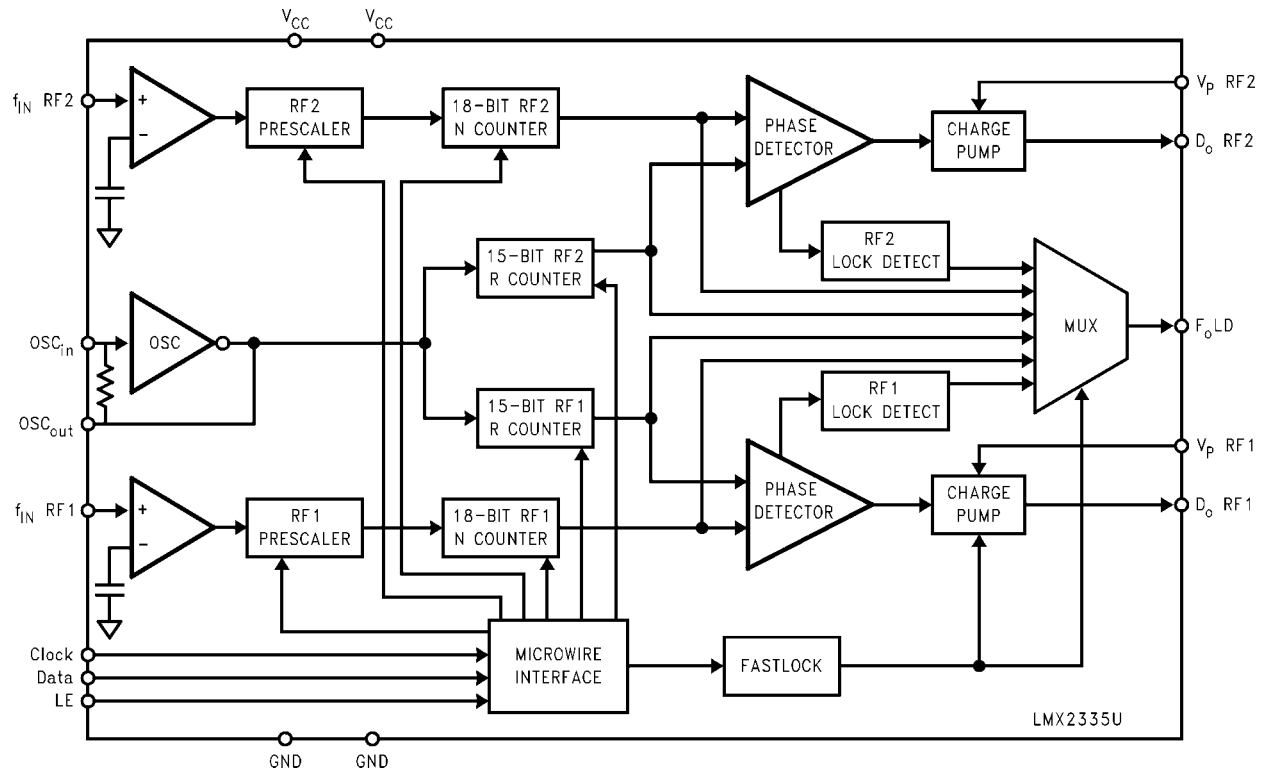
Ultra Thin Chip Scale Package (SLE20A)



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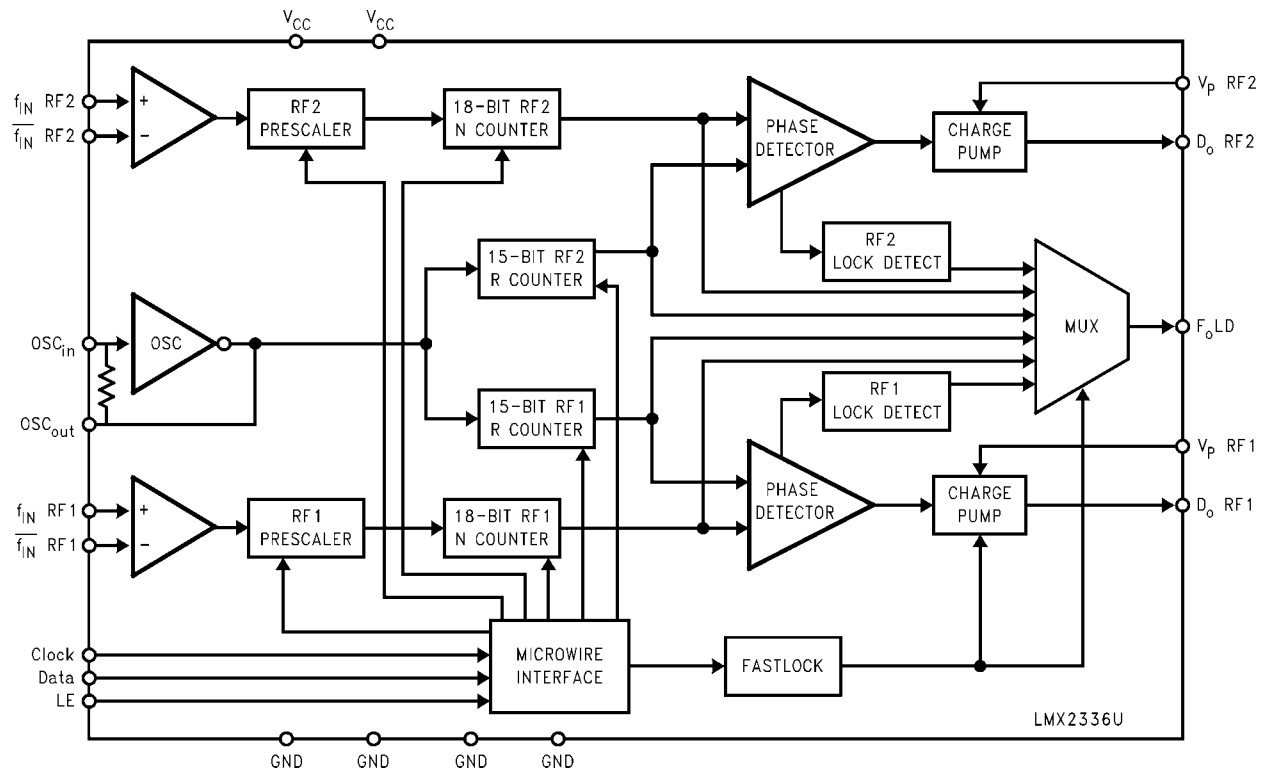
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## LMX2335U Functional Block Diagram



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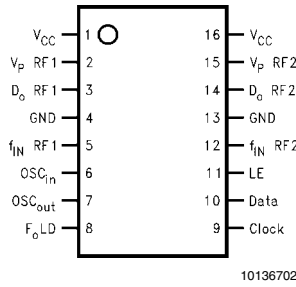
## LMX2336U Functional Block Diagram



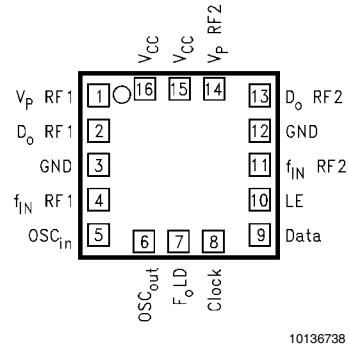
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## Connection Diagrams

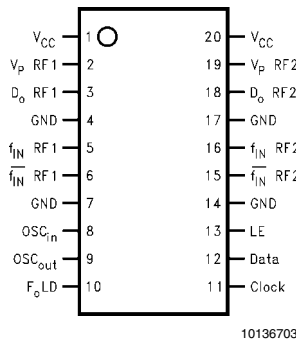
**LMX2335U Thin Shrink Small Outline Package (TM)  
(Top View)**



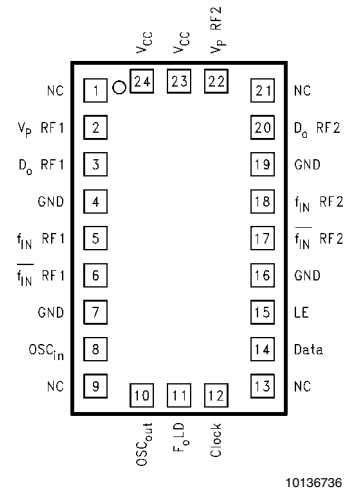
**LMX2335U Chip Scale Package (SLB)  
(Top View)**



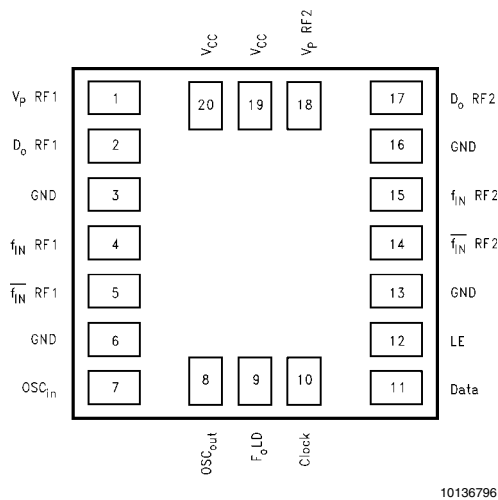
**LMX2336U Thin Shrink Small Outline Package (TM)  
(Top View)**



**LMX2336U Chip Scale Package (SLB)  
(Top View)**



**LMX2336U Ultra Thin Chip Scale Package (SLE)  
(Top View)**



## Pin Descriptions

Pin Name	Pin No. LMX2336U 20-Pin UTCSP	Pin No. LMX2336U 20-Pin TSSOP	Pin No. LMX2336U 24-Pin CSP	Pin No. LMX2335U 16-Pin TSSOP	Pin No. LMX2335U 16-Pin CSP	I/O	Description
$V_{CC}$	20	1	24	1	16	–	Power supply bias for the RF1 PLL analog and digital circuits. $V_{CC}$ may range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
$V_P$ RF1	1	2	2	2	1	–	RF1 PLL charge pump power supply. Must be $\geq V_{CC}$ .
$D_o$ RF1	2	3	3	3	2	O	RF1 PLL charge pump output. The output is connected to the external loop filter, which drives the input of the VCO.
GND	3	4	4	4	3	–	LMX2335U: Ground for the RF1 PLL analog and digital circuits. LMX2336U: Ground for the RF1 PLL digital circuitry.
$f_{IN}$ RF1	4	5	5	5	4	I	RF1 PLL prescaler input. Small signal input from the VCO.
$\overline{f_{IN}}$ RF1	5	6	6	X	X	I	LMX2335U: Don't care. LMX2336U: RF1 PLL prescaler complementary input. For single ended operation, this pin should be AC grounded. The LMX2336U RF1 PLL can be driven differentially when the bypass capacitor is omitted.
GND	6	7	7	X	X	–	LMX2335U: Don't care. LMX2336U: Ground for the RF1 PLL analog circuitry.
OSC <sub>in</sub>	7	8	8	6	5	I	Oscillator input. It has an approximate $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate.
OSC <sub>out</sub>	8	9	10	7	6	O	Oscillator output. This output is connected directly to a crystal. If a TCXO is used, it is left open.
$F_{oLD}$	9	10	11	8	7	O	Programmable multiplexed output pin. Functions as a general purpose CMOS TRI-STATE output, RF1/RF2 PLL push-pull analog lock detect output, N and R divider output, or Fastlock output, which connects a parallel resistor to the external loop filter.
Clock	10	11	12	9	8	I	MICROWIRE Clock input. High impedance CMOS input. Data is clocked into the 22-bit shift register on the rising edge of Clock.
Data	11	12	14	10	9	I	MICROWIRE Data input. High impedance CMOS input. Binary serial data. The MSB of Data is entered first. The last two bits are the control bits.
LE	12	13	15	11	10	I	MICROWIRE Latch Enable input. High impedance CMOS input. When LE transitions HIGH, Data stored in the shift registers is loaded into one of 4 internal control registers.

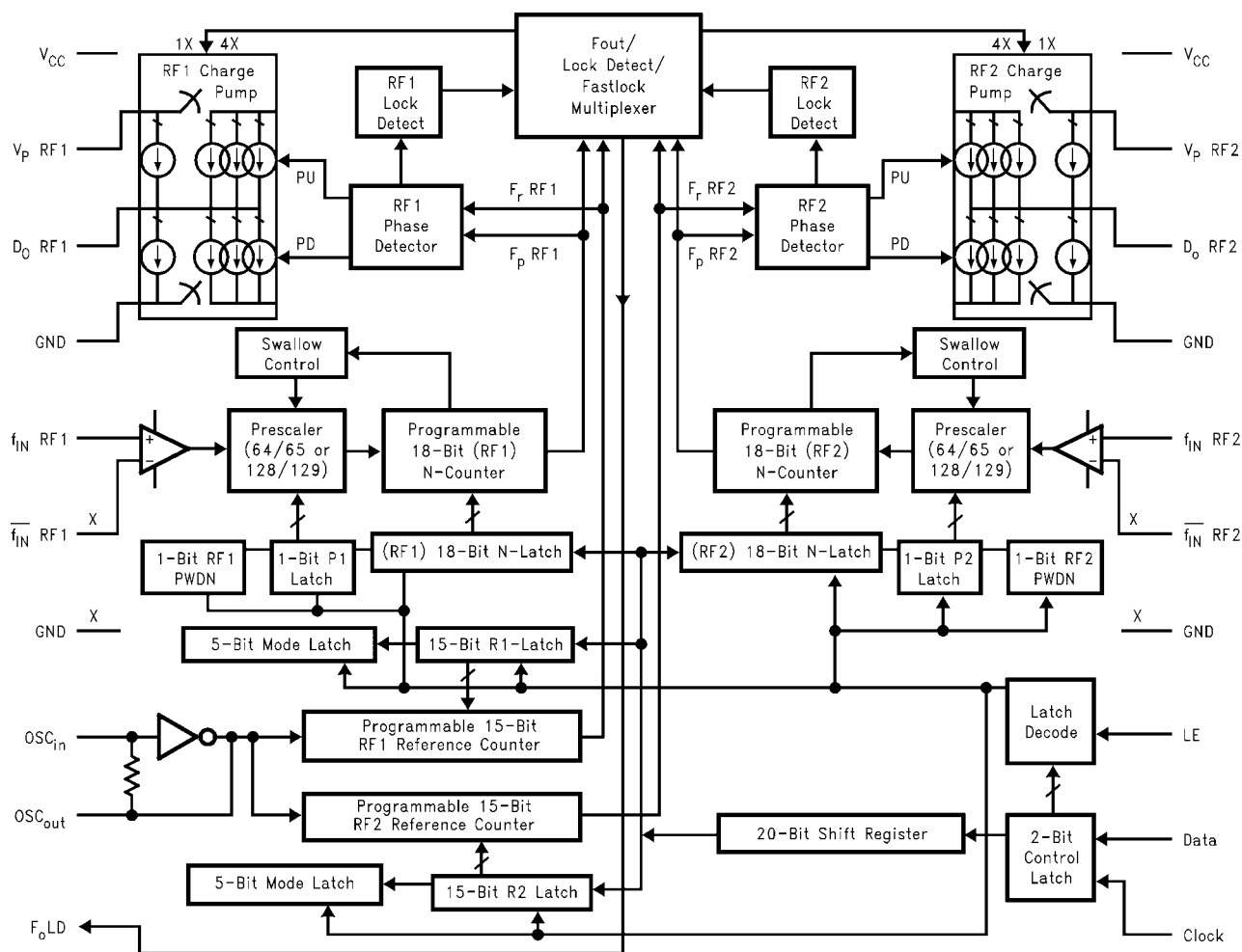
## Pin Descriptions (Continued)

Pin Name	Pin No. LMX2336U 20-Pin UTCSP	Pin No. LMX2336U 20-Pin TSSOP	Pin No. LMX2336U 24-Pin CSP	Pin No. LMX2335U 16-Pin TSSOP	Pin No. LMX2335U 16-Pin CSP	I/O	Description
GND	13	14	16	X	X	–	LMX2335U: Don't care. LMX2336U: Ground for the RF2 PLL analog circuitry.
$\overline{f_{IN}}$ RF2	14	15	17	X	X	I	LMX2335U: Don't care. LMX2336U: RF2 PLL prescaler complementary input. For single ended operation, this pin should be AC grounded. The LMX2336U RF2 PLL can be driven differentially when the bypass capacitor is omitted.
$f_{IN}$ RF2	15	16	18	12	11	I	RF2 PLL prescaler input. Small signal input from the VCO.
GND	16	17	19	13	12	–	LMX2335U: Ground for the RF2 PLL analog and digital circuits, MICROWIRE, $F_{oLD}$ and oscillator circuits. LMX2336U: Ground for the RF2 PLL digital circuitry, MICROWIRE, $F_{oLD}$ and oscillator circuits.
$D_o$ RF2	17	18	20	14	13	O	RF2 PLL charge pump output. The output is connected to the external loop filter, which drives the input of the VCO.
$V_P$ RF2	18	19	22	15	14	–	RF2 PLL charge pump power supply. Must be $\geq V_{CC}$ .
$V_{CC}$	19	20	23	16	15	–	Power supply bias for the RF2 PLL analog and digital circuits, MICROWIRE, $F_{oLD}$ and oscillator circuits. $V_{CC}$ may range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
NC	X	X	1, 9, 13, 21	X	X	–	LMX2335U: Don't Care. LMX2336U: No connect.

## Ordering Information

Model	Temperature Range	Package Description	Packing	NS Package Number
LMX2335USLBX	–40°C to +85°C	Chip Scale Package (CSP) Tape and Reel	2500 Units Per Reel	SLB16A
LMX2335UTM	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	96 Units Per Rail	MTC16
LMX2335UTMX	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP) Tape and Reel	2500 Units Per Reel	MTC16
LMX2336USLEX	–40°C to +85°C	Ultra Thin Chip Scale Package (UTCSP) Tape and Reel	2500 Units Per Reel	SLE20A
LMX2336USLBX	–40°C to +85°C	Chip Scale Package (CSP) Tape and Reel	2500 Units Per Reel	SLB24A
LMX2336UTM	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	73 Units Per Rail	MTC20
LMX2336UTMX	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP) Tape and Reel	2500 Units Per Reel	MTC20

# Detailed Block Diagram



## Notes:

1.  $V_{CC}$  supplies power to the RF1 and RF2 prescalers, RF1 and RF2 feedback dividers, RF1 and RF2 reference dividers, RF1 and RF2 phase detectors, the  $OSC_{in}$  buffer, MICROWIRE, and  $F_0LD$  circuits.
2.  $V_P$  RF1 and  $V_P$  RF2 supply power to the charge pumps. They can be run separately as long as  $V_P$  RF1  $\geq V_{CC}$  and  $V_P$  RF2  $\geq V_{CC}$ .
3. X signifies a pin that is NOT available on the LMX2335U PLL.

**Absolute Maximum Ratings** (Notes 1,

2, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

**Power Supply Voltage**

$V_{CC}$ to GND	–0.3V to +6.5V
$V_P$ RF1 to GND	–0.3V to +6.5V
$V_P$ RF2 to GND	–0.3V to +6.5V

**Voltage on any pin to GND ( $V_I$ )**

$V_I$ must be < +6.5V	–0.3V to $V_{CC}+0.3V$
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**Storage Temperature Range ( $T_S$ )** –65°C to +150°C**Lead Temperature (solder 4 s) ( $T_L$ )** +260°C**16-Pin TSSOP  $\theta_{JA}$  Thermal Impedance** 137.1°C/W**20-Pin TSSOP  $\theta_{JA}$  Thermal Impedance** 114.5°C/W16-Pin CSP  $\theta_{JA}$  Thermal Impedance 130°C/W24-Pin CSP  $\theta_{JA}$  Thermal Impedance 112°C/W**Recommended Operating Conditions** (Note 1)**Power Supply Voltage**

$V_{CC}$ to GND	+2.7V to +5.5V
$V_P$ RF1 to GND	$V_{CC}$ to +5.5V
$V_P$ RF2 to GND	$V_{CC}$ to +5.5V

**Operating Temperature ( $T_A$ )** –40°C to +85°C

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

**Note 2:** This device is a high performance RF integrated circuit with an ESD rating <2 kV and is ESD sensitive. Handling and assembly of this device should only be done at ESD protected work stations.

**Note 3:** GND = 0V

**Electrical Characteristics**

$V_{CC} = V_P$  RF1 =  $V_P$  RF2 = 3.0V, –40°C ≤  $T_A$  ≤ +85°C, unless otherwise specified

Symbol	Parameter	Conditions	Value			Units	
			Min	Typ	Max		
I <sub>CC</sub> PARAMETERS							
I <sub>CCRF1 + RF2</sub>	Power Supply Current, RF1 + RF2 Synthesizers	LMX2335U	Clock, Data and LE = GND OSC <sub>in</sub> = GND		3.0	4.0	mA
		LMX2336U	PWDN RF1 Bit = 0 PWDN RF2 Bit = 0		3.5	4.5	mA
I <sub>CCRF1</sub>	Power Supply Current, RF1 Synthesizer Only	LMX2335U	Clock, Data and LE = GND OSC <sub>in</sub> = GND		1.5	2.0	mA
		LMX2336U	PWDN RF1 Bit = 0 PWDN RF2 Bit = 1		2.0	2.5	mA
I <sub>CCRF2</sub>	Power Supply Current, RF2 Synthesizer Only	LMX2335U	Clock, Data and LE = GND OSC <sub>in</sub> = GND		1.5	2.0	mA
		LMX2336U	PWDN RF1 Bit = 1 PWDN RF2 Bit = 0		1.5	2.0	
I <sub>CC-PWDN</sub>	Powerdown Current	LMX2335U/	Clock, Data and LE = GND OSC <sub>in</sub> = GND		1.0	10.0	μA
		LMX2336U	PWDN RF1 Bit = 1 PWDN RF2 Bit = 1				
RF1 SYNTHESIZER PARAMETERS							
f <sub>IN</sub> RF1	RF1 Operating Frequency	LMX2335U		100		1200	MHz
		LMX2336U		200		2000	MHz
N <sub>RF1</sub>	RF1 N Divider Range	Prescaler = 64/65 (Note 4)		192		131135	
		Prescaler = 128/129 (Note 4)		384		262143	
R <sub>RF1</sub>	RF1 R Divider Range			3		32767	
F <sub>φRF1</sub>	RF1 Phase Detector Frequency					10	MHz
P <sub>f<sub>IN</sub></sub> RF1	RF1 Input Sensitivity	2.7V ≤ V <sub>CC</sub> ≤ 3.0V (Note 5)		−15		0	dBm
		3.0V < V <sub>CC</sub> ≤ 5.5V (Note 5)		−10		0	dBm



# Electrical Characteristics (Continued)

$V_{CC} = V_P$  RF1 =  $V_P$  RF2 = 3.0V,  $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ , unless otherwise specified

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
RF1 SYNTHESIZER PARAMETERS						
ID <sub>o</sub> RF1 SOURCE	RF1 Charge Pump Output Source Current	VD <sub>o</sub> RF1 = V <sub>P</sub> RF1/2 ID <sub>o</sub> RF1 Bit = 0 (Note 6)		-0.95		mA
		VD <sub>o</sub> RF1 = V <sub>P</sub> RF1/2 ID <sub>o</sub> RF1 Bit = 1 (Note 6)		-3.80		mA
ID <sub>o</sub> RF1 SINK	RF1 Charge Pump Output Sink Current	VD <sub>o</sub> RF1 = V <sub>P</sub> RF1/2 ID <sub>o</sub> RF1 Bit = 0 (Note 6)		0.95		mA
		VD <sub>o</sub> RF1 = V <sub>P</sub> RF1/2 ID <sub>o</sub> RF1 Bit = 1 (Note 6)		3.80		mA
ID <sub>o</sub> RF1 TRI-STATE	RF1 Charge Pump Output TRI-STATE Current	0.5V ≤ VD <sub>o</sub> RF1 ≤ V <sub>P</sub> RF1 - 0.5V (Note 6)	-2.5		2.5	nA
ID <sub>o</sub> RF1 SINK Vs ID <sub>o</sub> RF1 SOURCE	RF1 Charge Pump Output Sink Current Vs Charge Pump Output Source Current Mismatch	VD <sub>o</sub> RF1 = V <sub>P</sub> RF1/2 T <sub>A</sub> = +25°C (Note 7)		3	10	%
ID <sub>o</sub> RF1 Vs VD <sub>o</sub> RF1	RF1 Charge Pump Output Current Magnitude Variation Vs Charge Pump Output Voltage	0.5V ≤ VD <sub>o</sub> RF1 ≤ V <sub>P</sub> RF1 - 0.5V T <sub>A</sub> = +25°C (Note 7)		10	15	%
ID <sub>o</sub> RF1 Vs T <sub>A</sub>	RF1 Charge Pump Output Current Magnitude Variation Vs Temperature	VD <sub>o</sub> RF1 = V <sub>P</sub> RF1/2 (Note 7)		10		%
RF2 SYNTHESIZER PARAMETERS						
f <sub>IN</sub> RF2	RF2 Operating Frequency	LMX2335U		100		1200 MHz
		LMX2336U		100		1200 MHz
N <sub>RF2</sub>	RF2 N Divider Range	Prescaler = 64/65 (Note 4)	192		131135	
		Prescaler = 128/129 (Note 4)	384		262143	
R <sub>RF2</sub>	RF2 R Divider Range		3		32767	
F <sub>φRF2</sub>	RF2 Phase Detector Frequency				10	MHz
Pf <sub>IN</sub> RF2	RF2 Input Sensitivity	2.7V ≤ V <sub>CC</sub> ≤ 3.0V (Note 5)	-15		0	dBm
		3.0V < V <sub>CC</sub> ≤ 5.5V (Note 5)	-10		0	dBm

**Electrical Characteristics** (Continued) $V_{CC} = V_P$  RF1 =  $V_P$  RF2 = 3.0V,  $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ , unless otherwise specified

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
RF2 SYNTHESIZER PARAMETERS						
ID <sub>O</sub> RF2 SOURCE	RF2 Charge Pump Output Source Current	VD <sub>O</sub> RF2 = V <sub>P</sub> RF2/2 ID <sub>O</sub> RF2 Bit = 0 (Note 6)		-0.95		mA
		VD <sub>O</sub> RF2 = V <sub>P</sub> RF2/2 ID <sub>O</sub> RF2 Bit = 1 (Note 6)		-3.80		mA
ID <sub>O</sub> RF2 SINK	RF2 Charge Pump Output Sink Current	VD <sub>O</sub> RF2 = V <sub>P</sub> RF2/2 ID <sub>O</sub> RF2 Bit = 0 (Note 6)		0.95		mA
		VD <sub>O</sub> RF2= V <sub>P</sub> RF2/2 ID <sub>O</sub> RF2 Bit = 1 (Note 6)		3.80		mA
ID <sub>O</sub> RF2 TRI-STATE	RF2 Charge Pump Output TRI-STATE Current	0.5V ≤ VD <sub>O</sub> RF2 ≤ V <sub>P</sub> RF2 - 0.5V (Note 6)	-2.5		2.5	nA
ID <sub>O</sub> RF2 SINK Vs ID <sub>O</sub> RF2 SOURCE	RF2 Charge Pump Output Sink Current Vs Charge Pump Output Source Current Mismatch	VD <sub>O</sub> RF2 = V <sub>P</sub> RF2/2 T <sub>A</sub> = +25°C (Note 7)		3	10	%
ID <sub>O</sub> RF2 Vs VD <sub>O</sub> RF2	RF2 Charge Pump Output Current Magnitude Variation Vs Charge Pump Output Voltage	0.5V ≤ VD <sub>O</sub> RF2 ≤ V <sub>P</sub> RF2 - 0.5V T <sub>A</sub> = +25°C (Note 7)		10	15	%
ID <sub>O</sub> RF2 Vs T <sub>A</sub>	RF2 Charge Pump Output Current Magnitude Variation Vs Temperature	VD <sub>O</sub> RF2 = V <sub>P</sub> RF2/2 (Note 7)		10		%
OSCILLATOR PARAMETERS						
F <sub>OSC</sub>	Oscillator Operating Frequency		2		40	MHz
V <sub>OSC</sub>	Oscillator Sensitivity	(Note 8)	0.5		V <sub>CC</sub>	V <sub>PP</sub>
I <sub>OSC</sub>	Oscillator Input Current	V <sub>OSC</sub> = V <sub>CC</sub> = 5.5V			100	μA
		V <sub>OSC</sub> = 0V, V <sub>CC</sub> = 5.5V	-100			μA
DIGITAL INTERFACE (Data, LE, Clock, F <sub>o</sub> LD)						
V <sub>IH</sub>	High-Level Input Voltage		0.8 V <sub>CC</sub>			V
V <sub>IL</sub>	Low-Level Input Voltage				0.2 V <sub>CC</sub>	V
I <sub>IH</sub>	High-Level Input Current	V <sub>IH</sub> = V <sub>CC</sub> = 5.5V	-1.0		1.0	μA
I <sub>IL</sub>	Low-Level Input Current	V <sub>IL</sub> = 0V, V <sub>CC</sub> = 5.5V	-1.0		1.0	μA
V <sub>OH</sub>	High-Level Output Voltage	I <sub>OH</sub> = -500 μA	V <sub>CC</sub> - 0.4			V
V <sub>OL</sub>	Low-Level Output Voltage	I <sub>OL</sub> = 500 μA			0.4	V
MICROWIRE INTERFACE						
t <sub>CS</sub>	Data to Clock Set Up Time	(Note 9)	50			ns
t <sub>CH</sub>	Data to Clock Hold Time	(Note 9)	10			ns
t <sub>CWH</sub>	Clock Pulse Width HIGH	(Note 9)	50			ns
t <sub>CWL</sub>	Clock Pulse Width LOW	(Note 9)	50			ns
t <sub>ES</sub>	Clock to Load Enable Set Up Time	(Note 9)	50			ns
t <sub>EW</sub>	Latch Enable Pulse Width	(Note 9)	50			ns

**Electrical Characteristics** (Continued) $V_{CC} = V_P$  RF1 =  $V_P$  RF2 = 3.0V,  $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ , unless otherwise specified

Symbol	Parameter		Conditions	Value			Units
				Min	Typ	Max	
PHASE NOISE CHARACTERISTICS							
L <sub>N</sub> (f) RF1	RF1 Synthesizer Normalized Phase Noise Contribution (Note 10)		TCXO Reference Source ID <sub>o</sub> RF1 Bit = 1		-212.0		dBc/Hz
L(f) RF1	RF1 Synthesizer Single Side Band Phase Noise Measured	LMX2335U	f <sub>IN</sub> RF1 = 900 MHz f = 1 kHz Offset F <sub>φRF1</sub> = 200 kHz Loop Bandwidth = 12 kHz N = 4500 F <sub>OSC</sub> = 10 MHz V <sub>OSC</sub> = 0.632 V <sub>PP</sub> ID <sub>o</sub> RF1 Bit = 1 PWDN RF2 Bit = 1 T <sub>A</sub> = +25°C (Note 11)		-85.94		dBc/Hz
		LMX2336U	f <sub>IN</sub> RF1 = 1960 MHz f = 1 kHz Offset F <sub>φRF1</sub> = 200 kHz Loop Bandwidth = 15 kHz N = 9800 F <sub>OSC</sub> = 10 MHz V <sub>OSC</sub> = 0.632 V <sub>PP</sub> ID <sub>o</sub> RF1 Bit = 1 PWDN RF2 Bit = 1 T <sub>A</sub> = +25°C (Note 11)		-79.18		dBc/Hz

## Electrical Characteristics (Continued)

$V_{CC} = V_P$  RF1 =  $V_P$  RF2 = 3.0V,  $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ , unless otherwise specified

Symbol	Parameter		Conditions	Value			Units
				Min	Typ	Max	
PHASE NOISE CHARACTERISTICS							
L <sub>N</sub> (f) RF2	RF2 Synthesizer Normalized Phase Noise Contribution (Note 10)		TCXO Reference Source ID <sub>o</sub> RF2 Bit = 1		-212.0		dBc/Hz
L(f) RF2	RF2 Synthesizer Single Side Band Phase Noise Measured	LMX2335U	f <sub>IN</sub> RF2 = 900 MHz f = 1 kHz Offset F <sub>φRF2</sub> = 200 kHz Loop Bandwidth = 12 kHz N = 4500 F <sub>OSC</sub> = 10 MHz V <sub>OSC</sub> = 0.632 V <sub>PP</sub> ID <sub>o</sub> RF2 Bit = 1 PWDN RF1 Bit = 1 T <sub>A</sub> = +25°C (Note 11)		-85.94		dBc/Hz
		LMX2336U	f <sub>IN</sub> RF2 = 900 MHz f = 1 kHz Offset F <sub>φRF2</sub> = 200 kHz Loop Bandwidth = 12 kHz N = 4500 F <sub>OSC</sub> = 10 MHz V <sub>OSC</sub> = 0.632 V <sub>PP</sub> ID <sub>o</sub> RF2 Bit = 1 PWDN RF1 Bit = 1 T <sub>A</sub> = +25°C (Note 11)		-85.94		dBc/Hz

**Note 4:** Some of the values in this range are illegal divide ratios ( $B < A$ ). To obtain continuous legal division, the Minimum Divide Ratio must be calculated. Use  $N \geq P * (P-1)$ , where  $P$  is the value selected for the prescaler.

**Note 5:** Refer to the LMX2335U and LMX2336U  $f_{IN}$  Sensitivity Test Setup section

**Note 6:** Refer to the LMX2335U and LMX2336U Charge Pump Test Setup section

**Note 7:** Refer to the Charge Pump Current Specification Definitions for details on how these measurements are made.

**Note 8:** Refer to the LMX2335U and LMX2336U  $OSC_{in}$  Sensitivity Test Setup section

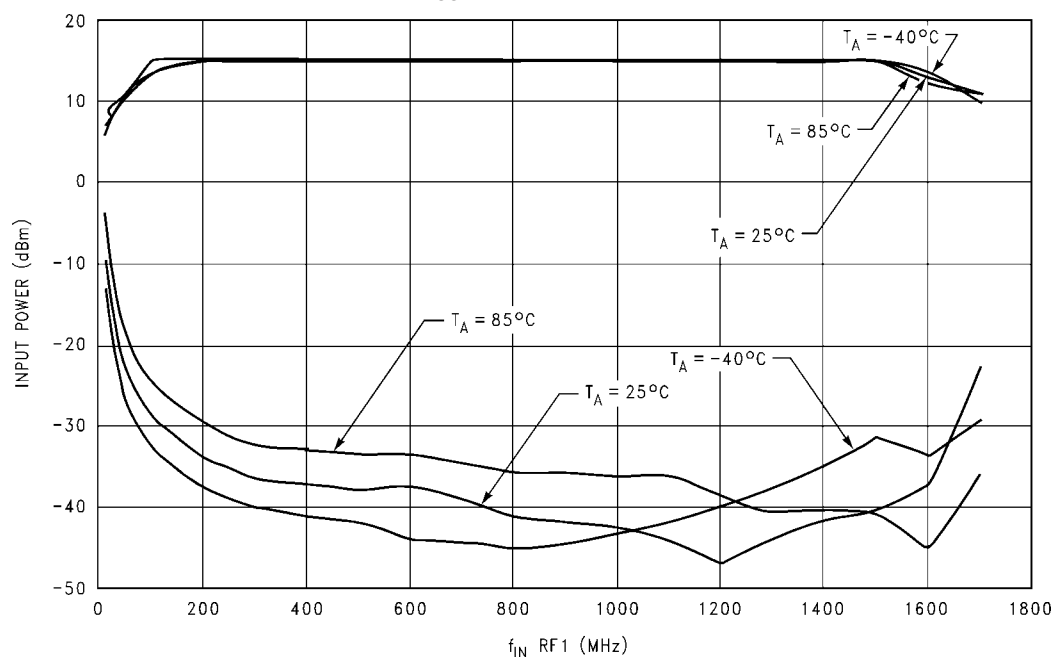
**Note 9:** Refer to the LMX2335U and LMX2336U Serial Data Input Timing section

**Note 10:** Normalized Phase Noise Contribution is defined as :  $L_N(f) = L(f) - 20 \log(N) - 10 \log(F_{\phi})$ , where  $L(f)$  is defined as the single side band phase noise measured at an offset frequency,  $f$ , in a 1 Hz bandwidth. The offset frequency,  $f$ , must be chosen sufficiently smaller than the PLL's loop bandwidth, yet large enough to avoid substantial phase noise contribution from the reference source.  $N$  is the value selected for the feedback divider and  $F_{\phi}$  is the RF1/RF2 phase detector comparison frequency..

**Note 11:** The synthesizer phase noise is measured with the LMX2335TMEB/LMX2335SLBEB or LMX2336TMEB/LMX2336SLBEB/LMX2336SLEEB Evaluation boards and the HP8566B Spectrum Analyzer.

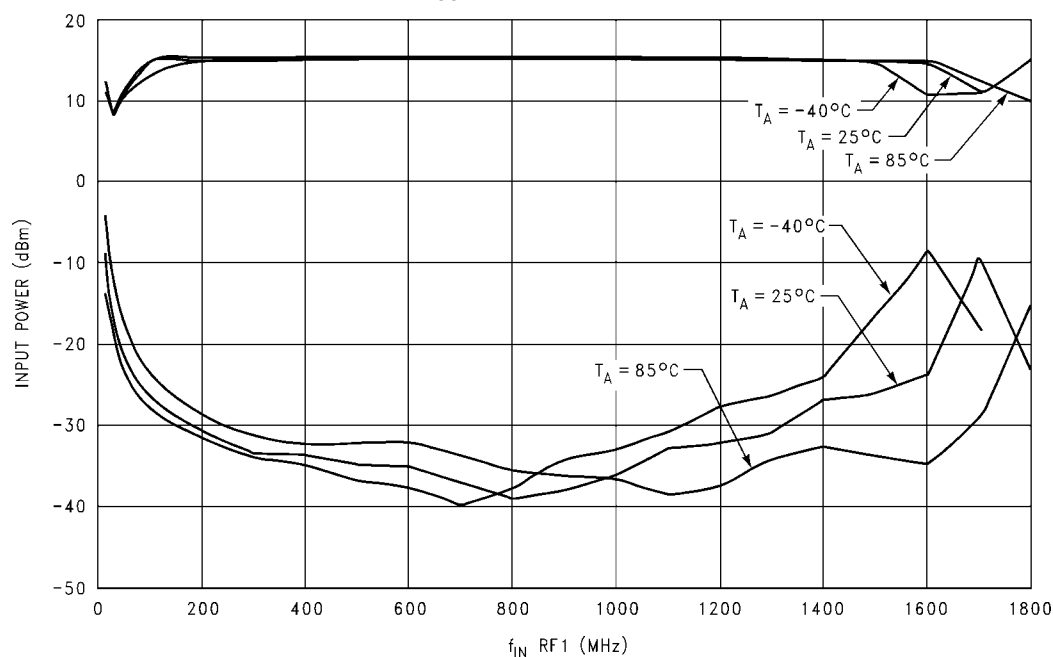
# Typical Performance Characteristics Sensitivity

LMX2335U  $f_{IN}$  RF1 Input Power Vs Frequency  
 $V_{CC} = V_P$  RF1 = 3.0V



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LMX2335U  $f_{IN}$  RF1 Input Power Vs Frequency  
 $V_{CC} = V_P$  RF1 = 5.5V

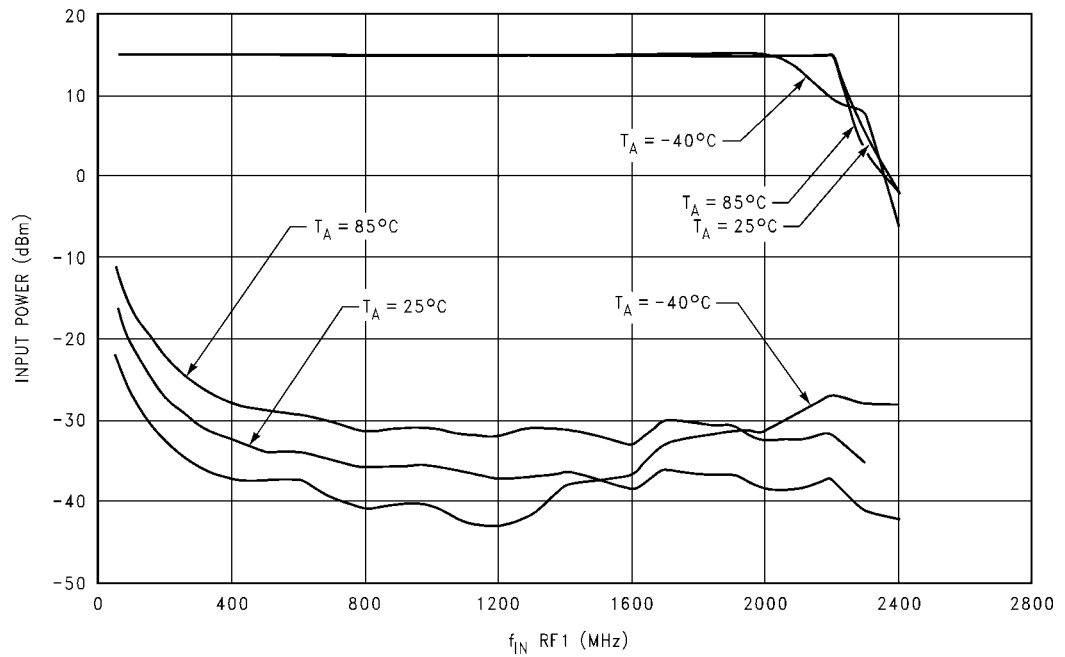


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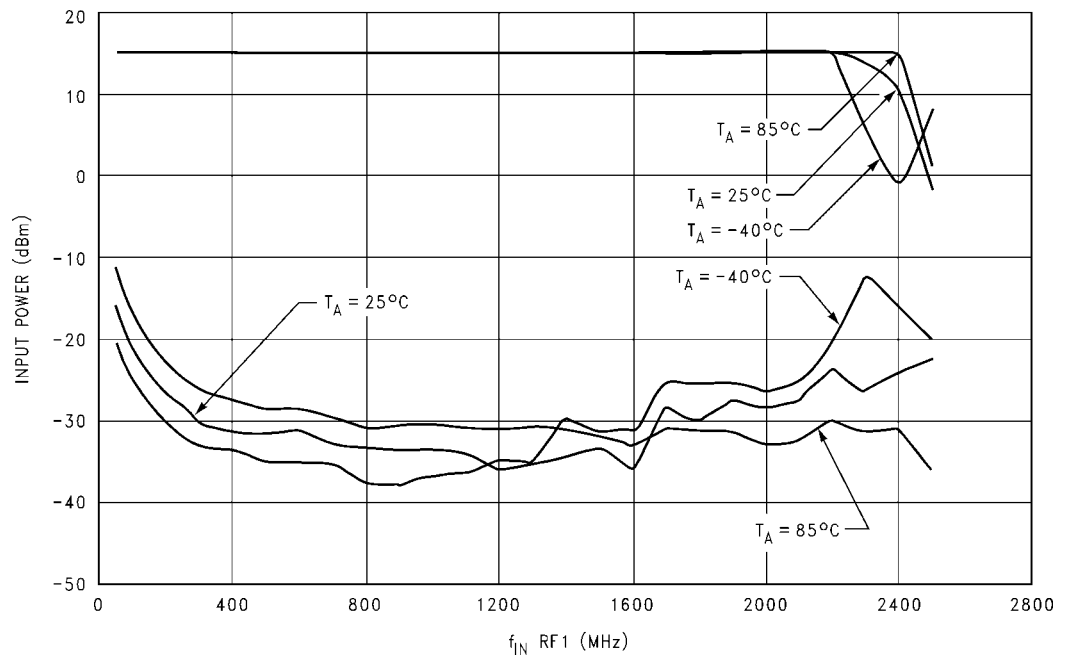
# Typical Performance Characteristics

## Sensitivity (Continued)

LMX2336U  $f_{IN}$  RF1 Input Power Vs Frequency  
 $V_{CC} = V_P$  RF1 = 3.0V



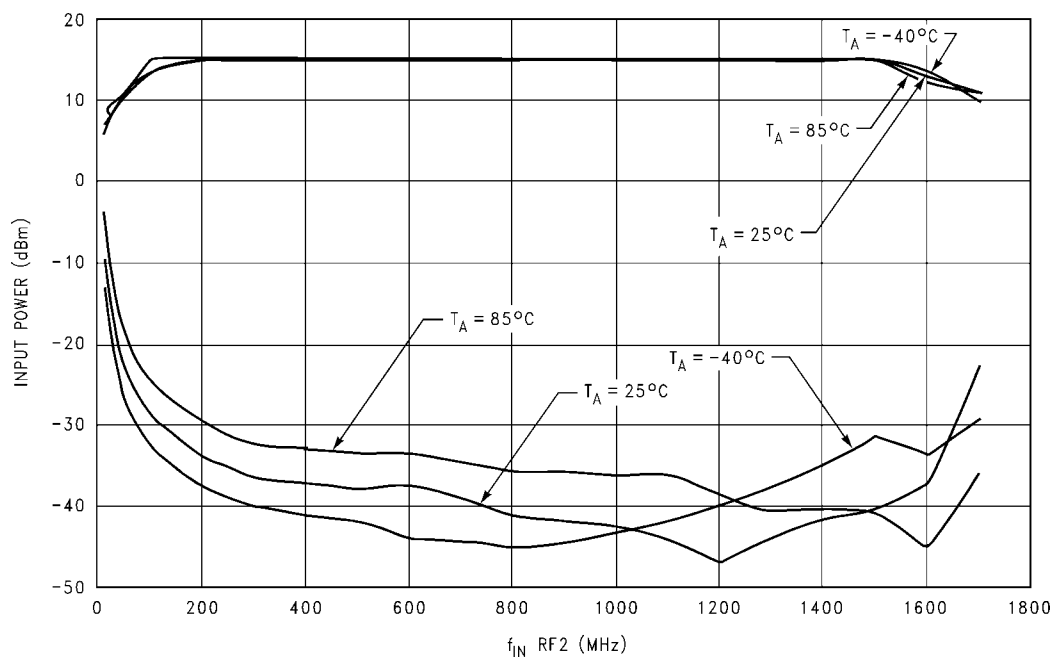
LMX2336U  $f_{IN}$  RF1 Input Power Vs Frequency  
 $V_{CC} = V_P$  RF1 = 5.5V



# Typical Performance Characteristics

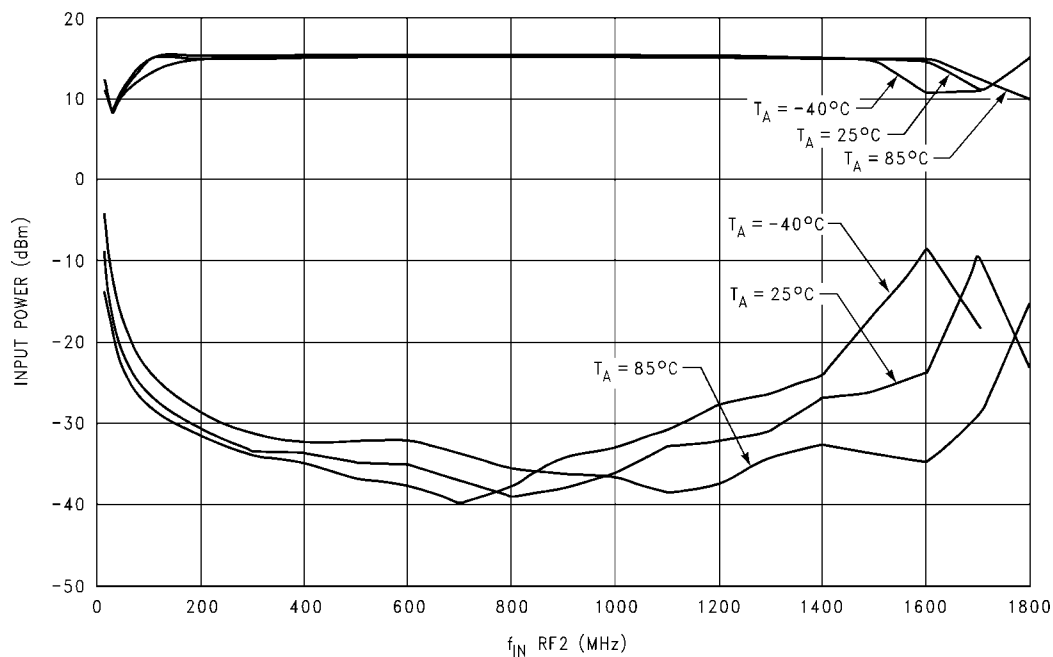
## Sensitivity (Continued)

LMX2335U and LMX2336U  $f_{IN}$  RF2 Input Power Vs Frequency  
 $V_{CC} = V_P$  RF2 = 3.0V



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LMX2335U and LMX2336U  $f_{IN}$  RF2 Input Power Vs Frequency  
 $V_{CC} = V_P$  RF2 = 5.5V

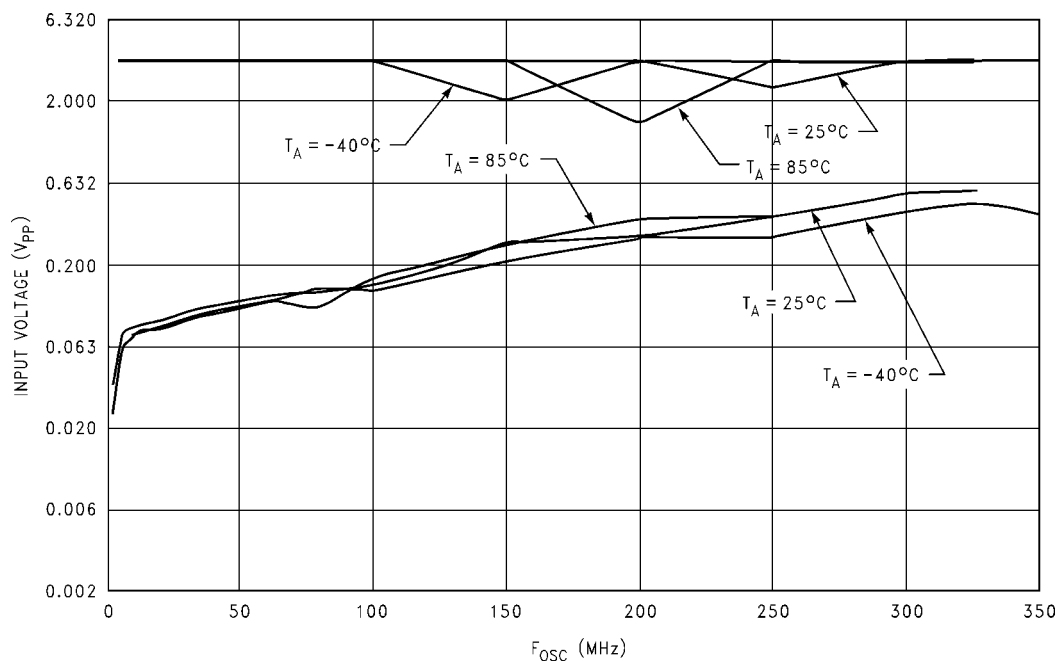


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# Typical Performance Characteristics

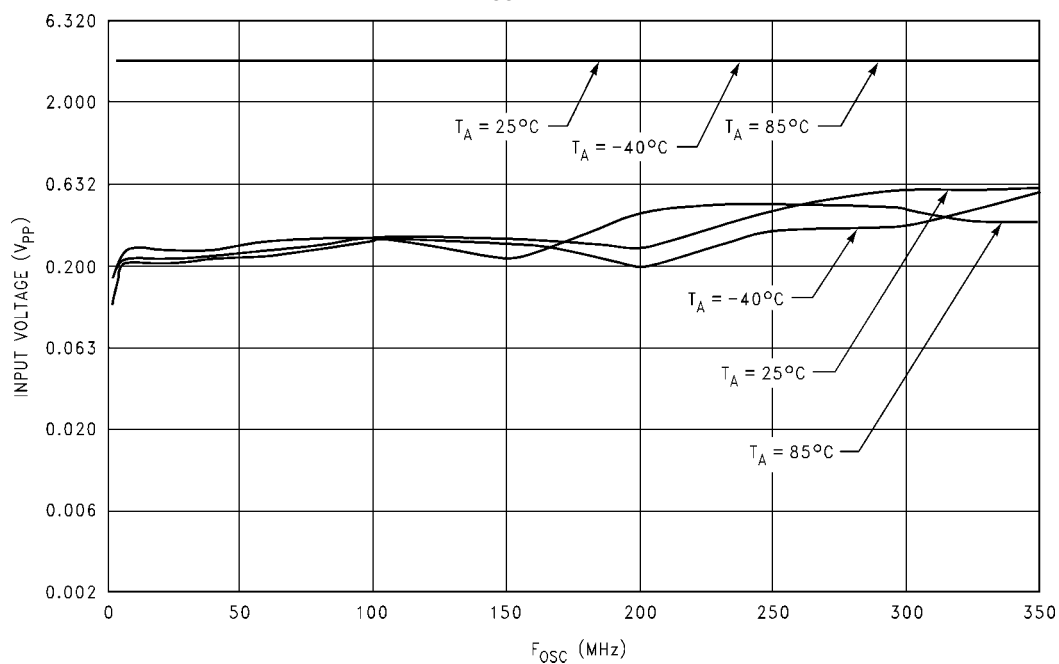
## Sensitivity (Continued)

LMX2335U and LMX2336U OSC<sub>in</sub> Input Voltage Vs Frequency  
V<sub>CC</sub> = 3.0V



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LMX2335U and LMX2336U OSC<sub>in</sub> Input Voltage Vs Frequency  
V<sub>CC</sub> = 5.5V

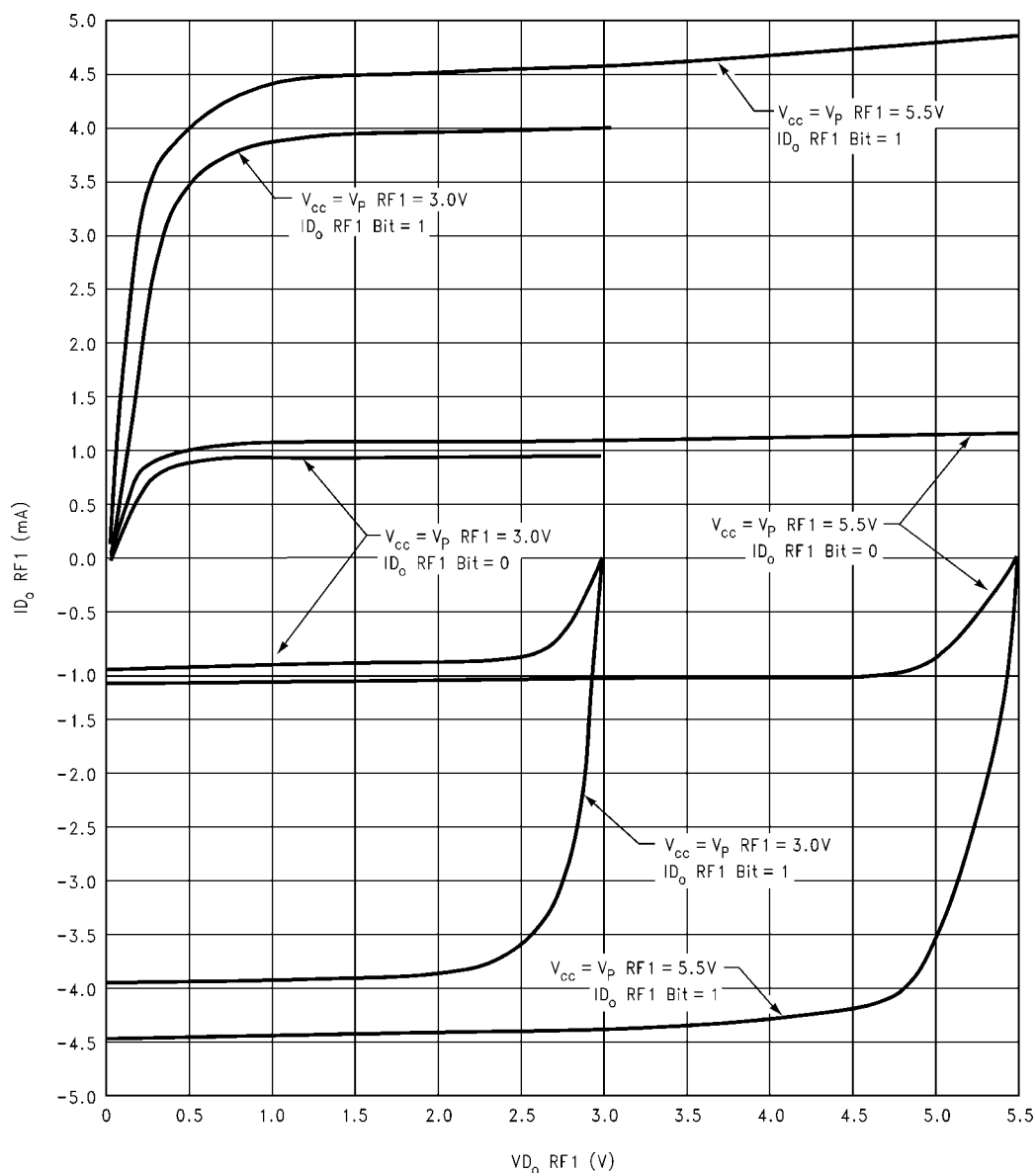


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# Typical Performance Characteristics Charge Pump

LMX2335U and LMX2336U RF1 Charge Pump Sweeps  
 $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$

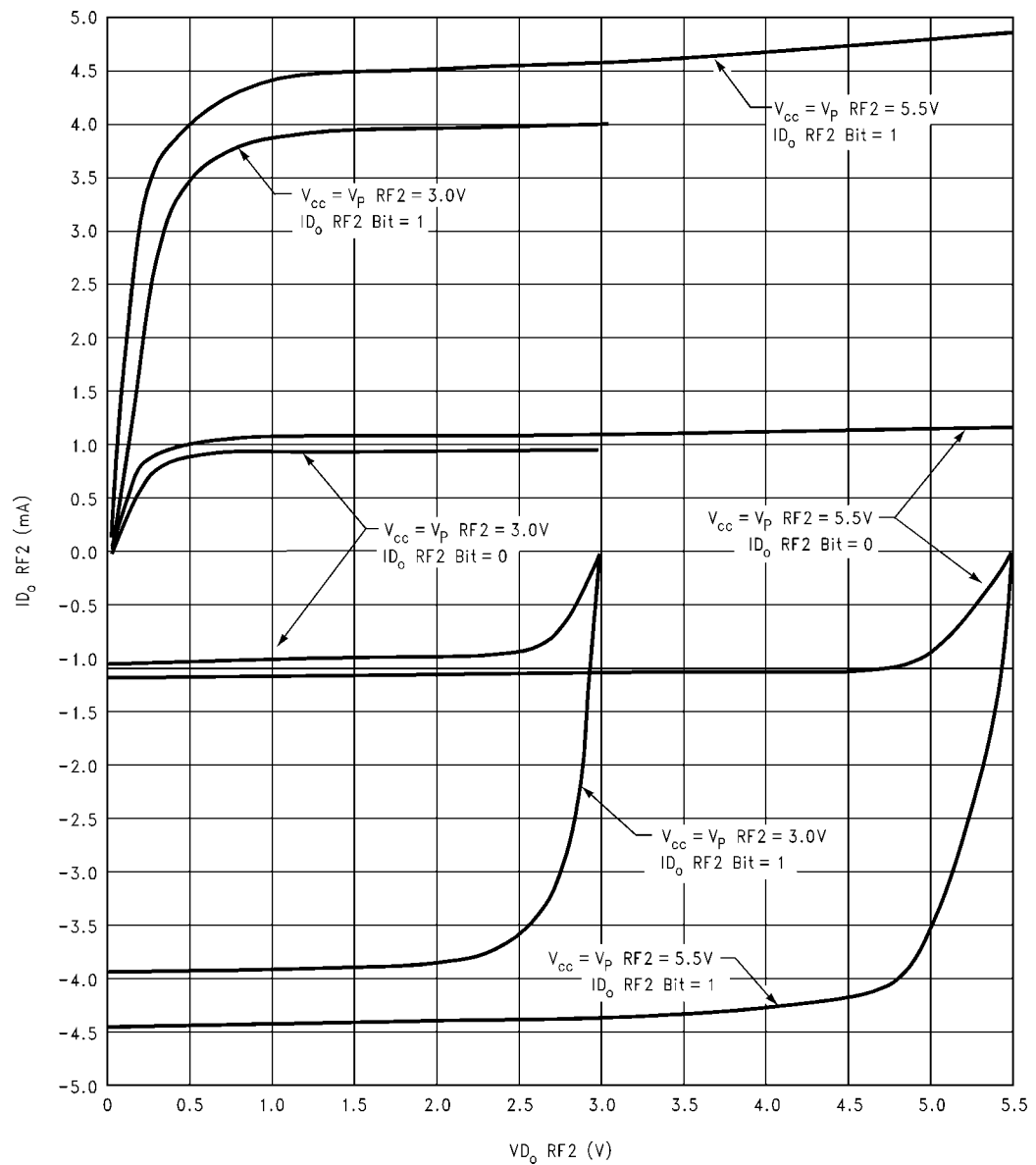


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# Typical Performance Characteristics

## Charge Pump (Continued)

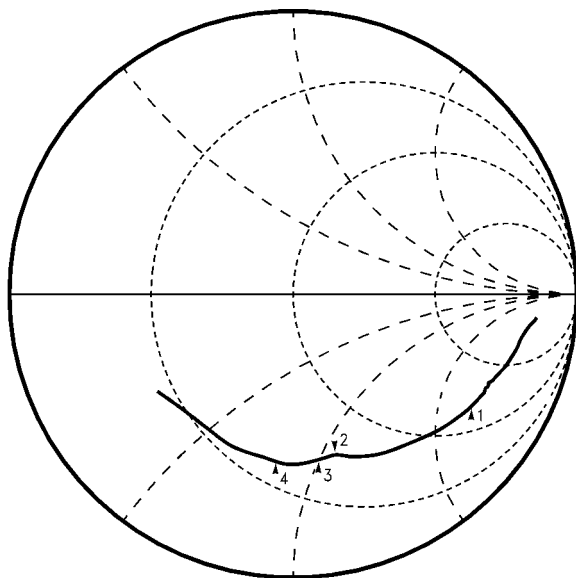
LMX2335U and LMX2336U RF2 Charge Pump Sweeps  
 $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$



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# Typical Performance Characteristics Input Impedance

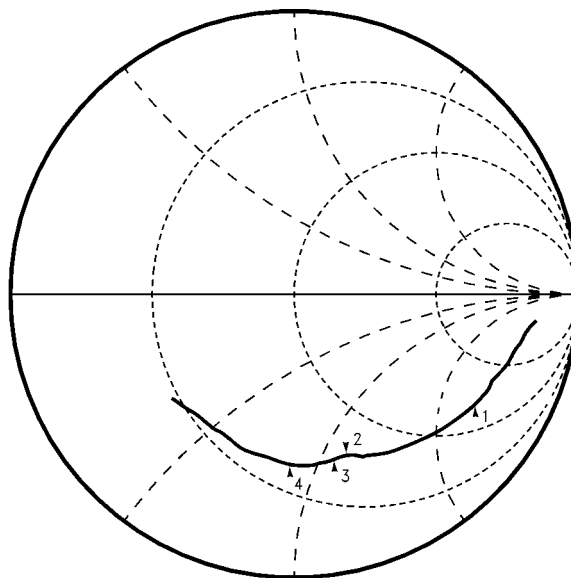
LMX2335U TSSOP and LMX2336U TSSOP  
 $f_{IN}$  RF1 and  $f_{IN}$  RF2 Input Impedance  
 $V_{CC} = 3.0V$ ,  $T_A = +25^\circ C$



Marker 1 = 900 MHz  
Marker 2 = 1800 MHz  
Marker 3 = 1900 MHz  
Marker 4 = 2000 MHz

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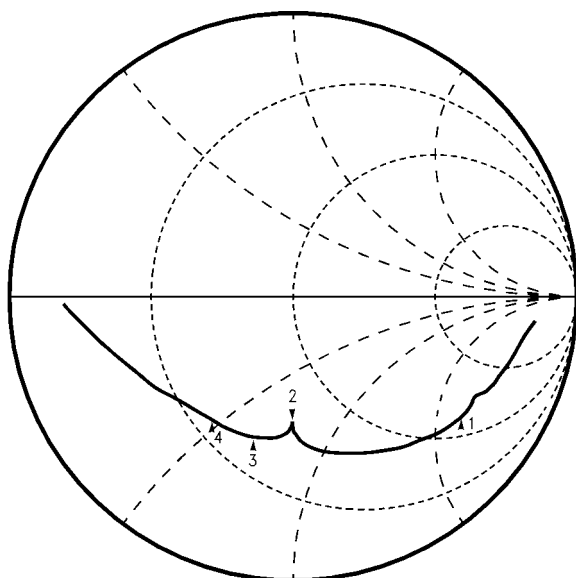
LMX2335U TSSOP and LMX2336U TSSOP  
 $f_{IN}$  RF1 and  $f_{IN}$  RF2 Input Impedance  
 $V_{CC} = 5.5V$ ,  $T_A = +25^\circ C$



Marker 1 = 900 MHz  
Marker 2 = 1800 MHz  
Marker 3 = 1900 MHz  
Marker 4 = 2000 MHz

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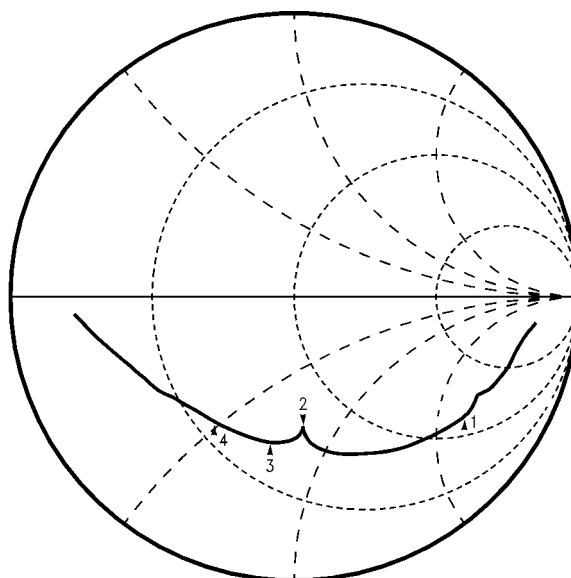
LMX2335U CSP and LMX2336U CSP  
 $f_{IN}$  RF1 and  $f_{IN}$  RF2 Input Impedance  
 $V_{CC} = 3.0V$ ,  $T_A = +25^\circ C$



Marker 1 = 900 MHz  
Marker 2 = 1800 MHz  
Marker 3 = 1900 MHz  
Marker 4 = 2000 MHz

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LMX2335U CSP and LMX2336U CSP  
 $f_{IN}$  RF1 and  $f_{IN}$  RF2 Input Impedance  
 $V_{CC} = 5.5V$ ,  $T_A = +25^\circ C$



Marker 1 = 900 MHz  
Marker 2 = 1800 MHz  
Marker 3 = 1900 MHz  
Marker 4 = 2000 MHz

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# Typical Performance Characteristics Input Impedance (Continued)

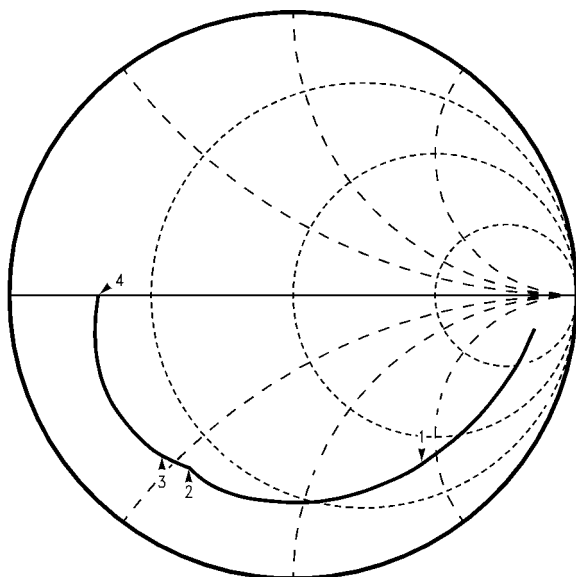
LMX2335U/LMX2336U TSSOP and LMX2335U/LMX2336U CSP  $f_{IN}$  RF1 and  $f_{IN}$  RF2 Input Impedance Table

$f_{IN}$ (MHz)	LMX2335U TSSOP/LMX2336U TSSOP ( $Z_{IN}$ RF1 and $Z_{IN}$ RF2)										LMX2335U CSP/LMX2336U CSP ( $Z_{IN}$ RF1 and $Z_{IN}$ RF2)									
	$V_{CC} = V_P$ RF1 = $V_P$ RF2 = 3.0V ( $T_A = 25^\circ\text{C}$ )										$V_{CC} = V_P$ RF1 = $V_P$ RF2 = 3.0V ( $T_A = 25^\circ\text{C}$ )									
	$ I_T $	$\angle I_T$	$\frac{R}{Z_{IN}}$ ( $\Omega$ )	$\frac{X}{Z_{IN}}$ ( $\Omega$ )	$ Z_{IN} $ ( $\Omega$ )	$ I_T $	$\angle I_T$	$\frac{R}{Z_{IN}}$ ( $\Omega$ )	$\frac{X}{Z_{IN}}$ ( $\Omega$ )	$ Z_{IN} $ ( $\Omega$ )	$ I_T $	$\angle I_T$	$\frac{R}{Z_{IN}}$ ( $\Omega$ )	$\frac{X}{Z_{IN}}$ ( $\Omega$ )	$ Z_{IN} $ ( $\Omega$ )	$ I_T $	$\angle I_T$	$\frac{R}{Z_{IN}}$ ( $\Omega$ )	$\frac{X}{Z_{IN}}$ ( $\Omega$ )	$ Z_{IN} $ ( $\Omega$ )
100	0.862	-6.23	439.774	-319.866	543.798	0.862	-6.07	448.230	-318.841	550.064	0.864	-6.44	431.004	-330.013	542.838	0.864	-6.30	438.240	-327.814	547.281
200	0.834	-9.30	307.614	-272.274	410.803	0.834	-9.00	316.479	-271.581	417.031	0.836	-9.88	291.252	-277.923	402.577	0.836	-9.57	300.190	-277.552	408.838
300	0.820	-12.11	237.700	-249.291	344.452	0.821	-11.66	247.264	-251.098	352.406	0.821	-13.24	215.318	-248.361	328.702	0.821	-12.76	224.824	-249.637	335.919
400	0.808	-15.25	185.048	-227.171	293.001	0.808	-14.61	194.668	-229.054	300.601	0.808	-16.88	163.190	-219.893	273.832	0.808	-16.24	171.345	-222.518	280.944
500	0.796	-18.51	147.785	-203.923	251.843	0.796	-17.66	156.935	-207.313	260.014	0.793	-20.90	126.193	-191.939	229.707	0.794	-20.00	133.885	-196.200	237.528
600	0.781	-21.81	122.091	-181.461	218.710	0.782	-20.70	130.906	-185.850	227.325	0.775	-24.82	102.956	-168.026	197.060	0.777	-23.70	109.531	-172.887	204.663
700	0.765	-24.72	106.107	-163.758	195.129	0.767	-23.45	113.780	-168.514	203.329	0.749	-28.29	90.820	-146.582	172.437	0.752	-27.02	96.279	-151.333	179.363
800	0.760	-28.35	87.984	-150.524	174.352	0.762	-26.97	94.255	-155.481	191.819	0.742	-31.22	79.737	-136.782	158.327	0.746	-29.85	84.470	-141.473	164.772
900	0.747	-32.60	73.777	-134.500	153.406	0.750	-30.95	79.270	-139.668	160.596	0.739	-36.04	64.577	-123.951	139.764	0.742	-34.37	69.006	-128.610	145.954
1000	0.732	-36.68	64.122	-120.908	136.859	0.735	-34.73	69.215	-126.104	143.851	0.719	-41.44	55.019	-108.415	121.577	0.723	-39.46	58.684	-113.123	127.439
1100	0.717	-41.25	55.780	-108.398	121.908	0.720	-39.12	60.041	-113.215	128.151	0.694	-47.27	48.056	-94.403	105.931	0.696	-45.08	51.159	-98.547	111.035
1200	0.698	-46.24	49.180	-96.605	108.403	0.702	-43.84	52.848	-101.254	114.216	0.669	-53.59	42.269	-82.401	92.610	0.674	-51.01	45.061	-86.368	97.434
1300	0.678	-51.43	43.982	-86.291	96.853	0.683	-48.77	47.173	-90.676	102.212	0.641	-60.42	37.856	-71.653	81.039	0.647	-57.50	40.230	-75.400	85.461
1400	0.663	-56.68	39.397	-77.901	87.296	0.667	-53.71	42.317	-82.070	92.337	0.610	-68.33	34.108	-61.481	70.308	0.613	-64.90	36.477	-64.572	74.424
1500	0.649	-62.08	35.566	-70.500	78.953	0.653	-58.74	38.281	-74.569	83.821	0.577	-77.01	31.049	-52.388	60.898	0.581	-73.18	33.054	-55.554	64.649
1600	0.630	-67.58	32.912	-63.544	71.562	0.634	-63.96	35.335	-67.423	76.121	0.539	-84.86	29.732	-44.952	53.895	0.543	-80.36	31.554	-48.119	57.597
1700	0.608	-72.22	31.555	-57.996	66.030	0.614	-68.51	33.590	-61.632	70.191	0.477	-97.97	100.359	-58.171	115.999	0.487	-84.99	33.106	-42.105	53.562
1800	0.595	-75.66	30.440	-54.462	62.392	0.601	-71.81	32.358	-57.943	66.366	0.455	-99.90	32.829	-37.624	49.933	0.468	-85.87	33.885	-40.554	52.847
1900	0.598	-80.06	27.915	-51.164	58.284	0.602	-76.22	29.678	-54.335	61.912	0.493	-87.34	29.357	-38.214	48.189	0.500	-88.90	29.576	-39.369	49.241
2000	0.607	-85.31	24.914	-47.651	53.771	0.607	-81.32	26.675	-50.603	57.203	0.520	-79.89	25.120	-35.225	43.264	0.521	-84.05	26.395	-37.576	45.921

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# Typical Performance Characteristics Input Impedance (Continued)

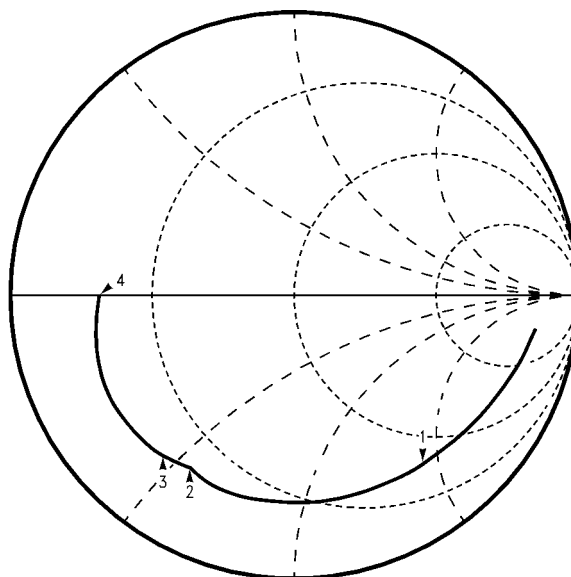
LMX2336U UTCSP  
 $f_{IN}$  RF1 and  $f_{IN}$  RF2 Input Impedance  
 $V_{CC} = 3.0V$ ,  $T_A = +25^\circ C$



Marker 1 = 900 MHz  
 Marker 2 = 1800 MHz  
 Marker 3 = 1900 MHz  
 Marker 4 = 2500 MHz

10136797

LMX2336U UTCSP  
 $f_{IN}$  RF1 and  $f_{IN}$  RF2 Input Impedance  
 $V_{CC} = 5.5V$ ,  $T_A = +25^\circ C$



Marker 1 = 900 MHz  
 Marker 2 = 1800 MHz  
 Marker 3 = 1900 MHz  
 Marker 4 = 2500 MHz

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# Typical Performance Characteristics Input Impedance (Continued)

LMX2336U UTCSP  $f_{IN}$  RF1 and  $f_{IN}$  RF2 Input Impedance Table

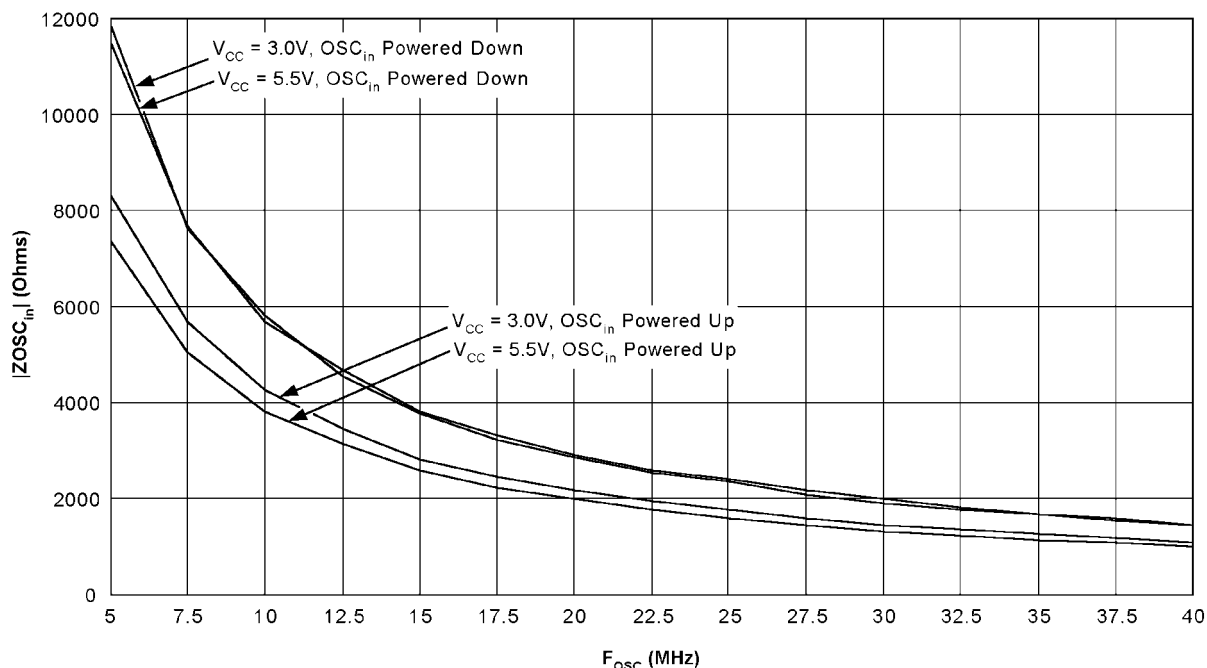
LMX2336U UTCSP $Z_{in}$ RF1 and $Z_{in}$ RF2									
$f_{in}$ (MHz)	$V_{CC} = V_P$ RF1 = $V_P$ RF2 = 3.0V ( $T_A = 25^\circ\text{C}$ )					$V_{CC} = V_P$ RF1 = $V_P$ RF2 = 5.5V ( $T_A = 25^\circ\text{C}$ )			
	$ S_{11} $	$\angle\Gamma$	$\frac{Re}{Z_{in}}$ ( $\Omega$ )	$\frac{Im}{Z_{in}}$ ( $\Omega$ )	$ Z_{in} $ ( $\Omega$ )	$ S_{11} $	$\angle\Gamma$	$\frac{Re}{Z_{in}}$ ( $\Omega$ )	$\frac{Im}{Z_{in}}$ ( $\Omega$ )
100	0.86	-8.67	335.53	-330.26	470.80	0.86	-8.61	333.98	-330.26
200	0.83	-13.59	206.36	-258.74	330.95	0.83	-13.55	207.11	-258.92
300	0.81	-18.53	143.19	-214.36	257.79	0.81	-18.45	144.05	-214.75
400	0.80	-23.67	103.09	-183.95	210.86	0.80	-23.63	103.36	-184.12
500	0.79	-29.24	76.58	-157.24	174.89	0.79	-29.07	77.30	-157.87
600	0.77	-34.87	61.79	-133.64	147.24	0.77	-34.64	62.46	-134.31
700	0.76	-40.52	50.03	-116.97	127.23	0.76	-40.33	50.42	-117.43
800	0.76	-46.45	39.82	-103.86	111.24	0.76	-46.18	40.22	-104.42
900	0.75	-53.27	32.87	-90.33	96.13	0.75	-52.89	33.27	-90.97
1000	0.74	-60.04	27.98	-79.30	84.09	0.74	-59.70	28.24	-79.77
1100	0.73	-66.62	24.49	-70.27	74.42	0.73	-66.10	24.81	-70.90
1200	0.73	-74.07	20.63	-62.00	65.34	0.73	-73.57	20.85	-62.52
1300	0.73	-81.67	17.67	-54.66	57.45	0.73	-81.15	17.86	-55.13
1400	0.73	-89.59	15.34	-47.95	50.34	0.73	-88.94	15.51	-48.47
1500	0.73	-97.85	13.48	-41.75	43.87	0.73	-97.12	13.63	-42.27
1600	0.73	-106.72	11.96	-35.80	37.74	0.73	-105.87	12.09	-36.34
1700	0.72	-115.82	11.22	-30.21	32.22	0.72	-114.76	11.35	-30.82
1800	0.70	-123.41	11.28	-25.85	28.20	0.70	-122.28	11.40	-26.45
1900	0.72	-130.06	9.80	-22.22	24.29	0.72	-129.92	9.86	-22.61
2000	0.74	-140.55	8.41	-17.48	19.39	0.74	-139.88	8.44	-17.80
2100	0.74	-150.74	7.97	-12.74	15.03	0.74	-150.01	7.99	-13.07
2200	0.73	-160.86	8.02	-8.22	11.48	0.73	-160.03	8.04	-8.58
2300	0.71	-170.43	8.54	-4.06	9.46	0.71	-169.62	8.55	-4.41
2400	0.69	-179.08	9.17	-0.39	9.18	0.69	-178.32	9.17	-0.71
2500	0.67	-172.36	9.92	3.20	10.43	0.67	-173.11	9.91	2.89

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# Typical Performance Characteristics

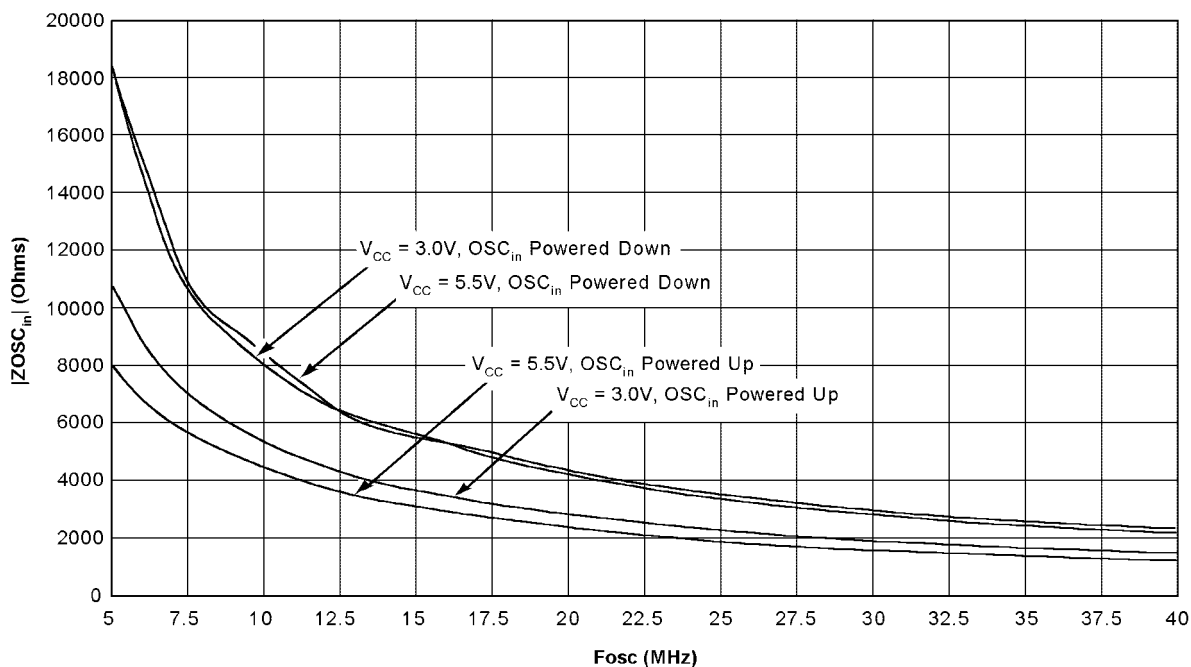
## Input Impedance (Continued)

LMX2335U TSSOP and LMX2336U TSSOP  
OSC<sub>in</sub> Input Impedance Vs Frequency  
T<sub>A</sub> = +25°C



10136776

LMX2335U CSP and LMX2336U CSP  
OSC<sub>in</sub> Input Impedance Vs Frequency  
T<sub>A</sub> = +25°C



10136777



# Typical Performance Characteristics Input Impedance (Continued)

LMX2335U/LMX2336U TSSOP and LMX2335U/LMX2336U CSP OSC<sub>in</sub> Input Impedance Table

LMX2336U TSSOP/LMX2336U TSSOP ZOSC <sub>in</sub>										LMX2336U CSP/LMX2336U CSP ZOSC <sub>in</sub>									
V <sub>CC</sub> = 3.0V (T <sub>A</sub> = 25°C)					V <sub>CC</sub> = 5.0V (T <sub>A</sub> = 25°C)					V <sub>CC</sub> = 3.0V (T <sub>A</sub> = 25°C)					V <sub>CC</sub> = 5.0V (T <sub>A</sub> = 25°C)				
OSC <sub>in</sub> BUFFER POWERED ON					OSC <sub>in</sub> BUFFER POWERED DOWN					OSC <sub>in</sub> BUFFER POWERED ON					OSC <sub>in</sub> BUFFER POWERED DOWN				
F <sub>osc</sub> (MHz)	Re ZOSC <sub>in</sub> (Ω)	Im ZOSC <sub>in</sub> (Ω)	Re ZOSC <sub>in</sub> (Ω)	Im ZOSC <sub>in</sub> (Ω)	Re ZOSC <sub>in</sub> (Ω)	Im ZOSC <sub>in</sub> (Ω)	Re ZOSC <sub>in</sub> (Ω)	Im ZOSC <sub>in</sub> (Ω)	Re ZOSC <sub>in</sub> (Ω)	Re ZOSC <sub>in</sub> (Ω)	Im ZOSC <sub>in</sub> (Ω)	Re ZOSC <sub>in</sub> (Ω)	Im ZOSC <sub>in</sub> (Ω)	Re ZOSC <sub>in</sub> (Ω)	Re ZOSC <sub>in</sub> (Ω)	Im ZOSC <sub>in</sub> (Ω)	Re ZOSC <sub>in</sub> (Ω)	Im ZOSC <sub>in</sub> (Ω)	Re ZOSC <sub>in</sub> (Ω)
5.0	2291.113	-4000.376	8321.872	985.863	-11825.259	11868.234	2832.878	-4774.635	7342.992	5107.688	-9328.374	10809.27	4154.194	-18073.24	18544.52	4656.963	-6544.007	8656.318	4154.104
7.5	12102.388	-6538.167	6687.218	294.460	-7543.322	7545.994	3267.479	-4861.023	8232.579	2240.061	-4544.470	6903.146	1571.337	-10705.48	10525.74	2656.379	-4998.176	5646.179	1812.311
10.0	791.970	-4218.628	4292.353	208.942	-5793.060	5799.207	779.926	-3754.673	3826.889	1644.888	-5170.600	5432.325	1046.681	-4350.651	4350.74	1192.723	-4029.216	4512.261	876.928
12.5	427.894	-3418.676	3459.456	197.674	-4547.064	4551.307	544.280	-3076.845	3128.584	1248.750	-4345.537	4573.153	727.756	-4341.105	4385.735	1192.342	-3496.985	3663.045	889.897
15.0	343.020	-2817.902	2838.754	161.801	-3761.566	3765.044	416.844	-2536.243	2570.238	872.629	-3558.426	3663.861	482.219	-3658.272	3675.536	806.006	-2877.501	3088.519	436.542
17.5	319.446	-2439.647	2460.065	141.526	-3203.261	3206.467	369.867	-2162.584	2214.372	681.377	-3158.030	3232.825	296.061	-4799.817	4809.036	697.781	-2605.665	2467.992	309.618
20.0	228.026	-2179.146	2191.006	83.505	-2879.021	2880.631	227.640	-1874.267	1987.347	599.597	-2791.612	2847.441	194.872	-4242.476	4246.948	554.417	-2318.061	2384.315	302.378
22.5	211.699	-1932.636	1944.061	86.108	-2543.320	2545.222	214.873	-1741.021	1754.310	442.147	-2532.525	2551.129	186.123	-3777.847	3782.429	495.437	-2041.770	2056.100	198.193
25.0	163.618	-1762.803	1770.480	85.270	-2240.221	2241.923	169.812	-1586.814	1598.857	444.524	-2281.024	2304.357	170.072	-3402.400	3406.648	424.556	-1815.270	1812.988	174.460
27.5	193.733	-1689.620	1698.030	88.675	-2198.263	2197.405	160.401	-1435.713	1444.646	367.245	-2060.013	2062.491	191.728	-3114.867	3120.783	373.066	-1714.705	1756.195	159.273
30.0	148.446	-1463.071	1470.583	81.310	-1926.009	1928.004	141.201	-1314.929	1322.520	356.662	-1993.442	1996.747	188.260	-2837.317	2843.527	357.340	-1587.676	1608.182	157.454
32.5	130.683	-1340.206	1348.562	48.948	-1795.854	1791.445	121.612	-1213.493	1219.462	348.616	-1776.646	1810.480	128.014	-2654.486	2667.608	332.665	-1481.571	1488.018	157.389
35.0	129.059	-1255.024	1261.349	38.046	-1692.230	1682.666	116.385	-1131.429	1137.399	302.652	-1648.266	1675.961	85.424	-2471.170	2473.011	299.813	-1338.125	1390.849	155.530
37.5	115.848	-1178.854	1184.632	37.202	-1547.816	1548.263	100.381	-1064.491	1070.098	300.020	-1549.601	1578.377	117.732	-2231.664	2234.684	284.854	-1274.270	1325.774	144.727
40.0	108.280	-1089.031	1095.296	36.351	-1439.460	1439.919	100.267	-985.544	990.831	281.334	-1454.266	1481.260	81.318	-2182.472	2183.987	273.323	-1199.916	1235.054	152.283

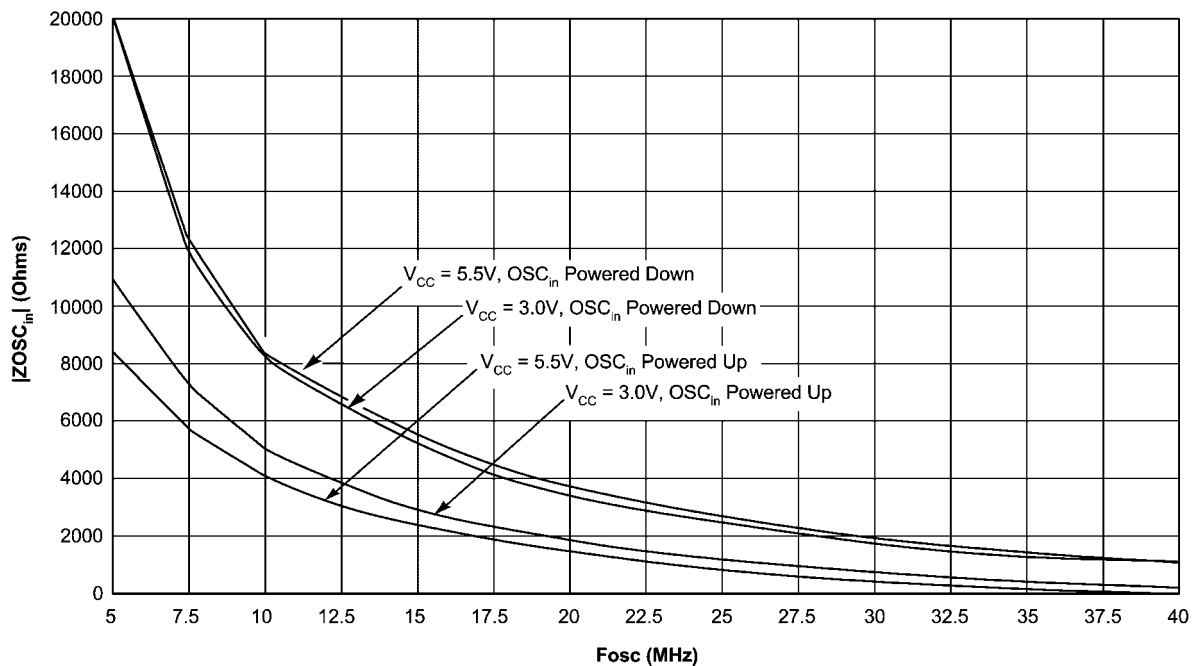
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# Typical Performance Characteristics

## Input Impedance (Continued)

LMX2336U UTCSP  
OSC<sub>in</sub> Input Impedance Vs Frequency  
T<sub>A</sub> = +25°C



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# Typical Performance Characteristics

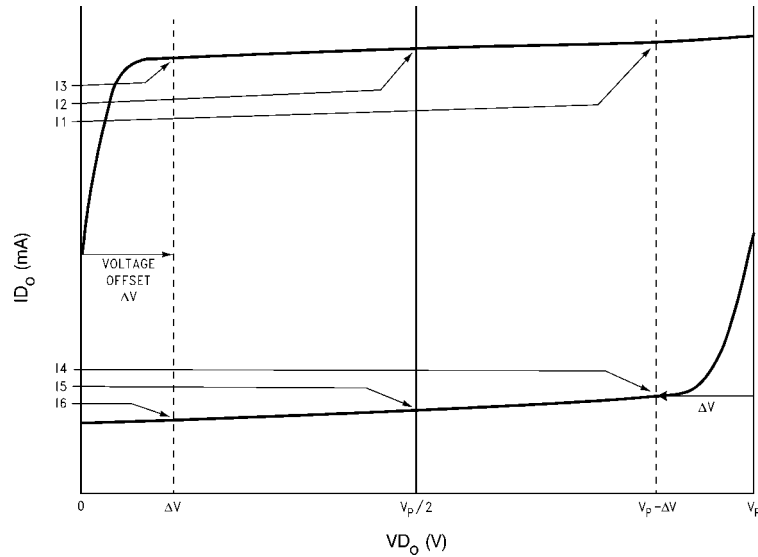
## Input Impedance (Continued)

LMX2336U UTCSP OSC<sub>in</sub> Input Impedance Table

LMX2336U UTCSP ZOSC <sub>in</sub>												
V <sub>CC</sub> = 3.0V (T <sub>A</sub> = 25°C)							V <sub>CC</sub> = 5.5V (T <sub>A</sub> = 25°C)					
F <sub>osc</sub> (MHz)	OSC <sub>in</sub> BUFFER POWERED UP			OSC <sub>in</sub> BUFFER POWERED DOWN			OSC <sub>in</sub> BUFFER POWERED UP			OSC <sub>in</sub> BUFFER POWERED DOWN		
	I <sub>in</sub> ZOSC <sub>in</sub> (Ω)	I <sub>in</sub> ZOSC <sub>in</sub> (Ω)	I <sub>in</sub> ZOSC <sub>in</sub> (Ω)	I <sub>in</sub> ZOSC <sub>in</sub> (Ω)	I <sub>in</sub> ZOSC <sub>in</sub> (Ω)	I <sub>in</sub> ZOSC <sub>in</sub> (Ω)	I <sub>in</sub> ZOSC <sub>in</sub> (Ω)	I <sub>in</sub> ZOSC <sub>in</sub> (Ω)	I <sub>in</sub> ZOSC <sub>in</sub> (Ω)	I <sub>in</sub> ZOSC <sub>in</sub> (Ω)	I <sub>in</sub> ZOSC <sub>in</sub> (Ω)	I <sub>in</sub> ZOSC <sub>in</sub> (Ω)
5.0	5918.57	-9897.80	11532.39	1822.62	-19947.73	20030.82	4982.73	-7668.32	9144.98	2478.02	-19591.11	19747.21
7.5	3097.46	-7441.43	8060.35	2238.93	-12114.22	12319.38	2742.97	-6062.16	6653.85	2483.54	-12531.99	12775.71
10.0	1695.22	-5720.83	5966.72	998.16	-9046.84	9101.74	1582.29	-4875.36	5125.70	1064.38	-9063.97	9126.25
12.5	1241.03	-4759.14	4918.29	660.39	-7338.93	7368.58	1150.39	-4034.66	4195.46	621.48	-7679.86	7704.97
15.0	820.55	-3955.33	4039.55	471.57	-6142.40	6160.48	861.48	-3448.80	3654.76	591.34	-6481.87	6508.79
17.5	646.18	-3417.20	3477.76	317.24	-5165.41	5175.14	599.49	-3009.04	3068.18	154.67	-5518.01	5520.17
20.0	520.20	-3006.22	3050.90	223.35	-4567.95	4573.41	491.78	-2647.38	2692.67	120.99	-4867.07	4868.57
22.5	459.63	-2666.05	2705.38	219.57	-4040.96	4046.92	396.64	-2342.62	2375.96	137.85	-4301.63	4303.84
25.0	391.21	-2398.19	2429.89	172.20	-3664.77	3668.81	323.46	-2108.25	2132.92	89.00	-3864.60	3865.62
27.5	348.79	-2210.66	2238.01	169.02	-3291.50	3295.84	312.14	-1920.70	1945.90	114.48	-3476.68	3478.56
30.0	285.07	-1996.71	2016.96	110.02	-3005.42	3007.43	260.59	-1763.82	1782.97	121.11	-3185.26	3187.56
32.5	267.83	-1847.30	1866.61	117.14	-2725.46	2727.97	239.41	-1612.35	1630.02	111.70	-2876.34	2878.50
35.0	252.27	-1719.32	1737.73	114.38	-2558.44	2561.00	222.16	-1503.76	1520.08	115.42	-2690.37	2692.84
37.5	224.94	-1639.80	1655.15	70.31	-2408.64	2409.67	191.46	-1422.88	1435.71	48.06	-2550.41	2550.86
40.0	208.96	-1512.91	1527.27	76.50	-2242.79	2244.09	180.75	-1329.24	1341.47	72.61	-2353.73	2354.85

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## Charge Pump Current Specification Definitions



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$I_1$  = Charge Pump Sink Current at  $VD_o = V_P - \Delta V$

$I_2$  = Charge Pump Sink Current at  $VD_o = V_P/2$

$I_3$  = Charge Pump Sink Current at  $VD_o = \Delta V$

$I_4$  = Charge Pump Source Current at  $VD_o = V_P - \Delta V$

$I_5$  = Charge Pump Source Current at  $VD_o = V_P/2$

$I_6$  = Charge Pump Source Current at  $VD_o = \Delta V$

$\Delta V$  = Voltage offset from the positive and negative rails. Dependent on the VCO tuning range relative to  $V_{CC}$  and GND. Typical values are between 0.5V and 1.0V.

$V_P$  refers to either  $V_P$  RF1 or  $V_P$  RF2

$VD_o$  refers to either  $VD_o$  RF1 or  $VD_o$  RF2

$ID_o$  refers to either  $ID_o$  RF1 or  $ID_o$  RF2

### Charge Pump Output Current Magnitude Variation Vs Charge Pump Output Voltage

$$ID_o \text{ Vs } VD_o = \frac{(|I_1| - |I_3|)}{(|I_1| + |I_3|)} \times 100\%$$

$$= \frac{(|I_4| - |I_6|)}{(|I_4| + |I_6|)} \times 100\%$$

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### Charge Pump Output Sink Current Vs Charge Pump Output Source Current Mismatch

$$ID_o \text{ SINK Vs } ID_o \text{ SOURCE} = \frac{|I_2| - |I_5|}{\frac{1}{2}(|I_2| + |I_5|)} \times 100\%$$

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### Charge Pump Output Current Magnitude Variation Vs Temperature

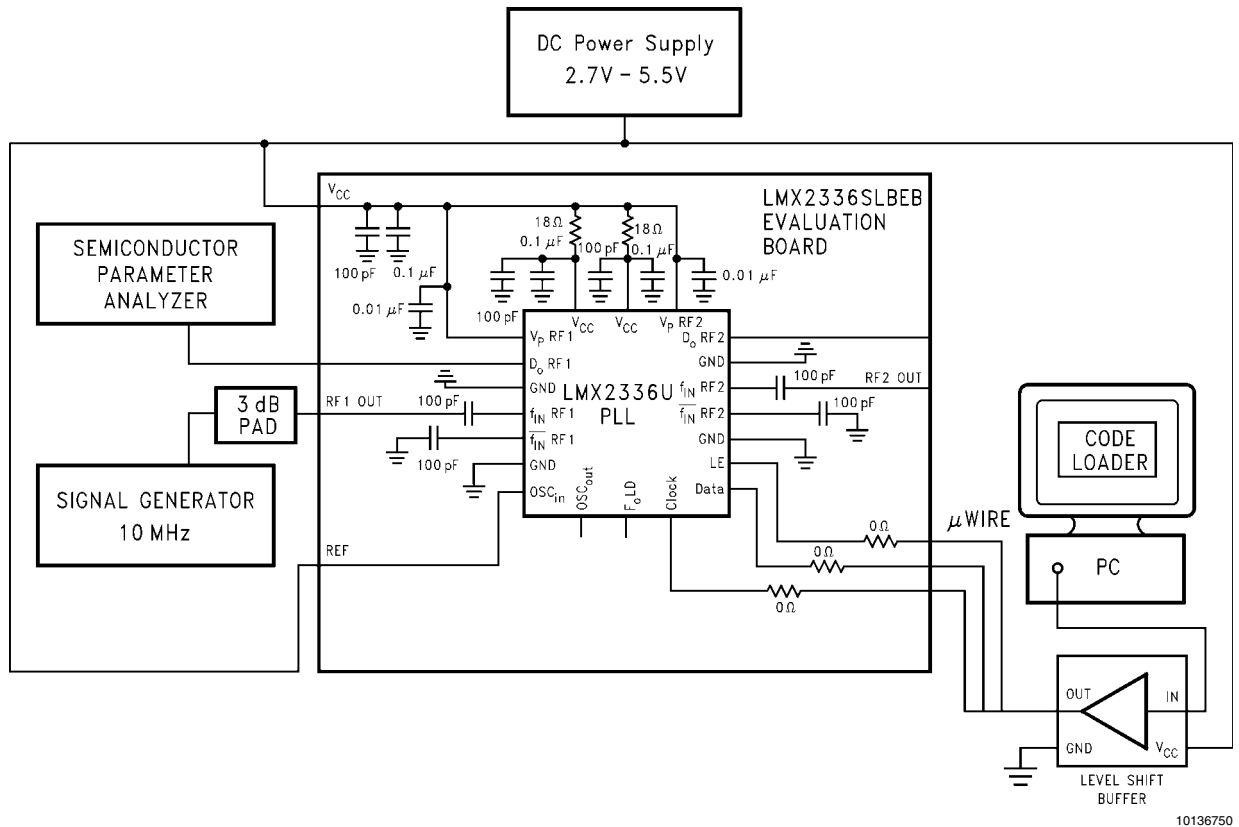
$$ID_o \text{ Vs } T_A = \frac{|I_2|_{T_A} - |I_2|_{T_A=25^\circ\text{C}}}{|I_2|_{T_A=25^\circ\text{C}}} \times 100\%$$

$$= \frac{|I_5|_{T_A} - |I_5|_{T_A=25^\circ\text{C}}}{|I_5|_{T_A=25^\circ\text{C}}} \times 100\%$$

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## Test Setups

LMX2335U and LMX2336U Charge Pump Test Setup



The block diagram above illustrates the setup required to measure the LMX2336U device's RF1 charge pump sink current. The same setup is used for the LMX2336TMEB/LMX2336SLEEB Evaluation Boards. The RF2 charge pump measurement setup is similar to the RF1 charge pump measurement setup. The purpose of this test is to assess the functionality of the RF1 charge pump.

This setup uses an open loop configuration. A power supply is connected to  $V_{CC}$  and swept from 2.7V to 5.5V. By means of a signal generator, a 10 MHz signal is typically applied to the  $f_{IN}$  RF1 pin. The signal is one of two inputs to the phase detector. The 3 dB pad provides a 50  $\Omega$  match between the PLL and the signal generator. The  $OSC_{in}$  pin is tied to  $V_{CC}$ . This establishes the other input to the phase detector. Alternatively, this input can be tied directly to the ground plane. With the  $D_O$  RF1 pin connected to a Semiconductor Parameter Analyzer in this way, the sink, source, and TRI-STATE currents can be measured by simply toggling the **Phase Detector Polarity** and **Charge Pump State** states in Code Loader. Similarly, the LOW and HIGH currents can be measured by switching the **Charge Pump Gain's** state between **1X** and **4X** in Code Loader.

Let  $F_r$  represent the frequency of the signal applied to the  $OSC_{in}$  pin, which is simply zero in this case (DC), and let  $F_p$  represent the frequency of the signal applied to the  $f_{IN}$  RF1 pin. The phase detector is sensitive to the rising edges of  $F_r$  and  $F_p$ . Assuming positive VCO characteristics; the charge pump turns ON and sinks current when the first rising edge of  $F_p$  is detected. Since  $F_r$  has no rising edge, the charge pump continues to sink current indefinitely.

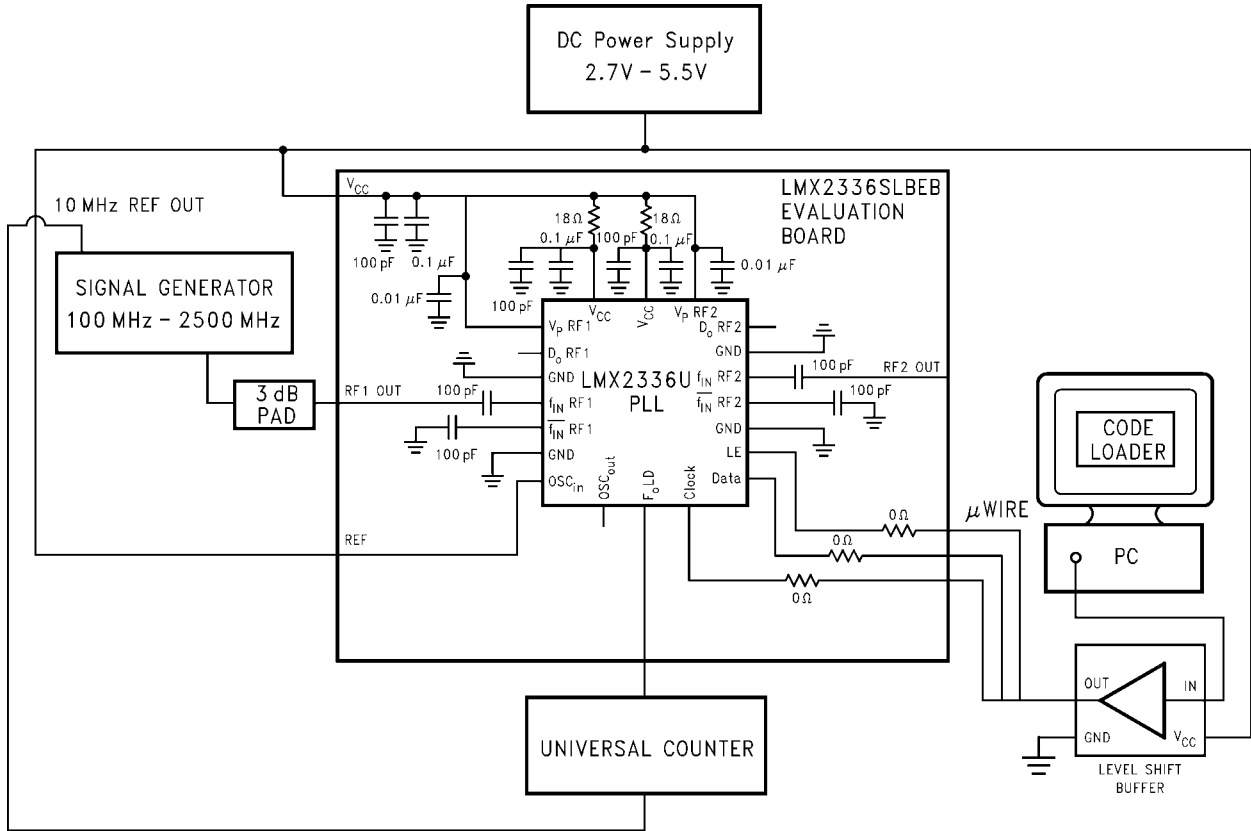
Toggling the **Phase Detector Polarity** state to negative VCO characteristics allows the measurement of the RF1 charge pump source current. Likewise, selecting **TRI-STATE** (TRI-STATE  $ID_O$  RF1 Bit = 1) for **Charge Pump State** in Code Loader facilitates the measurement of the TRI-STATE current.

The measurements are repeated at different temperatures, namely  $T_A = -40^\circ\text{C}$ ,  $+25^\circ\text{C}$ , and  $+85^\circ\text{C}$ .

The LMX2335U charge pump test setup is very much similar to the above test setup.

# Test Setups (Continued)

LMX2335U and LMX2336U  $f_{IN}$  Sensitivity Test Setup



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The block diagram above illustrates the setup required to measure the LMX2336U device's RF1 input sensitivity level. The same setup is used for the LMX2336TMEB/LMX2336SLEEB Evaluation Boards. The RF2 input sensitivity test setup is similar to the RF1 sensitivity test setup. The purpose of this test is to measure the acceptable signal level to the  $f_{IN}$  RF1 input of the PLL chip. Outside the acceptable signal range, the feedback divider begins to divide incorrectly and miscount the frequency.

The setup uses an open loop configuration. A power supply is connected to  $V_{CC}$  and the bias voltage is swept from 2.7V to 5.5V. The RF2 PLL is powered down (PWDN RF2 Bit = 1). By means of a signal generator, an RF signal is applied to the  $f_{IN}$  RF1 pin. The 3 dB pad provides a 50  $\Omega$  match between the PLL and the signal generator. The  $OSC_{in}$  pin is tied to  $V_{CC}$ . The N value is typically set to 10000 in Code Loader, i.e. RF1 N\_CNTRB Word = 156 and RF1 N\_CNTRA Word = 16 for PRE RF1 Bit = 0. The feedback divider output is routed to the  $F_0LD$  pin by selecting the **RF1 PLL N Divider Output** word ( $F_0LD$  Word = 6 or 14) in Code Loader. A Universal Counter is connected to the  $F_0LD$  pin and tied to

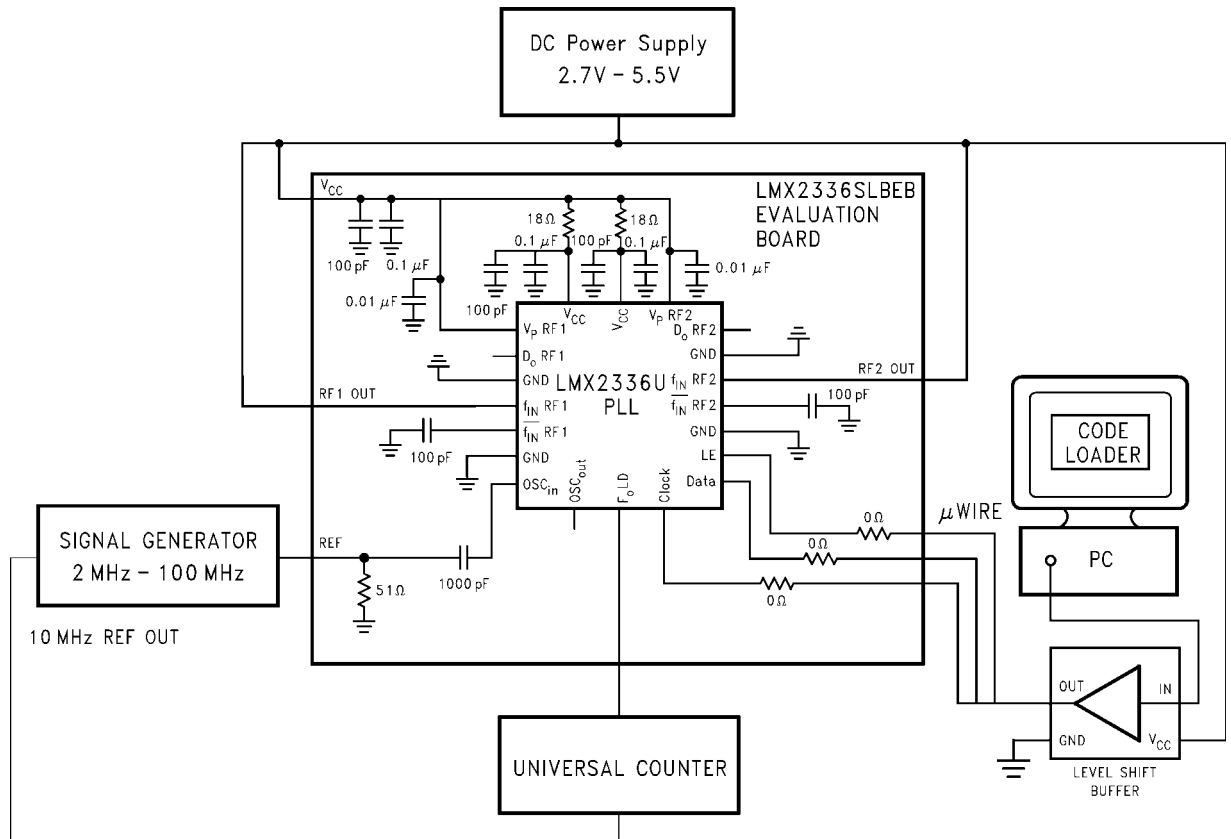
the 10 MHz reference output of the signal generator. The output of the feedback divider is thus monitored and should be equal to  $f_{IN} RF1 / N$ .

The  $f_{IN}$  RF1 input frequency and power level are then swept with the signal generator. The measurements are repeated at different temperatures, namely  $T_A = -40^\circ C$ ,  $+25^\circ C$ , and  $+85^\circ C$ . Sensitivity is reached when the frequency error of the divided RF input is greater than or equal to 1 Hz. The power attenuation from the cable and the 3 dB pad must be accounted for. The feedback divider will actually miscount if too much or too little power is applied to the  $f_{IN}$  RF1 input. Therefore, the allowed input power level will be bounded by the upper and lower sensitivity limits. In a typical application, if the power level to the  $f_{IN}$  RF1 input approaches the sensitivity limits, this can introduce spurs and degradation in phase noise. When the power level gets even closer to these limits, or exceeds it, then the RF1 PLL loses lock.

The LMX2335U  $f_{IN}$  sensitivity test setup is very much similar to the above test setup.

## Test Setups (Continued)

### LMX2335U and LMX2336U OSC<sub>in</sub> Sensitivity Test Setup



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The block diagram above illustrates the setup required to measure the LMX2336U device's OSC<sub>in</sub> buffer sensitivity level. The same setup is used for the LMX2336TMEB/ LMX2336SLEEB Evaluation Boards. This setup is similar to the  $f_{IN}$  sensitivity setup except that the signal generator is now connected to the OSC<sub>in</sub> pin and both  $f_{IN}$  pins are tied to  $V_{CC}$ . The 51  $\Omega$  shunt resistor matches the OSC<sub>in</sub> input to the signal generator. The R counter is typically set to 1000, i.e. RF1 R\_CNTR Word = 1000 or RF2 R\_CNTR Word = 1000. The reference divider output is routed to the F<sub>0</sub>LD pin by selecting the **RF1 PLL R Divider Output** word (F<sub>0</sub>LD Word = 2 or 10) or the **RF2 PLL R Divider Output** word (F<sub>0</sub>LD Word = 1 or 9) in Code Loader. Similarly, a Universal

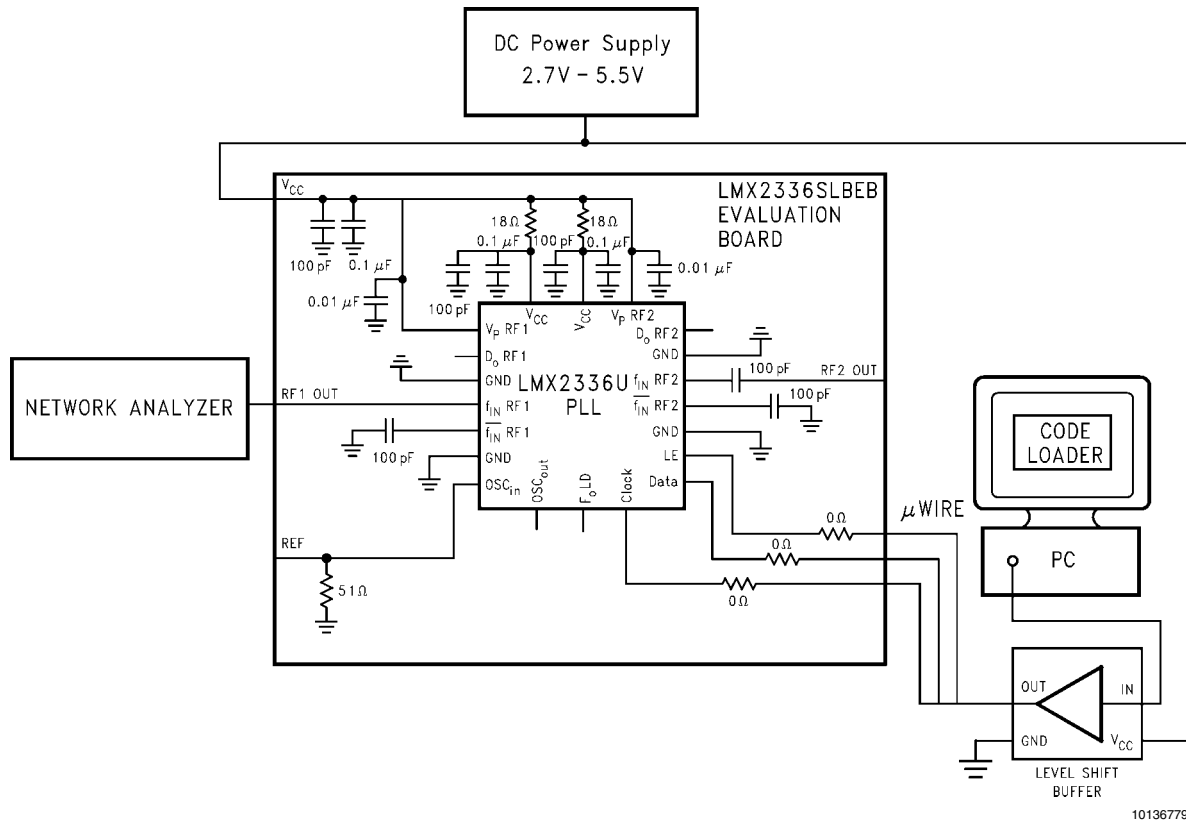
Counter is connected to the F<sub>0</sub>LD pin and is tied to the 10 MHz reference output from the signal generator. The output of the reference divider is monitored and should be equal to OSC<sub>in</sub>/ RF1 R\_CNTR or OSC<sub>in</sub>/ RF2 R\_CNTR.

Again,  $V_{CC}$  is swept from 2.7V to 5.5V. The OSC<sub>in</sub> input frequency and voltage level are then swept with the signal generator. The measurements are repeated at different temperatures, namely  $T_A = -40^\circ\text{C}$ ,  $+25^\circ\text{C}$ , and  $+85^\circ\text{C}$ . Sensitivity is reached when the frequency error of the divided input signal is greater than or equal to 1 Hz.

The LMX2335U OSC<sub>in</sub> sensitivity test setup is very much similar to the above test setup.

## Test Setups (Continued)

### LMX2335U and LMX2336U $f_{IN}$ Impedance Test Setup



The block diagram above illustrates the setup required to measure the LMX2336U device's RF1 input impedance. The RF2 input impedance and reference oscillator impedance setups are very much similar. The same setup is used for a LMX2336TMEB Evaluation Board. Measuring the device's input impedance facilitates the design of appropriate matching networks to match the PLL to the VCO, or in more critical situations, to the characteristic impedance of the printed circuit board (PCB) trace, to prevent undesired transmission line effects.

Before the actual measurements are taken, the Network Analyzer needs to be calibrated, i.e. the error coefficients need to be calculated. Therefore, three standards will be used to calculate these coefficients: an **open**, **short** and a **matched load**. A 1-port calibration is implemented here.

To calculate the coefficients, the PLL chip is first removed from the PCB. The Network Analyzer port is then connected to the RF1 OUT connector of the evaluation board and the desired operating frequency is set. The typical frequency range selected for the LMX2336U device's RF1 synthesizer is from 100 MHz to 2000 MHz. The standards will be located down the length of the RF1 OUT transmission line. The transmission line adds electrical length and acts as an offset from the reference plane of the Network Analyzer; therefore, it must be included in the calibration. Although not shown, 0  $\Omega$  resistors are used to complete the RF1 OUT transmission line (trace).

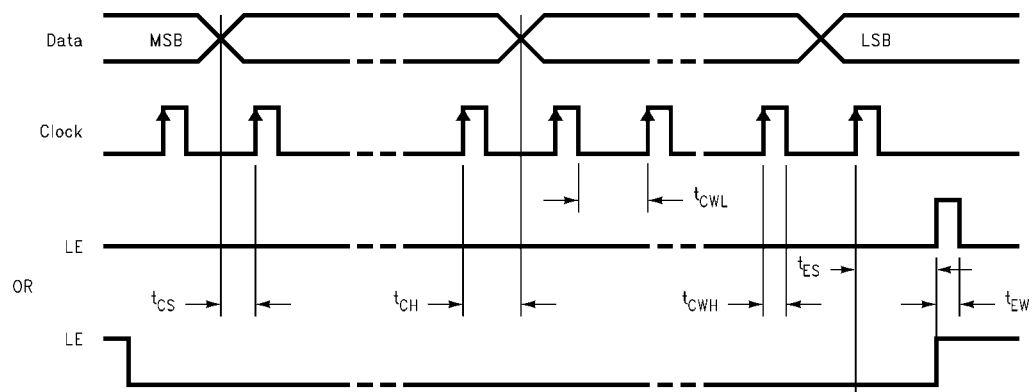
To implement an **open** standard, the end of the RF1 OUT trace is simply left open. To implement a **short** standard, a 0  $\Omega$  resistor is placed at the end of the RF1 OUT transmission line. Last of all, to implement a **matched load** standard, two 100  $\Omega$  resistors in parallel are placed at the end of the RF1 OUT transmission line. The Network Analyzer calculates the calibration coefficients based on the measured  $S_{11}$  parameters. With this all done, calibration is now complete.

The PLL chip is then placed on the PCB. A power supply is connected to  $V_{CC}$  and the bias voltage is swept from 2.7V to 5.5V. The OSC<sub>in</sub> pin is tied to the ground plane. Alternatively, the OSC<sub>in</sub> pin can be tied to  $V_{CC}$ . In this setup, the complementary input ( $\overline{f_{IN}}$  RF1) is AC coupled to ground. With the Network Analyzer still connected to RF1 OUT, the measured  $f_{IN}$  RF1 impedance is displayed.

**Note:** The impedance of the reference oscillator is measured when the oscillator buffer is powered up (PWDN RF1 Bit = 0 **or** PWDN RF2 Bit = 0), and when the oscillator buffer is powered down (PWDN RF1 Bit = 1 **and** PWDN RF2 Bit = 1).

The LMX2335U  $f_{IN}$  impedance test setup is very much similar to the above test setup. Note that there are no complementary inputs in the LMX2335U device.

## LMX2335U and LMX2336U Serial Data Input Timing



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### Notes:

1. Data is clocked into the 22-bit shift register on the rising edge of Clock
2. The MSB of Data is shifted in first.



## 1.0 Functional Description

The basic phase-lock-loop (PLL) configuration consists of a high-stability crystal reference oscillator, a frequency synthesizer such as the National Semiconductor LMX2335U or LMX2336U, a voltage controlled oscillator (VCO), and a passive loop filter. The frequency synthesizer includes a phase detector, current mode charge pump, programmable reference R and feedback N frequency dividers. The VCO frequency is established by dividing the crystal reference signal down via the reference divider to obtain a comparison reference frequency. This reference signal,  $F_r$ , is then presented to the input of a phase/frequency detector and compared with the feedback signal,  $F_p$ , which was obtained by dividing the VCO frequency down by way of the feedback divider. The phase/frequency detector measures the phase error between the  $F_r$  and  $F_p$  signals and outputs control signals that are directly proportional to the phase error. The charge pump then pumps charge into or out of the loop filter based on the magnitude and direction of the phase error. The loop filter converts the charge into a stable control voltage for the VCO. The phase/frequency detector's function is to adjust the voltage presented to the VCO until the feedback signal's frequency and phase match that of the reference signal. When this "Phase-Locked" condition exists, the VCO frequency will be N times that of the comparison frequency, where N is the feedback divider ratio.

### 1.1 REFERENCE OSCILLATOR INPUT

The reference oscillator frequency for both the RF1 and RF2 PLLs is provided from an external reference via the  $OSC_{in}$  pin. The reference buffer circuit supports input frequencies from 5 to 40 MHz with a minimum input sensitivity of 0.5  $V_{PP}$ . The reference buffer circuit has an approximate  $V_{CC}/2$  input threshold and can be driven from an external CMOS or TTL logic gate. Typically, the  $OSC_{in}$  pin is connected to the output of a crystal oscillator.

### 1.2 REFERENCE DIVIDERS (R COUNTERS)

The reference dividers divide the reference input signal,  $OSC_{in}$ , by a factor of R. The output of the reference divider circuits feeds the reference input of the phase detector. This reference input to the phase detector is often referred to as the comparison frequency. The divide ratio should be chosen such that the maximum phase comparison frequency ( $F_{\phi RF1}$  or  $F_{\phi RF2}$ ) of 10 MHz is not exceeded.

The RF1 and RF2 reference dividers are each comprised of 15-bit CMOS binary counters that support a continuous integer divide ratio from 3 to 32767. The RF1 and RF2 reference divider circuits are clocked by the output of the reference buffer circuit which is common to both.

### 1.3 PRESCALERS

The  $f_{IN}$  RF1 ( $f_{IN}$  RF2) and  $\overline{f_{IN}}$  RF1 ( $\overline{f_{IN}}$  RF2) input pins of the LMX2336U device drives the input of a bipolar, differential-pair amplifier. The output of the bipolar, differential-pair amplifier drives a chain of ECL D-type flip-flops in a dual modu-

lus configuration. The output of the prescaler is used to clock the subsequent feedback dividers. The complementary inputs of both the RF1 and RF2 synthesizers can be driven differentially, or the negative input can be AC coupled to ground through an external capacitor for single ended configuration. A 64/65 or a 128/129 prescale ratio can be selected for the both the RF1 and RF2 synthesizers. On the other hand, the LMX2335U PLL is only intended for single ended operation. Similarly, a 64/65 or a 128/129 prescale ratio can be selected for both the RF1 and RF2 synthesizers.

### 1.4 PROGRAMMABLE FEEDBACK DIVIDERS (N COUNTERS)

The programmable feedback dividers operate in concert with the prescalers to divide the input signal  $f_{IN}$  by a factor of N. The output of the programmable reference divider is provided to the feedback input of the phase detector circuit. The divide ratio should be chosen such that the maximum phase comparison frequency ( $F_{\phi RF1}$  or  $F_{\phi RF2}$ ) of 10 MHz is not exceeded.

The programmable feedback divider circuit is comprised of an A counter (swallow counter) and a B counter (programmable binary counter). The RF1 N\_CNTRA counter and RF2 N\_CNTRA counter are both 7-bit CMOS swallow counters, programmable from 0 to 127. The RF1 N\_CNTRB and RF2 N\_CNTRB counters are both 11-bit CMOS binary counters, programmable from 3 to 2047. A continuous integer divide ratio is achieved if  $N \geq P * (P-1)$ , where P is the value of the prescaler selected. Divide ratios less than the minimum continuous divide ratio are achievable as long as the binary programmable counter value is greater than the swallow counter value ( $N_{CNTRB} \geq N_{CNTRA}$ ). Refer to **Sections 2.5.1, 2.5.2, 2.7.1 and 2.7.2** for details on how to program the N\_CNTRA and N\_CNTRB counters. The following equations are useful in determining and programming a particular value of N:

$$N = (P \times N_{CNTRB}) + N_{CNTRA}$$

$$f_{IN} = N \times F_{\phi}$$

#### Definitions:

$F_{\phi}$ :	RF1 or RF2 phase detector comparison frequency
$f_{IN}$ :	RF1 or RF2 input frequency
N_CNTRA:	RF1 or RF2 A counter value
N_CNTRB:	RF1 or RF2 B counter value
P:	Preset modulus of the dual modulus prescaler
	LMX2335U RF1 synthesizer: P = 64 or 128
	LMX2336U RF1 synthesizer: P = 64 or 128
	LMX2335U RF2 synthesizer: P = 64 or 128
	LMX2336U RF2 synthesizer: P = 64 or 128

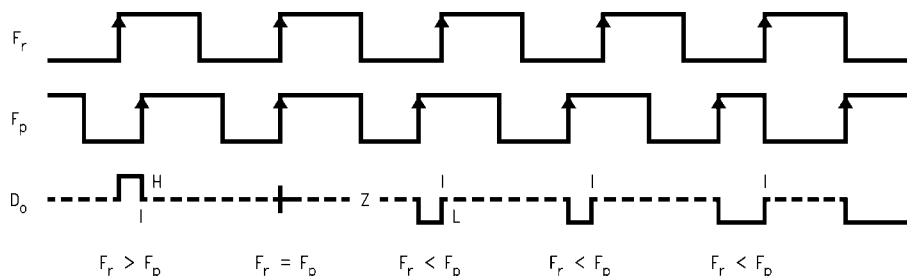
## 1.0 Functional Description (Continued)

### 1.5 PHASE/FREQUENCY DETECTORS

The RF1 and RF2 phase/frequency detectors are driven from their respective N and R counter outputs. The maximum frequency for both the RF1 and RF2 phase detector inputs is 10 MHz. The phase/frequency detector outputs control the respective charge pumps. The polarity of the pump-up or pump-down control signals are programmed using the **PD\_POL RF1** or **PD\_POL RF2** control bits, de-

pending on whether the RF1 or RF2 VCO characteristics are positive or negative. Refer to **Sections 2.4.2** and **2.6.2** for more details. The phase/frequency detectors have a detection range of  $-2\pi$  to  $+2\pi$ . The phase/frequency detectors also receive a feedback signal from the charge pump in order to eliminate dead zone.

#### PHASE COMPARATOR AND INTERNAL CHARGE PUMP CHARACTERISTICS



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#### Notes:

1. The minimum width of the pump-up and pump-down current pulses occur at the  $D_o$  RF1 or  $D_o$  RF2 pins when the loop is phase locked.
2. The diagram assumes positive VCO characteristics, i.e. **PD\_POL RF1** or **PD\_POL RF2** = 1.
3.  $F_r$  is the phase detector input from the reference divider (R counter).
4.  $F_p$  is the phase detector input from the programmable feedback divider (N counter).
5.  $D_o$  refers to either the RF1 or RF2 charge pump output.

### 1.6 CHARGE PUMPS

The charge pump directs charge into or out of an external loop filter. The loop filter converts the charge into a stable control voltage which is applied to the tuning input of the VCO. The charge pump steers the VCO control voltage towards  $V_P$  RF1 or  $V_P$  RF2 during pump-up events and towards GND during pump-down events. When locked,  $D_o$  RF1 or  $D_o$  RF2 are primarily in a TRI-STATE mode with small corrections occurring at the phase comparator rate. The charge pump output current magnitude can be selected by toggling the **ID\_o RF1** or **ID\_o RF2** control bits.

### 1.7 MICROWIRE SERIAL INTERFACE

The programmable register set is accessed via the MICROWIRE serial interface. The interface is comprised of three signal pins: Clock, Data and LE (Latch Enable). Serial data is clocked into the 22-bit shift register on the rising edge of Clock. The last two bits decode the internal control register address. When LE transitions HIGH, data stored in the shift register is loaded into one of four control registers depending on the state of the address bits. The MSB of Data is loaded in first. The synthesizers can be programmed even in power down mode. A complete programming description is provided in **Section 2.0 Programming Description**.

### 1.8 MULTI-FUNCTION OUTPUTS

The  $F_oLD$  output pin is a multi-function output that can be configured as the RF1 FastLock output, a push-pull analog lock detect output, counter reset, or used to monitor the output of the various reference divider (R counter) or feedback divider (N counter) circuits. The  $F_oLD$  control word is used to select the desired output function. When the PLL is in powerdown mode, the  $F_oLD$  output is pulled to a LOW state. A complete programming description of the multi-function output is provided in **Section 2.8  $F_oLD$** .

#### 1.8.1 Push-Pull Analog Lock Detect Output

An analog lock detect status generated from the phase detector is available on the  $F_oLD$  output pin if selected. The lock detect output goes HIGH when the charge pump is inactive. It goes LOW when the charge pump is active during a comparison cycle. When viewed with an oscilloscope, narrow negative pulses are observed when the charge pump turns on. The lock detect output signal is a push-pull configuration.

Three separate lock detect signals are routed to the multiplexer. Two of these monitor the 'lock' status of the individual synthesizers. The third detects the condition when both the RF1 and RF2 synthesizers are in a 'locked state'. External circuitry however, is required to provide a steady DC signal to indicate when the PLL is in a locked state. Refer to **Section 2.8  $F_oLD$**  for details on how to program the different lock detect options.

# 1.0 Functional Description (Continued)

## 1.8.2 Open Drain FastLock Output

The LMX233xU Fastlock feature allows faster loop response time during lock acquisition. The loop response time (lock time) can be approximately halved if the loop bandwidth is doubled. In order to achieve this, the same gain/ phase relationship at twice the loop bandwidth must be maintained. This can be achieved by increasing the charge pump current from 0.95 mA ( $ID_0$  RF1 Bit = 0) in the steady state mode, to 3.8 mA ( $ID_0$  RF1 Bit = 1) in Fastlock. When the  $F_{oLD}$  output is configured as a FastLock output, an open drain device is enabled. The open drain device switches in a parallel resistor  $R2'$  to ground, of equal value to resistor  $R2$  of the external loop filter. The loop bandwidth is effectively doubled and stability is maintained. Once locked to the correct frequency, the PLL will return to a steady state condition. Refer to **Section 2.8  $F_{oLD}$**  for details on how to configure the  $F_{oLD}$  output to an open drain Fastlock output.

## 1.8.3 Counter Reset

Three separate counter reset functions are provided. When the  $F_{oLD}$  is programmed to **Reset RF2 Counters**, both the RF2 feedback divider and the RF2 reference divider are held at their load point. When the **Reset RF1 Counters** is programmed, both the RF1 feedback divider and the RF1 reference divider are held at their load point. When the **Reset All Counters** mode is enabled, all feedback dividers and reference dividers are held at their load point. When the device is programmed to normal operation, both the feedback divider and reference divider are enabled and resume counting in 'close' alignment to each other. Refer to **Section 2.8  $F_{oLD}$**  for more details.

## 1.8.4 Reference Divider and Feedback Divider Output

The outputs of the various N and R dividers can be monitored by selecting the appropriate  $F_{oLD}$  word. This is essential when performing  $OSC_{in}$  or  $f_{IN}$  sensitivity measurements. Refer to the **Test Setups** section for more details. Refer to **Section 2.8  $F_{oLD}$**  for more details on how to route the appropriate divider output to the  $F_{oLD}$  pin.

## 1.9 POWER CONTROL

Each synthesizer in the LMX2335U or LMX2336U is individually power controlled by device powerdown bits. The powerdown word is comprised of the **PWDN RF1 (PWDN RF2)** bit, in conjunction with the **TRI-STATE  $ID_0$  RF1 (TRI-STATE  $ID_0$  RF2)** bit. The powerdown control word is used to set the operating mode of the device. Refer to **Sections 2.4.4, 2.5.4, 2.6.4, and 2.7.4** for details on how to program the RF1 or RF2 powerdown bits.

When either the RF1 synthesizer or the RF2 synthesizer enters the powerdown mode, the respective prescaler, phase detector, and charge pump circuit are disabled. The  $D_0$  RF1 ( $D_0$  RF2),  $f_{IN}$  RF1 ( $f_{IN}$  RF2), and  $\overline{f_{IN}}$  RF1 ( $\overline{f_{IN}}$  RF2) pins are all forced to a high impedance state. The reference divider and feedback divider circuits are held at the load point during powerdown. The oscillator buffer is disabled when both the RF1 and RF2 synthesizers are powered down. The  $OSC_{in}$  pin is forced to a HIGH state through an approximate 100 k $\Omega$  resistance when this condition exists. When either synthesizer is activated, the respective prescaler, phase detector, charge pump circuit, and the oscillator buffer are all powered up. The feedback divider, and the reference divider are held at load point. This allows the reference oscillator, feedback divider, reference divider and prescaler circuitry to reach proper bias levels. After a finite delay, the feedback and reference dividers are enabled and they resume counting in 'close' alignment (the maximum error is one prescaler cycle). The MICROWIRE control register remains active and capable of loading and latching data while in the powerdown mode.

### Synchronous Powerdown Mode

In this mode, the powerdown function is gated by the charge pump. When the device is configured for synchronous powerdown, the device will enter the powerdown mode upon completion of the next charge pump pulse event.

### Asynchronous Powerdown Mode

In this mode, the powerdown function is NOT gated by the completion of a charge pump pulse event. When the device is configured for asynchronous powerdown, the part will go into powerdown mode immediately.

TRI-STATE $ID_0$	PWDN	Operating Mode
0	0	PLL Active, Normal Operation
1	0	PLL Active, Charge Pump Output in High Impedance State
0	1	Synchronous Powerdown
1	1	Asynchronous Powerdown

#### Notes:

1. TRI-STATE  $ID_0$  refers to either the TRI-STATE  $ID_0$  RF1 or TRI-STATE  $ID_0$  RF2 bit .
2. PWDN refers to either the PWDN RF1 or PWDN RF2 bit.

## 2.0 Programming Description

### 2.1 MICROWIRE INTERFACE

The 22-bit shift register is loaded via the MICROWIRE interface. The shift register consists of a 20-bit *Data[19:0] Field* and a 2-bit *Address[1:0] Field* as shown below. The Address Field is used to decode the internal control register address. When LE transitions HIGH, data stored in the shift register is loaded into one of 4 control registers depending on the state of the address bits. The MSB of Data is loaded in first. The Data Field assignments are shown in **Section 2.3 CONTROL REGISTER CONTENT MAP**.

MSB										LSB	
Data[19:0]										Address[1:0]	
21									2 1	0	

### 2.2 CONTROL REGISTER LOCATION

The address bits Address[1:0] decode the internal register address. The table below shows how the address bits are mapped into the target control register.

Address[1:0] Field		Target Register
0	0	RF2 R
0	1	RF2 N
1	0	RF1 R
1	1	RF1 N

### 2.3 CONTROL REGISTER CONTENT MAP

The control register content map describes how the bits within each control register are allocated to specific control functions.

## 2.0 Programming Description (Continued)

Reg.	Most Significant Bit										SHIFT REGISTER BIT LOCATION														Least Significant Bit			
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
	Data Field																						Address Field					
RF2 R	F <sub>0</sub> LD0	F <sub>0</sub> LD2	TRI-STATE ID <sub>0</sub> RF2	ID <sub>0</sub> RF2	PD <sub>-</sub> POL RF2	RF2 R_CNTR[14:0]										0		0		0		0						
RF2 N	PWDN RF2	PRE RF2	RF2 N_CNTRB[10:0]										RF2 N_CNTRA[6:0]										0		1			
RF1 R	F <sub>0</sub> LD1	F <sub>0</sub> LD3	TRI-STATE ID <sub>0</sub> RF1	ID <sub>0</sub> RF1	PD <sub>-</sub> POL RF1	RF1 R_CNTR[14:0]										1		0		0		0						
RF1 N	PWDN RF1	PRE RF1	RF1 N_CNTRB[10:0]										RF1 N_CNTRA[6:0]										1		1			

## 2.0 Programming Description (Continued)

### 2.4 RF2 R REGISTER

The RF2 R register contains the RF2 R\_CNTR, PD\_POL RF2, ID<sub>o</sub> RF2, and TRI-STATE ID<sub>o</sub> RF2 control words, in addition to two bits that compose the F<sub>o</sub>LD control word. The detailed description and programming information for each control word is discussed in the following sections. RF2 R\_CNTR[14:0]

Reg.	SHIFT REGISTER BIT LOCATION																			Least Significant Bit		
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																				Address Field	
RF2 R	F <sub>0</sub> LD0	F <sub>0</sub> LD2	TRI-STATE ID <sub>0</sub> RF2	ID <sub>0</sub> RF2	PD_POL RF2	RF2 R_CNTR[14:0]															0	0

#### 2.4.1 RF2 R\_CNTR[14:0] RF2 SYNTHESIZER PROGRAMMABLE REFERENCE DIVIDER (R COUNTER) RF2 R[2:16]

The RF2 reference divider (RF2 R\_CNTR) can be programmed to support divide ratios from 3 to 32767. Divide ratios less than 3 are prohibited.

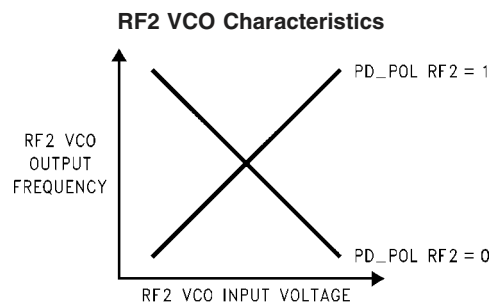
Divide Ratio	RF2 R_CNTR[14:0]														
	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

#### 2.4.2 PD\_POL RF2 RF2 SYNTHESIZER PHASE DETECTOR POLARITY

RF2 R[17]

The PD\_POL RF2 bit is used to control the RF2 synthesizer's phase detector polarity based on the VCO tuning characteristics.

Control Bit	Register Location	Description	Function	
			0	1
PD_POL RF2	RF2 R[17]	RF2 Phase Detector Polarity	RF2 VCO Negative Tuning Characteristics	RF2 VCO Positive Tuning Characteristics



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#### 2.4.3 ID<sub>o</sub> RF2 RF2 SYNTHESIZER CHARGE PUMP CURRENT GAIN

RF2 R[18]

The ID<sub>o</sub> RF2 bit controls the RF2 synthesizer's charge pump gain. Two current levels are available.

Control Bit	Register Location	Description	Function	
			0	1
ID <sub>o</sub> RF2	RF2 R[18]	RF2 Charge Pump Current Gain	LOW 0.95 mA	HIGH 3.80 mA

## 2.0 Programming Description (Continued)

### 2.4.4 TRI-STATE ID<sub>O</sub> RF2 RF2 SYNTHESIZER CHARGE PUMP TRI-STATE CURRENT

RF2 R[19]

The TRI-STATE ID<sub>O</sub> RF2 bit allows the charge pump to be switched between a normal operating mode and a high impedance output state. This happens asynchronously with the change in the TRI-STATE ID<sub>O</sub> RF2 bit.

Furthermore, the TRI-STATE ID<sub>O</sub> RF2 bit operates in conjunction with the PWDN RF2 bit to set a synchronous or an asynchronous powerdown mode.

Control Bit	Register Location	Description	Function	
			0	1
TRI-STATE ID <sub>O</sub> RF2	RF2 R[19]	RF2 Charge Pump TRI-STATE Current	RF2 Charge Pump Normal Operation	RF2 Charge Pump Output in High Impedance State

### 2.5 RF2 N REGISTER

The RF2 N register contains the RF2 N\_CNTRA, RF2 N\_CNTRB, PRE RF2, and PWDN RF2 control words. The RF2 N\_CNTRA and RF2 N\_CNTRB control words are used to setup the programmable feedback divider. The detailed description and programming information for each control word is discussed in the following sections.

Reg.	Most Significant Bit										SHIFT REGISTER BIT LOCATION										Least Significant Bit	
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																				Address Field	
RF2 N	PWDN RF2	PRE RF2	RF2 N_CNTRB[10:0]										RF2 N_CNTRA[6:0]								0	1

#### 2.5.1 RF2 N\_CNTRA[6:0] RF2 SYNTHESIZER SWALLOW COUNTER (A COUNTER)

RF2 N[2:8]

The RF2 N\_CNTRA control word is used to setup the RF2 synthesizer's A counter. The A counter is a 7-bit swallow counter used in the programmable feedback divider. The RF2 N\_CNTRA control word can be programmed to values ranging from 0 to 127.

Divide Ratio	RF2 N_CNTRA[6:0]						
	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

#### 2.5.2 RF2 N\_CNTRB[10:0] RF2 SYNTHESIZER PROGRAMMABLE BINARY COUNTER (B COUNTER)

RF2 N[9:19]

The RF2 N\_CNTRB control word is used to setup the RF2 synthesizer's B counter. The B counter is an 11-bit programmable binary counter used in the programmable feedback divider. The RF2 N\_CNTRB control word can be programmed to values ranging from 3 to 2047.

Divide Ratio	RF2 N_CNTRB[10:0]										
	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

#### 2.5.3 PRE RF2 RF2 SYNTHESIZER PRESCALER SELECT

RF2 N[20]

The RF2 synthesizer utilizes a selectable dual modulus prescaler.

Control Bit	Register Location	Description	Function	
			0	1
PRE RF2	RF2 N[20]	RF2 Prescaler Select	64/65 Prescaler Selected	128/129 Prescaler Selected

## 2.0 Programming Description (Continued)

### 2.5.4 PWDN RF2

### RF2 SYNTHESIZER POWERDOWN

RF2 N[21]

The PWDN RF2 bit is used to switch the RF2 PLL between a powered up and powered down mode.

Furthermore, the PWDN RF2 bit operates in conjunction with the TRI-STATE ID<sub>0</sub> RF2 bit to set a synchronous or an asynchronous powerdown mode.

Control Bit	Register Location	Description	Function	
			0	1
PWDN RF2	RF2 N[21]	RF2 Powerdown	RF2 PLL Active	RF2 PLL Powerdown

### 2.6 RF1 R REGISTER

The RF1 R register contains the RF1 R\_CNTR, PD\_POL RF1, ID<sub>0</sub> RF1, and TRI-STATE ID<sub>0</sub> RF1 control words, in addition to two bits that compose the F<sub>0</sub>LD control word. The detailed description and programming information for each control word is discussed in the following sections.

Reg.	SHIFT REGISTER BIT LOCATION																			Least Significant Bit		
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	<i>Data Field</i>																				<i>Address Field</i>	
RF1 R	F <sub>0</sub> LD1	F <sub>0</sub> LD3	TRI-STATE ID <sub>0</sub> RF1	ID <sub>0</sub> RF1	PD_ POL RF1	RF1 R_CNTR[14:0]															1	0

### 2.6.1 RF1 R\_CNTR[14:0] RF1 SYNTHESIZER PROGRAMMABLE REFERENCE DIVIDER (R COUNTER) RF1 R[2:16]

The RF1 reference divider (RF1 R\_CNTR) can be programmed to support divide ratios from 3 to 32767. Divide ratios less than 3 are prohibited.

Divide Ratio	RF1 R_CNTR[14:0]														
	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

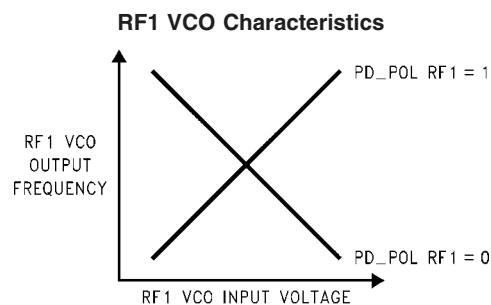
### 2.6.2 PD\_POL RF1

### RF1 SYNTHESIZER PHASE DETECTOR POLARITY

RF1 R[17]

The PD\_POL RF1 bit is used to control the RF1 synthesizer's phase detector polarity based on the VCO tuning characteristics.

Control Bit	Register Location	Description	Function	
			0	1
PD_POL RF1	RF1 R[17]	RF1 Phase Detector Polarity	RF1 VCO Negative Tuning Characteristics	RF1 VCO Positive Tuning Characteristics



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## 2.0 Programming Description (Continued)

### 2.6.3 ID<sub>0</sub> RF1

#### RF1 SYNTHESIZER CHARGE PUMP CURRENT GAIN

RF1 R[18]

The ID<sub>0</sub> RF1 bit controls the RF1 synthesizer's charge pump gain. Two current levels are available.

Control Bit	Register Location	Description	Function	
			0	1
ID <sub>0</sub> RF1	RF1 R[18]	RF1 Charge Pump Current Gain	LOW 0.95 mA	HIGH 3.80 mA

### 2.6.4 TRI-STATE ID<sub>0</sub> RF1

#### RF1 SYNTHESIZER CHARGE PUMP TRI-STATE CURRENT

RF1 R[19]

The TRI-STATE ID<sub>0</sub> RF1 bit allows the charge pump to be switched between a normal operating mode and a high impedance output state. This happens asynchronously with the change in the TRI-STATE ID<sub>0</sub> RF1 bit.

Furthermore, the TRI-STATE ID<sub>0</sub> RF1 bit operates in conjunction with the PWDN RF1 bit to set a synchronous or an asynchronous powerdown mode.

Control Bit	Register Location	Description	Function	
			0	1
TRI-STATE ID <sub>0</sub> RF1	RF1 R[19]	RF1 Charge Pump TRI-STATE Current	RF1 Charge Pump Normal Operation	RF1 Charge Pump Output in High Impedance State

### 2.7 RF1 N REGISTER

The RF1 N register contains the RF1 N\_CNTRA, RF1 N\_CNTRB, PRE RF1, and PWDN RF1 control words. The RF1 N\_CNTRA and RF1 N\_CNTRB control words are used to setup the programmable feedback divider. The detailed description and programming information for each control word is discussed in the following sections.

Reg.	SHIFT REGISTER BIT LOCATION																				Least Significant Bit	
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																				Address Field	
RF1 N	PWDN RF1	PRE RF1	RF1 N_CNTRB[10:0]											RF1 N_CNTRA[6:0]						1	1	

### 2.7.1 RF1 N\_CNTRA[6:0]

#### RF1 SYNTHESIZER SWALLOW COUNTER (A COUNTER)

RF1 N[2:8]

The RF1 N\_CNTRA control word is used to setup the RF1 synthesizer's A counter. The A counter is a 7-bit swallow counter used in the programmable feedback divider. The RF1 N\_CNTRA control word can be programmed to values ranging from 0 to 127.

Divide Ratio	RF1 N_CNTRA[6:0]						
	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

### 2.7.2 RF1 N\_CNTRB[10:0]

#### RF1 SYNTHESIZER PROGRAMMABLE BINARY COUNTER (B COUNTER)

RF1 N[9:19]

The RF1 N\_CNTRB control word is used to setup the RF1 synthesizer's B counter. The B counter is an 11-bit programmable binary counter used in the programmable feedback divider. The RF1 N\_CNTRB control word can be programmed to values ranging from 3 to 2047.

Divide Ratio	RF1 N_CNTRB[10:0]										
	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

## 2.0 Programming Description (Continued)

### 2.7.3 PRE RF1

#### RF1 SYNTHESIZER PRESCALER SELECT

RF1 N[20]

The RF1 synthesizer utilizes a selectable dual modulus prescaler.

Control Bit	Register Location	Description	Function	
			0	1
PRE RF1	RF1 N[20]	RF1 Prescaler Select	64/65 Prescaler Selected	128/129 Prescaler Selected

### 2.7.4 PWDN RF1

#### RF1 SYNTHESIZER POWERDOWN

RF1 N[21]

The PWDN RF1 bit is used to switch the RF1 PLL between a powered up and powered down mode.

Furthermore, the PWDN RF1 bit operates in conjunction with the TRI-STATE ID<sub>0</sub> RF1 bit to set a synchronous or an asynchronous powerdown mode.

Control Bit	Register Location	Description	Function	
			0	1
PWDN RF1	RF1 N[21]	RF1 Powerdown	RF1 PLL Active	RF1 PLL Powerdown

## 2.0 Programming Description (Continued)

### 2.8 F<sub>o</sub>LD[3:0]

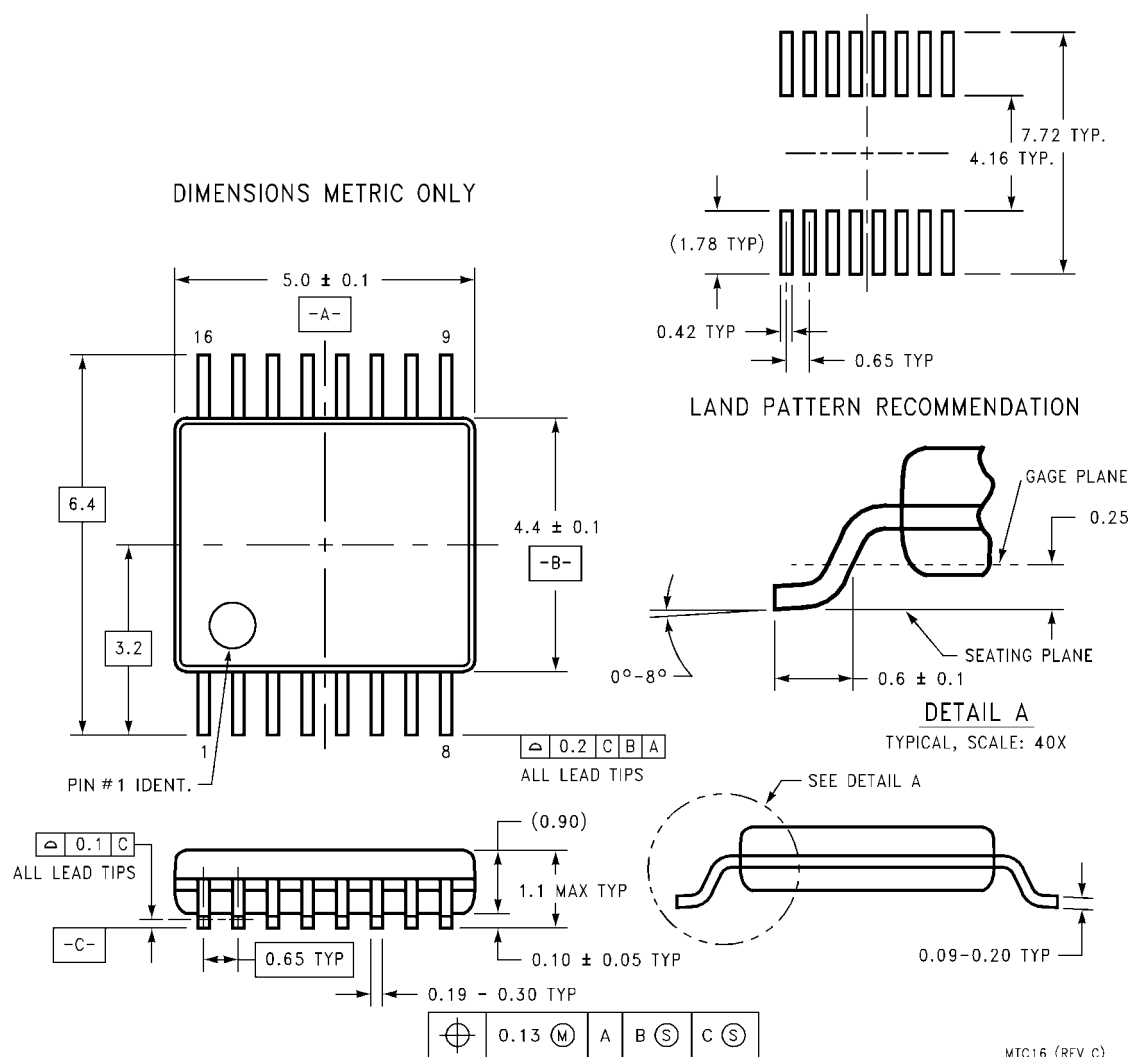
#### MULTI-FUNCTION OUTPUT SELECT

[RF1 R[20], RF2 R[20], RF1 R [21], RF2 R[21]]

The F<sub>o</sub>LD control word is used to select which signal is routed to the F<sub>o</sub>LD pin.

F <sub>o</sub> LD3	F <sub>o</sub> LD2	F <sub>o</sub> LD1	F <sub>o</sub> LD0	F <sub>o</sub> LD Output State
0	0	0	0	LOW Logic State Output
0	0	0	1	RF2 PLL R Divider Output, Push-Pull Output
0	0	1	0	RF1 PLL R Divider Output, Push-Pull Output
0	0	1	1	Open Drain Fastlock Output
0	1	0	0	RF2 PLL Analog Lock Detect, Push-Pull Output
0	1	0	1	RF2 PLL N Divider Output, Push-Pull Output
0	1	1	0	RF1 PLL N Divider Output, Push-Pull Output
0	1	1	1	Reset RF2 Counters, LOW Logic State Output
1	0	0	0	RF1 Analog Lock Detect, Push-Pull Output
1	0	0	1	RF2 PLL R Divider Output, Push-Pull Output
1	0	1	0	RF1 PLL R Divider Output, Push-Pull Output
1	0	1	1	Reset RF1 Counters, LOW Logic State Output
1	1	0	0	RF1 and RF2 Analog Lock Detect, Push-Pull Output
1	1	0	1	RF2 PLL N Divider Output, Push-Pull Output
1	1	1	0	RF1 PLL N Divider Output, Push-Pull Output
1	1	1	1	Reset All Counters, LOW Logic State Output

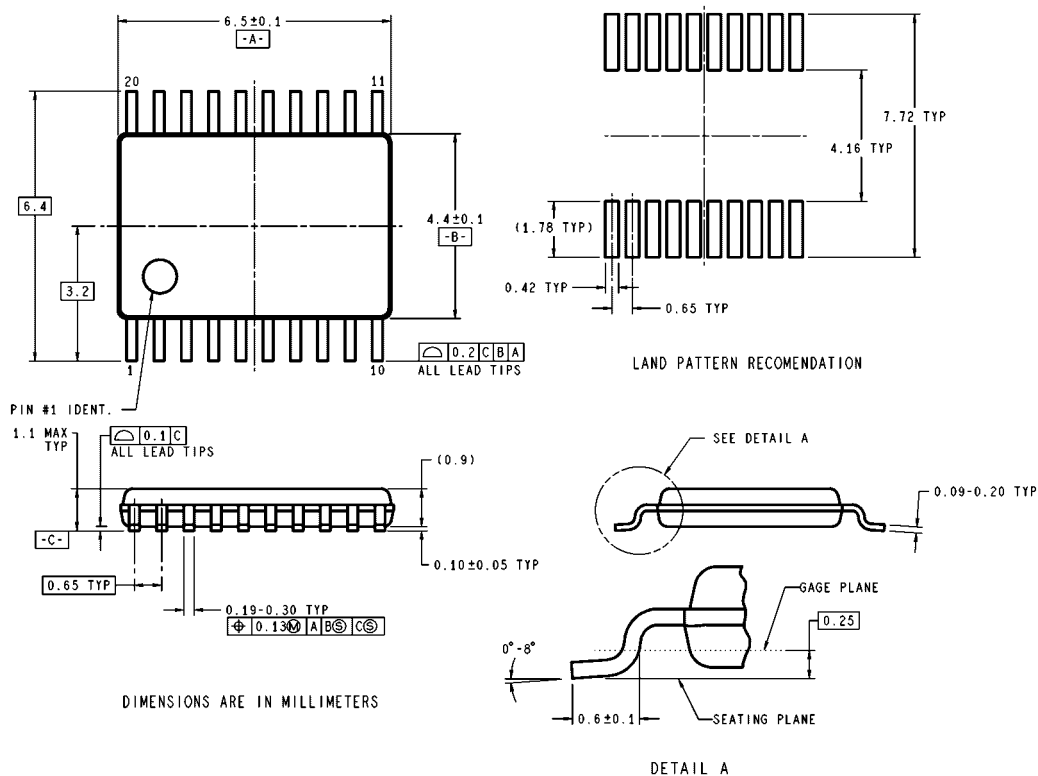
**Physical Dimensions** inches (millimeters)  
unless otherwise noted



**16-Pin Thin Shrink Small Outline Package (TM)**  
**NS Package Number MTC16**

MTC16 (REV C)

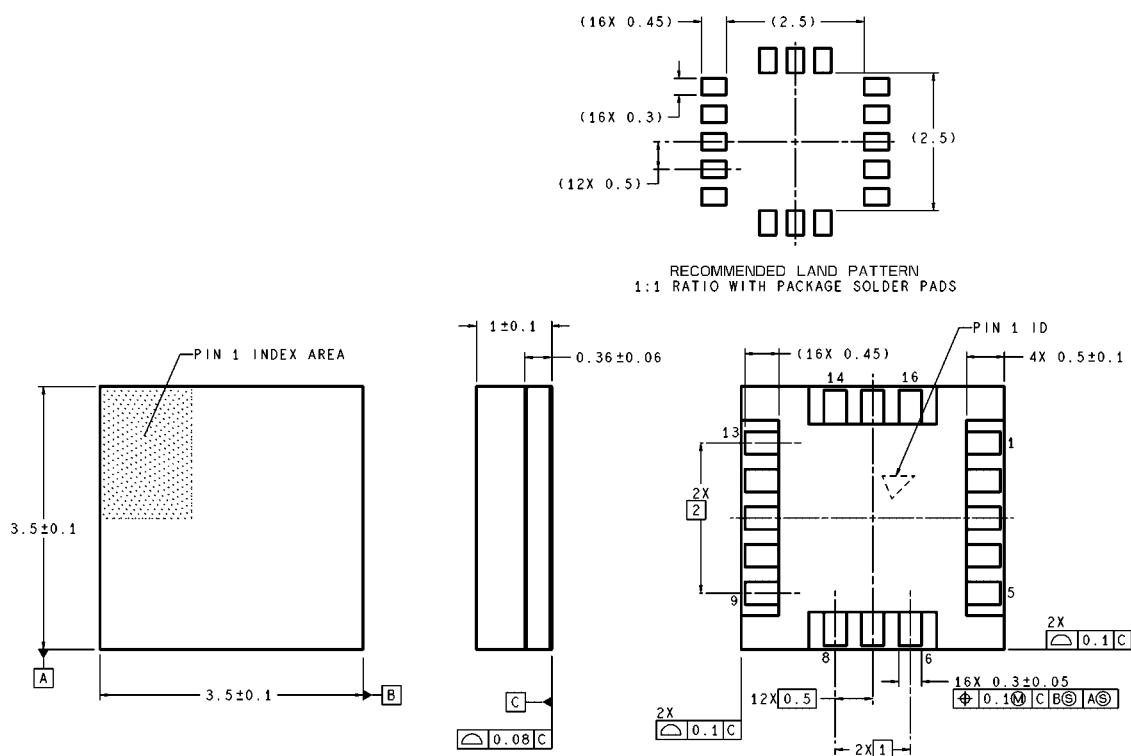
# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



MTC20 (Rev D)

**20-Pin Thin Shrink Small Outline Package (TM)**  
**NS Package Number MTC20**

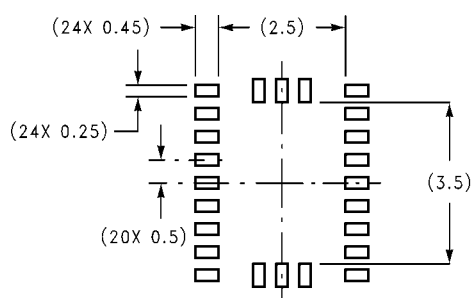
# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

SLB16A (Rev B)

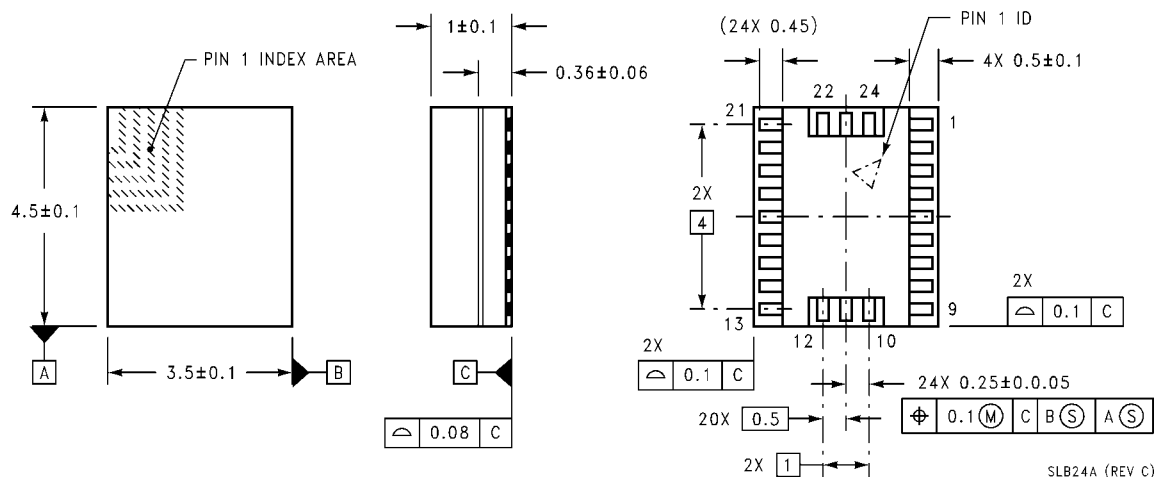
**16-Pin Chip Scale Package (SLB)**  
**NS Package Number SLB16A**



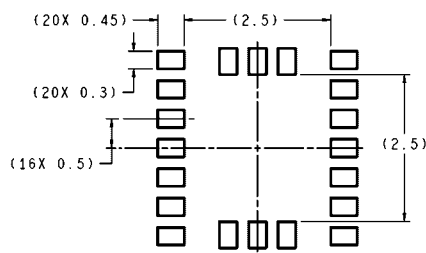
DIMENSIONS ARE IN MILLIMETERS

### RECOMMENDED LAND PATTERN

1:1 RATIO WITH PACKAGE SOLDER PADS

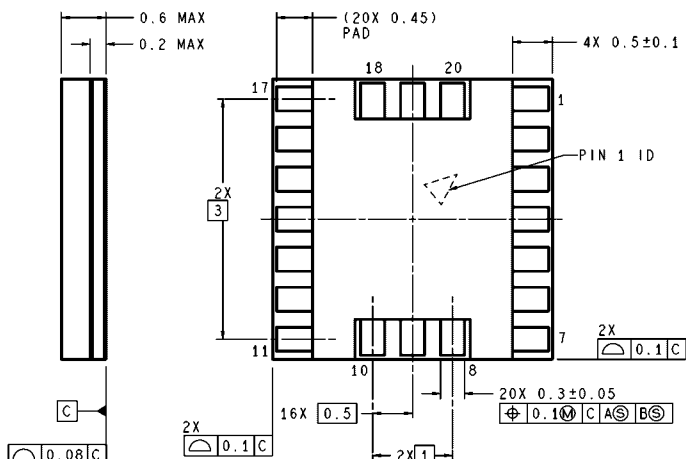
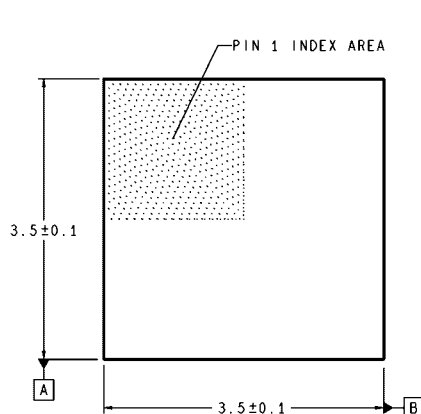


**24-Pin Chip Scale Package (SLB)**  
**NS Package Number SLB24A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

RECOMMENDED LAND PATTERN  
1:1 RATIO WITH PACKAGE SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS



SLE20A (Rev A)

**20-Pin Ultra Thin Chip Scale Package (SLE)**  
**NS Package Number SLE20A**

## LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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TABLE 3. *Continued*