National Semiconductor

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LMX2240
Intermediate Frequency Receiver

General Description

The LMX2240 is a monolithic, integrated intermediate frequency receiver suitable for use in Digital European Cordless Telecommunications (DECT) systems as well as other mobile telephony and wireless communications applications. It is fabricated using National's ABiC™ IV BiCMOS process (f_T = 15 GHz).

The LMX2240 consists of a high gain limiting amplifier, a frequency discriminator, and a received signal strength indicator (RSSI). The high gain limiting amplifier and discriminator operate in the 40 MHz to 150 MHz frequency range, and the limiter has approximately 70 dB of gain. The use of the limiter and the discriminator provides a low cost, high performance demodulator for communications systems. The RSSI output can be used for channel quality monitoring.

The LMX2240 is intended to support single conversion receivers. This device saves power, size, and cost by eliminating the second local oscillator (LO), second converter (mixer), and additional filters. The LMX2240 is recommended for systems with channel bandwidths of 300 kHz to 2.5 MHz.

The LMX2240 is available in a 16-pin JEDEC surface mount plastic package.

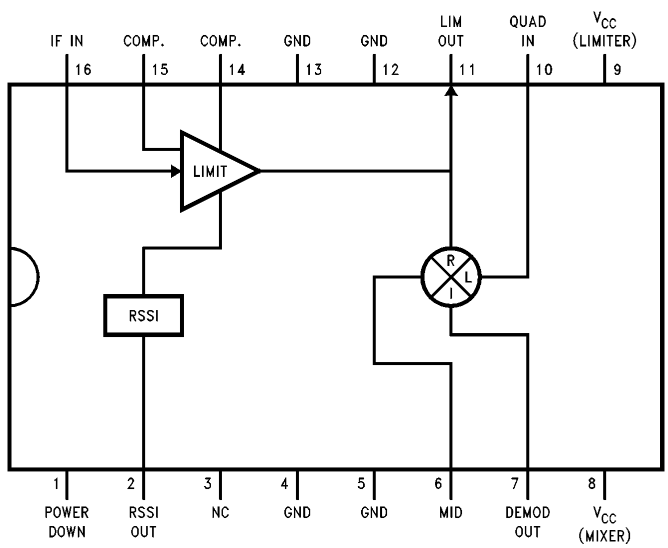
Features

- Typical operation at 110 MHz
- RF sensitivity to −75 dBm; RSSI sensitivity to −82 dBm
- High gain (70 dB) limiting amplifier
- Average current consumption: 480 μA for DECT handset (burst mode)
- +3V operation
- Power down mode for increased current savings
- Part of a complete receiver solution with the LMX2216 LNA/Mixer, the LMX2315/20 Phase-locked Loop, and the LMX2411 Baseband Processor
- Compliant to ARi1™ specification

Applications

- Digital European Cordless Telecommunications (DECT)
- Portable wireless communications (PCS/PCN, cordless)
- Wireless local area networks (WLANs)
- Digital cellular telephone systems
- Other wireless communications systems

Functional Block Diagram



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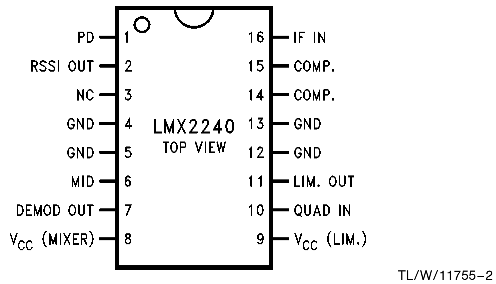
Connection Diagram

Small Outline Package



Top View
Order Number LMX2240M
See NS Package Number M16A

Pin Description

Pin No.	Pin Name	I/O	Description
1	PD	I	Power Down; a HIGH signal switches the part to power down mode.
2	RSSI Out	O	Voltage output of the received signal strength indicator (RSSI).
3	NC		No connection
4	GND		Ground
5	GND		Ground
6	MID	O	Mid-range output of the discriminator; can be used for comparator threshold.
7	Demod Out	O	Demodulated output of the discriminator.
8	V_{CC} (Mixer)		Source voltage for the mixer (discriminator).
9	V_{CC} (Lim.)		Source voltage for the limiter.
10	Quad In	I	Quadrature input. A DC path from source through an inductor must be present at this pin, but, there must be no series resistance (a parallel resistor to the inductor is acceptable).
11	Lim. Out	O	Limiter output to the quadrature tank.
12	GND		Ground
13	GND		Ground
14	Comp.		Compensation pin for the limiter. See Applications Information for capacitor value.
15	Comp.		Compensation pin for the limiter. See Applications Information for capacitor value.
16	IF In	I	IF input to the limiter.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage (V_{CC})	6.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Lead Temperature (T_L) (Soldering, 10 seconds)	+260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
3V	2.85	3.15	V
Operating Temperature (T_A)	−10	+70	°C

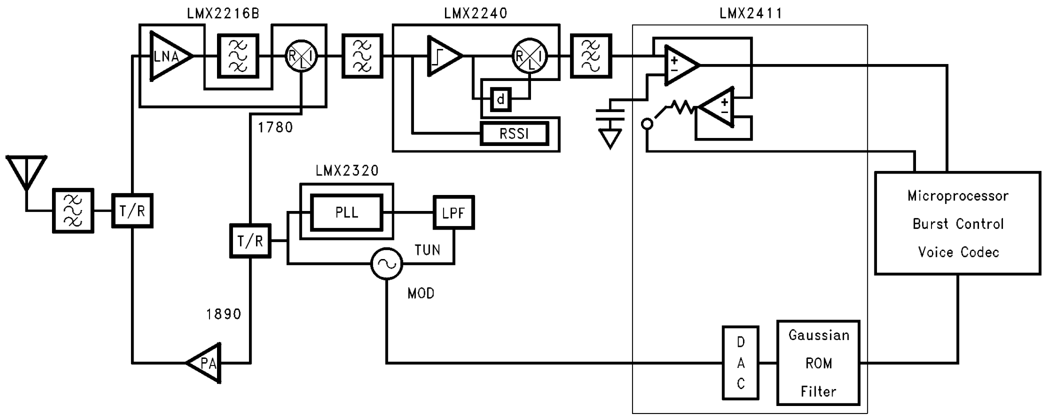
Electrical Characteristics

The following specifications apply for supply voltage V_{CC} = +3V ±5%, f_{IN} = 120 MHz, and T_A = 25°C unless otherwise specified

Symbol	Parameter	Conditions	Min	Value Typ	Max	Units
I_{DD}	Supply Current			8	10	mA
I_{PD}	Power Down Current			115	200	µA
f_{max}	Maximum IF Input Frequency		120	150		MHz
f_{min}	Minimum IF Input Frequency			10		MHz
IF LIMITER						
NF	IF Limiter Noise Figure			11.5	12.5	dB
A_V	Limiter Gain	Z_L = 1000Ω		70		dB
sens	Limiter/Disc. Sensitivity	BER = 0.001		−75		dBm
IF_{in}	IF Limiter Input Impedance		150		225	Ω
IF_{out}	IF Limiter Output Impedance			250		Ω
V_{max}	Maximum Input Voltage Level			500		mV_{PP}
V_{out}	Output Swing		350	500		V_{PP}
Lim	Input Limiting Point			−70		dBm
DISCRIMINATOR						
V_{out}	Discriminator Output Peak-to-Peak Voltage (Note 1)	See Test Circuit	1.0	1.2		V_{PP}
V_{OS}	Disc. Output DC Voltage (Pin 7)		1.4		1.7	V
MID	Mid-Range Output (Pin 6)		1.4		1.7	V
$DISC_{in}$	Disc. Input Impedance			1000		Ω
$DISC_{out}$	Disc. Output Impedance			150		Ω
RSSI						
RSSI	RSSI Dynamic Range			70		dB
$RSSI_{out}$	RSSI Output Voltage	Pin = −80 dBm	0.35	0.5	0.8	V
		Pin = 0 dBm	1.15	1.5	1.8	V
	RSSI Slope	Pin = −70 dBm to −20 dBm	11	16		mV/dB
	RSSI Linearity			3		dB

Note 1: The discriminator output peak-to-peak voltage is measured by operating the discriminator mixer with two separate inputs (i.e., as a mixer). A beat frequency of 1 kHz is generated, and this tone's output swing is guaranteed to be at least 1.0 V_{PP}. When the mixer is configured as a discriminator with the limiter and a tank circuit, the guaranteed 1.0 V_{PP} output translates to (1.0V *(36/180) =) 200 mV_{PP} demodulated output, assuming at least 36° phase shift across the band of interest from the tank circuit.

Typical Application Block Diagram



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Functional Description

OVERVIEW

The LMX2240 IF demodulator is a low power IF processor that includes a frequency discriminator, an IF hard limiting amplifier, and a received signal strength indicator (RSSI). The LMX2240 is capable of differentially demodulating an FM or AM signal with as high an IF as 150 MHz, avoiding a costly second down-conversion. The RSSI output can be used for time gated channel measurements required in TDMA and other systems. Other features include high receiver sensitivity and a power down mode to allow for standby operation.

THE LIMITING AMPLIFIER

The limiting amplifier has a typical gain of 70 dB and a sensitivity of about −75 dBm. This allows it to be used in the DECT system with 20 dB net RF gain in front of it to achieve a sensitivity of −95 dBm. The limiter is a five stage amplifier with internal compensation at each stage to ensure stability. Two external compensation capacitors are also required to further enhance stability. The input to the limiter is a relatively low impedance to allow easy matching to typical IF surface acoustic wave (SAW) filters. The output of the limiter is connected off chip to an external quadrature tank circuit as well as connected internally to the discriminator (mixer). The output impedance of the limiter is 250Ω (typical).

THE RECEIVED SIGNAL STRENGTH INDICATOR (RSSI)

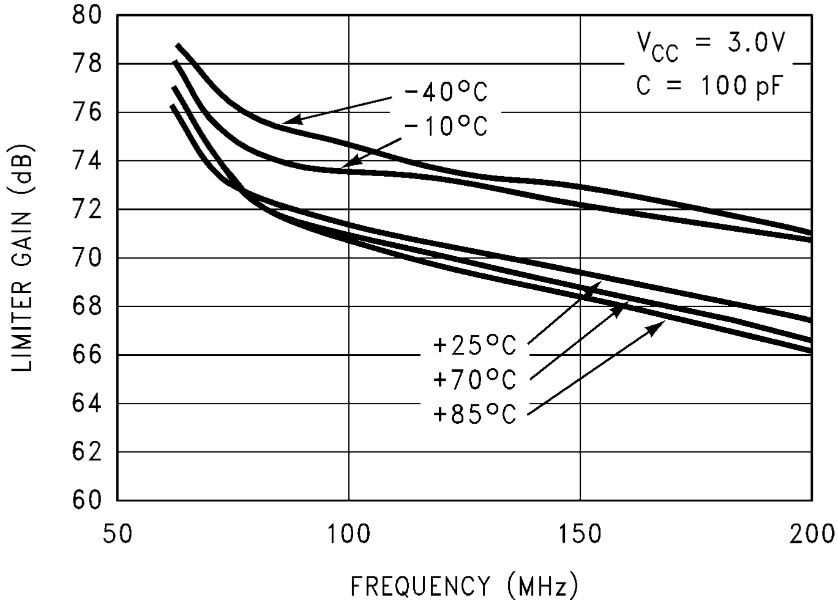
The RSSI circuit has a range of 70 dB. Its output voltage is proportional to the logarithm of the input signal level. The RSSI circuit has a sensitivity of −82 dBm. The output voltage of the circuit ranges from 0.5V to 1.5V typically.

THE FREQUENCY DISCRIMINATOR

The frequency discriminator is a Gilbert cell mixer that requires an external tank circuit to create a 90° phase shift at the desired frequency. The output of this circuit is centered at 1.5V by an internal level shifting circuit, and a mid-range voltage (at 1.5V) is also provided. The sensitivity of the discriminator to phase inaccuracies is 5.5 mV/degree (see Applications Information). This means that for a phase imbalance of 10°, the received eye diagram will be shifted by about 55 mV off of the 1.5V mid-range voltage. For the typical case, this amounts to about 10% of the output eye diagram (for 400 mV_{PP} output).

Typical Performance Characteristics

Limiter Gain vs Frequency with Temperature as a Parameter



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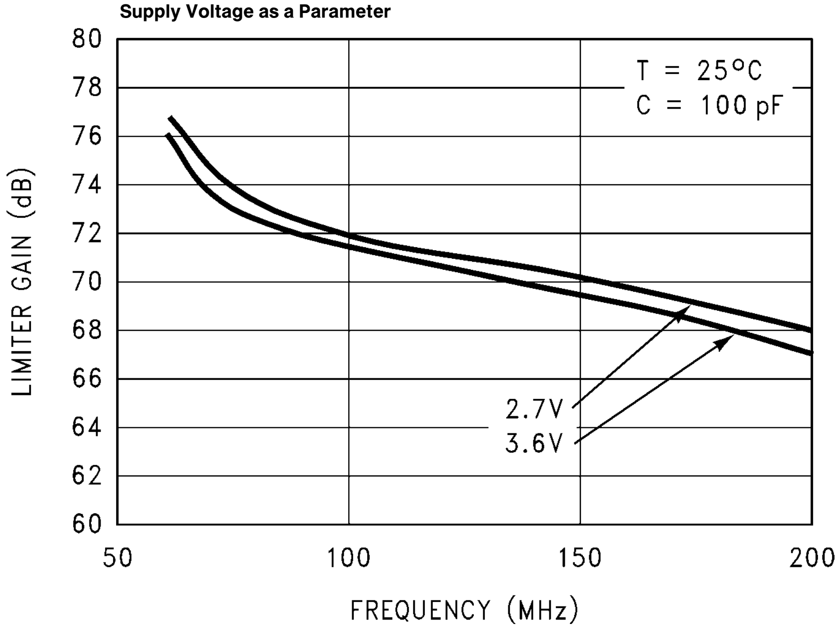
Limiter Gain vs Frequency with Supply Voltage as a Parameter



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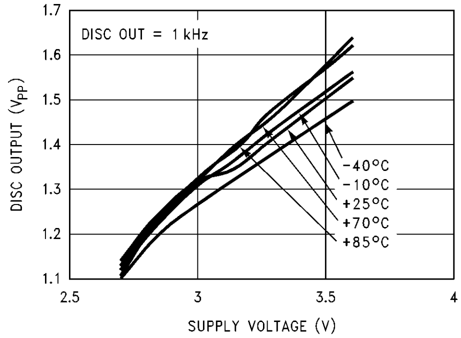
Typical Performance Characteristics (Continued)

Discriminator Output Peak-to-Peak Voltage vs Supply with Temperature as a Parameter



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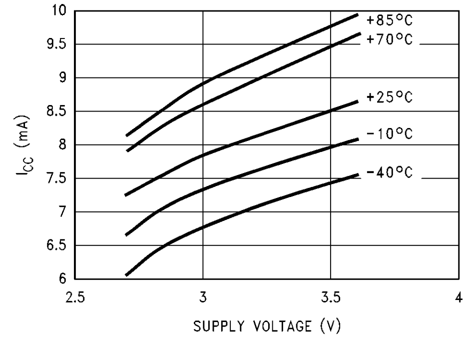
Current Consumption vs Supply Voltage with Temperature as a Parameter



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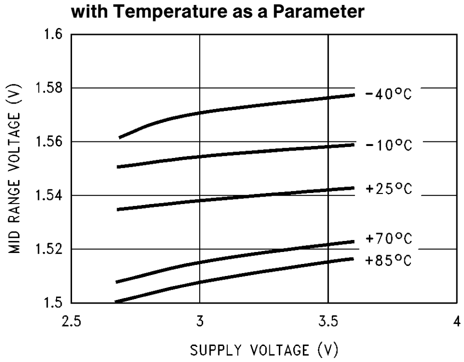
Mid-Range (Reference) Voltage vs Supply with Temperature as a Parameter



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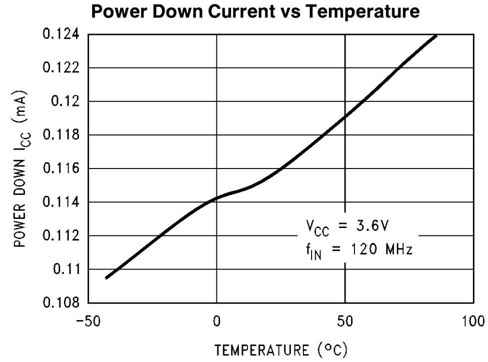
Power Down Current vs Temperature



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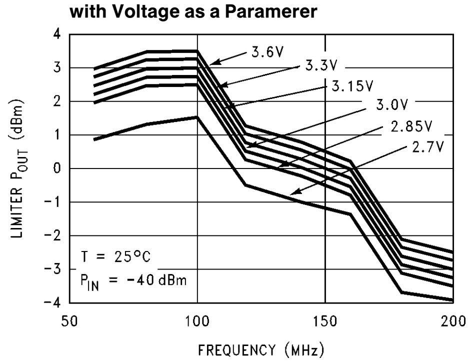
Limiter Output Power vs Frequency with Voltage as a Paramerer



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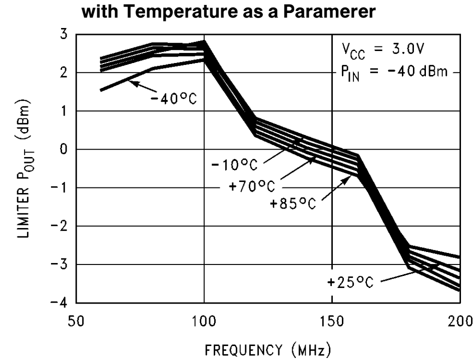
Limiter Output Power vs Frequency with Temperature as a Paramerer



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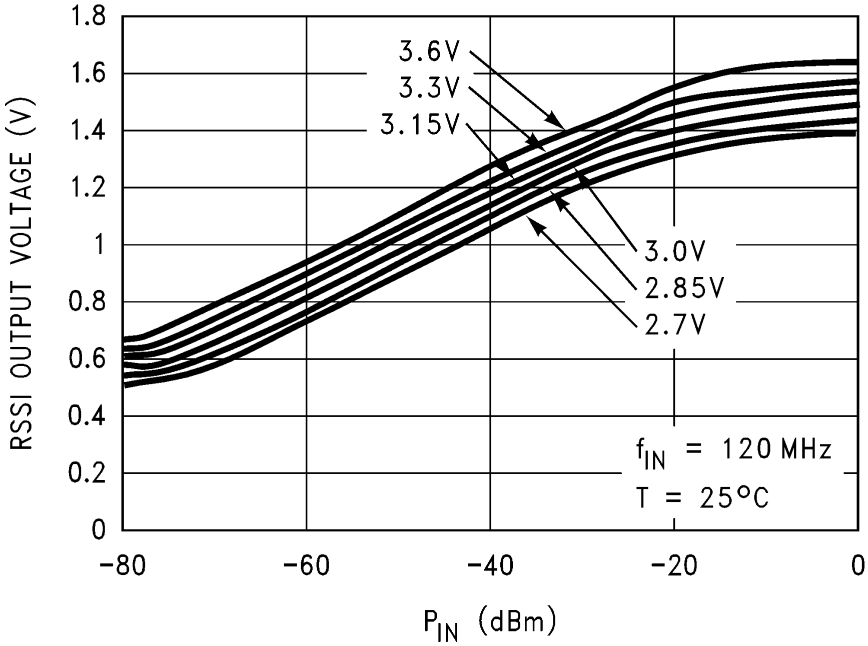
Typical Performance Characteristics (Continued)

RSSI Output vs Input Power with V_{CC} as a Parameter



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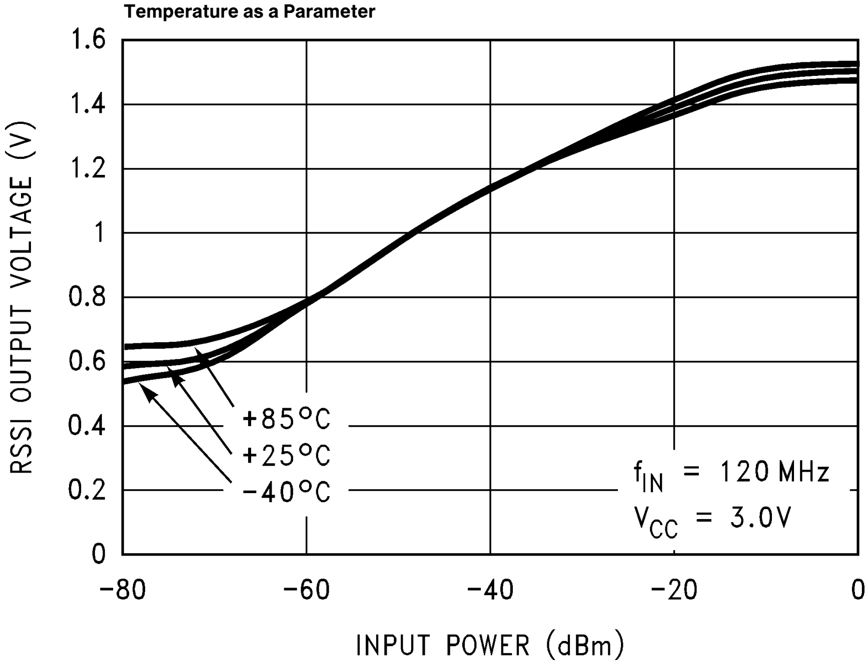
RSSI Output vs Input Power with Temperature as a Parameter



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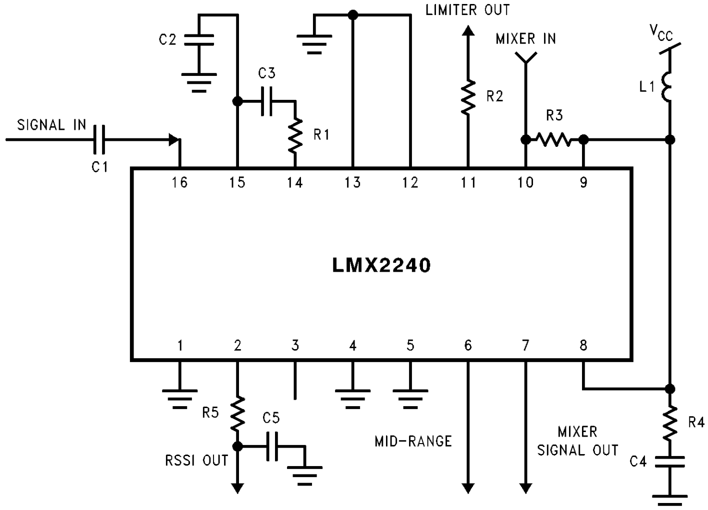
Automatic Test Circuit



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C1 = 1000 pF ±10% NPO Ceramic

C3 = 1000 pF ±10% NPO Ceramic

R2 = 1 kΩ ±5% ¼W Thin Film Carbon

L1 = 10 μH ±5% Air Coil

R4 = 20Ω ±5% ¼W Thin Film Carbon

R5 = 3.9 kΩ ±5% ¼W Thin Film Carbon

C2 = 1000 pF ±10% NPO Ceramic

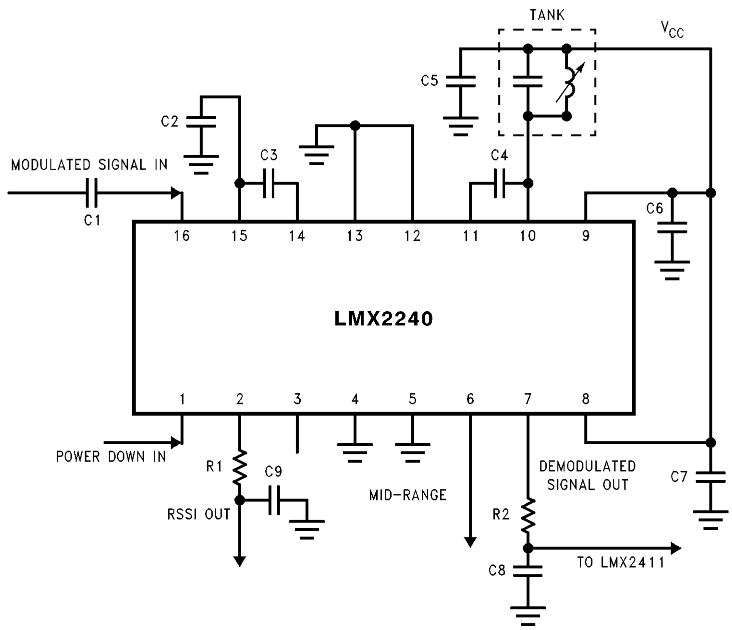
R1 = 25Ω ±5% ¼W Thin Film Carbon

R3 = 1 kΩ ±5% ¼W Thin Film Carbon

C4 = 1000 pF ±10% NPO Ceramic

C5 = 1000 pF ±10% NPO Ceramic

Typical Application Example



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C1 = C2 = C3 = C5 = C6 = 100 pF ±10% NPO Ceramic

C4 = 1 pF ±10% NPO Ceramic

C7 = C9 = 0.01 μF ±10% NPO Ceramic

C8 = 82 pF ±10% X7R Ceramic

R1 = 4 kΩ ±5% ¼W Thin Film Carbon

R2 = 880Ω ±5% ¼W Thin Film Carbon

Tank = Toko #638AH-0294

All supporting components 0603 surface mount except tank.

Applications Information

THE INTERMEDIATE FREQUENCY LIMITER

The IF limiter has a large amount of gain at high enough frequency to cause concern about oscillation. To ensure that the limiter does not oscillate, a few precautions should be taken. The compensation capacitors that are used should be chosen to roll off any unwanted frequencies below the band of interest. The capacitor should be a high Q, RF type ceramic chip capacitor. For DECT, the capacitor value should be 100 pF, and the capacitors should be soldered as close to the LMX2240 as possible. This will create a pass band from 40 MHz to 150 MHz. The AC coupling capacitor at the input to the limiter (from the SAW filter) should be the same value as the compensation capacitors.

THE DISCRIMINATOR

There are two types of discriminator that can be used to demodulate FM signals. The first is a delay line discriminator, which uses a delay in one path of the received signal to introduce a phase difference between it and the received signal. The operation of the delay line discriminator is derived in the inset box. The other type of discriminator relies on a quadrature tank to directly introduce a phase shift in the received signal. This is the type of implementation that is commonly used in mobile communications because of its relative ease of construction and low cost.

The discriminator operates best when the inputs to it are hard-limited (i.e., square edges). If the input signal is small enough such that the IF amplifier cannot limit it, the output voltage swing of the limiter will suffer. Typically, the minimum voltage swing the discriminator can see and still fully switch is about 100 mV_{PP}. The two inputs to the discriminator can be of different peak-to-peak voltage swings as long as both are over the lower limit. This allows the quadrature tank circuit to have some insertion loss. In fact, up to 8 dB insertion loss can be tolerated while still ensuring that the discriminator output won't suffer.

The quadrature circuit can also affect the discriminator output voltage swing. The discriminator output voltage swing specified assumes perfect quadrature at the frequency of interest (mixer operation). With available analog components, perfect quadrature is not possible. This is due in part to the high frequency of the IF and the proportionally very narrow bandwidth of the desired signal. For example, a DECT signal is about 1 MHz wide, which is $< 1\%$ of the IF at which the demodulation occurs. This makes the quadrature circuit difficult to achieve. With moderately high Q components, however, a reasonable phase shift can be achieved with a single pole tank. This is illustrated by the following equation: the output of the discriminator is given by

$$DISC_{out} = \cos(\omega_c t) \bullet \cos(\omega_c t + \phi), \tag{1}$$

which results in

$$DISC_{out} = \cos(\omega_c t + \omega_c t + \phi) + \cos(\omega_c t - \omega_c t - \phi). \tag{2}$$

When the double frequency component is filtered out with a low pass filter, the cosine of the phase remains

$$DISC_{out} = \cos(-\phi) = \cos(\phi). \tag{3}$$

It can be seen that at 90° phase shift, the output will be zero. At 0°, the output will be 0.5, and at 180°, it will be −0.5. The output swing is then set by the multiplication of the cosine term with the discriminator output amplifier's gain.

With a circuit that gives an output peak-to-peak voltage of 1.0 V_{PP} (min) with ideal quadrature, the slope is seen to be 5.5 mV/degree. With a practical quadrature tank circuit at 110.6 MHz, the phase shift over a 1 MHz bandwidth is about 45°−50°, which translates to an output peak-to-peak voltage of about 250 mV_{PP}.

Assume the FM modulated signal is denoted as

$$s(t) = \cos(\omega c t + m(t)), \tag{4}$$

where $m(t) = m \int_{-\infty}^{t} b(t)\,dt$,

and b(t) is the modulating baseband signal. The constant m is defined as $m = 2\Delta f T b$. The signal s(t) must be delayed by some τ so that

$$l(t) = s(t+\tau) = \cos(\omega c(t+\tau) + m(t+\tau)). \tag{5}$$

If the delay τ is such that

$$\omega c t = 2n\pi + \frac{\pi}{2}, \quad n = 0, 1, 2, 3, \ldots, \tag{6}$$

then $s(t+\tau) = \sin(\omega c t + m(t+\tau))$, (7)

and multiplying (4) and (7) yields

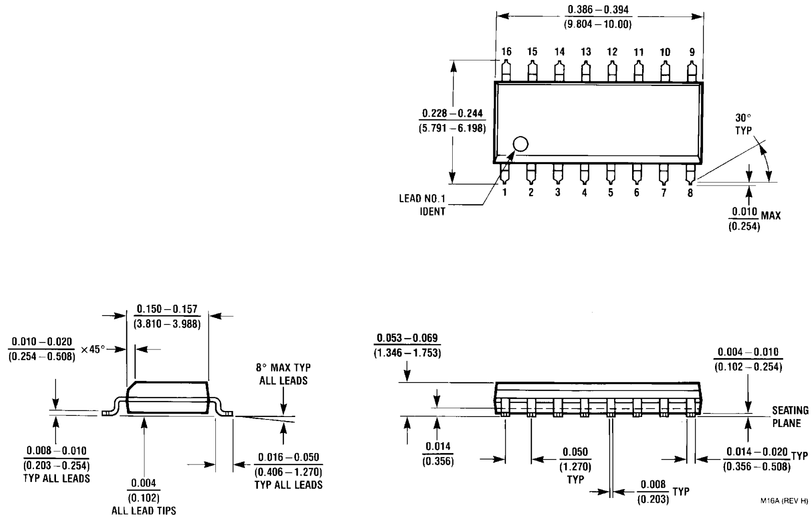
$$\begin{aligned} s(t)\,l(t) &= \cos(\omega c t + m(t)) \sin(\omega c t + m(t+\tau)) \\ &= \frac{1}{2} \sin(2\omega c t + m(t) + m(t+\tau)) \\ &\quad + \frac{1}{2} \sin(m(t+\tau) - m(t)). \end{aligned} \tag{8}$$

The double frequency component can be filtered off with a lowpass filter. If τ is kept small,

$$\begin{aligned} \frac{1}{2} \sin(m(t+\tau) - m(t)) &\approx \frac{1}{2}[m(t+\tau) - m(t)] \\ &= \frac{m}{2} \int_{-\infty}^{t+\tau} b(t)\,dt - \frac{m}{2} \int_{-\infty}^{t} b(t)\,dt \\ &= \frac{m}{2} \int_{t}^{t+\tau} b(t)\,dt \\ &\approx \tau \frac{m}{2} b(t). \end{aligned} \tag{9}$$

The object for a delay line, then, is to maximize the delay while retaining the approximations necessary to satisfy (9), $\tau < 0.1$ Tb.

Physical Dimensions inches (millimeters)



16-Lead Molded Package (SO)
Order Number LMX2240M
For Tape and Reel Order Number LMX2240MX
NS Package Number M16A

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