National Semiconductor

June 2005

LMV112
40 MHz Dual Clock Buffer

General Description

The LMV112 is a high speed dual clock buffer designed for portable communications and accurate multi-clock systems. The LMV112 integrates two 40 MHz low noise buffers which optimizes application and out performs large discrete solutions. This device enables superb system operation between the base band and the oscillator signal path while eliminating crosstalk.

National Semiconductor's unique technology and design deliver accuracy, capacitance and load resistance while increasing the drive capability of the device. The low power consumption makes the LMV112 perfect for battery applications.

The robust, independent, and flexible buffers are designed to provide the customer with the ability to manage complex clock signals in the latest wireless applications. The buffers deliver 110 V/µs internal slew rate with independent shutdown and duty cycle precision. The patented analog circuit drives capacitive loads beyond 20 pF. National's proven biasing technique has 1V centering, rail-to-rail input/output unity gain, and AC coupled convenient inputs. These integrated cells save space and require no external bias resistors. National's rapid recovery after disable optimizes performance and current consumption. The LMV112 offers individual enable pin controls and since there is no internal ground reference either single or split supply configurations offer additional system flexibility and power choices.

The LMV112 is a proven replacement for any discrete circuitry and simplifies board layout while minimizing related parasitic components.

The LMV112 is produced in the small LLP package which offers high quality while minimizing its use of PCB space. National's advanced packaging offers direct PCB-IC evaluation via pin access.

Features

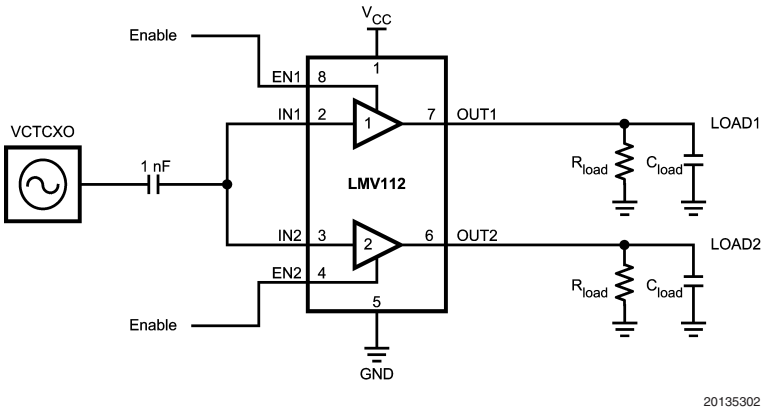
(Typical values are: V_{SUPPLY} = 2.7V and C_L = 20 pF, unless otherwise specified)

- Small signal bandwidth 40 MHz
- Supply voltage range 2.4V to 5V
- Slew rate 110 V/µs
- Total supply current 1.6 mA
- Shutdown current 59 µA
- Rail-to-rail input and output
- Individual buffer enable pins
- Rapid T_{on} technology
- Crosstalk rejection circuitry
- 8-pin LLP, pin access packaging
- Temperature range –40˚C to 85˚C

Applications

- 3G mobile applications
- WLAN–WiMAX modules
- TD_SCDMA multi-mode MP3 and camera
- GSM modules
- Oscillator modules

Typical Application



20135302

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltages ($V^+ - V^-$)	5.5V
ESD Tolerance (Note 2)	
Human Body	2000V
Machine Model	200V
Storage Temperature Range	−65˚C to +150˚C
Junction Temperature (Note 3)	+150˚C
Soldering Information	
Infrared or Convection (35 sec.)	235˚C

Operating Ratings (Note 1)

Supply Voltage ($V^+ - V^-$)	2.4V to 5.0V
Temperature Range (Notes 3, 4)	−40˚C to +85˚C
Package Thermal Resistance (Notes 3, 4)	
LLP-8 (θ_{JA})	217˚C/W

2.7V Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_J = 25˚C, V_{DD} = 2.7V, V_{SS} = 0V, V_{CM} = 1V, $Enable_{1,2} = V_{DD}$, C_L = 20 pF, R_L = 30 kΩ, $C_{COUPLING}$ = 1 nF. **Boldface** limits apply at temperature range extremes of operating condition. See (Note 4)

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
Frequency Domain Response						
SSBW	Small Signal Bandwidth	V_{IN} = 0.63 V_{PP}; −3 dB		40		MHz
FPBW	Full Power Bandwidth	V_{IN} = 1.6 V_{PP}; −3 dB		28		MHz
GFN	Gain Flatness < 0.1 dB	f > 100 kHz		3.4		MHz
Distortion and Noise Performance						
e_n	Input-Referred Voltage Noise	f = 1 MHz		26		nV/$\sqrt{Hz}$
$I_{SOLATION}$	Output to Input	f = 1 MHz		91		dB
CT	Crosstalk Rejection	f = 26 MHz, P_{IN} = 0 dBm		54		dB
Time Domain Response						
t_r	Rise Time	0.1 V_{PP} Step (10-90%), f = 1 MHz		7		ns
t_f	Fall Time			6		ns
t_s	Settling Time to 0.1%	1 V_{PP} Step, f = 1 MHz		118		ns
OS	Overshoot	0.1 V_{PP} Step, f = 1 MHz		41		%
SR	Slew Rate (Note 7)	V_{IN} = 1.6 V_{PP}, f = 26 MHz		110		V/µs
Static DC Performance						
I_S	Supply Current	$Enable_{1,2} = V_{DD}$; No Load		1.6	2.0 **2.1**	mA
		$Enable_{1,2} = V_{SS}$; No Load		59	72 **78**	µA
PSRR	Power Supply Rejection Ratio	DC (3.0V to 5.0V)	58 **57**	68		dB
A_{CL}	Small Signal Voltage Gain	V_{OUT} = 0.1 V_{PP}	0.97 **0.95**	1.01	1.05 **1.07**	V/V
V_{OS}	Output Offset Voltage			0.4	16 **17**	mV
TC V_{OS}	Temperature Coefficient Output Offset Voltage (Note 8)			4		µV/˚C
R_{OUT}	Output Resistance	f = 100 kHz		0.5		Ω
		f = 26 MHz		140		
Miscellaneous Performance						
R_{IN}	Input Resistance per Buffer	Enable = V_{DD}		141		kΩ
		Enable = V_{SS}		141		
C_{IN}	Input Capacitance per Buffer	Enable = V_{DD}		2.3		pF
		Enable = V_{SS}		2.3		
Z_{IN}	Input Impedance	f = 26 MHz, Enable = V_{DD}		10.4		kΩ
		f = 26 MHz, Enable = V_{SS}		10.9		

2.7V Electrical Characteristics (Continued)

Unless otherwise specified, all limits are guaranteed for T_J = 25˚C, V_{DD} = 2.7V, V_{SS} = 0V, V_{CM} = 1V, $Enable_{1,2}$ = V_{DD}, C_L = 20 pF, R_L = 30 kΩ, $C_{COUPLING}$ = 1 nF. **Boldface** limits apply at temperature range extremes of operating condition. See (Note 4)

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_O	Output Swing Positive	V_{IN} = V_{DD}	2.65 **2.63**	2.69		V
	Output Swing Negative	V_{IN} = V_{SS}		10	50 **65**	mV
I_{SC}	Output Short-Circuit Current (Note 9)	Sourcing	–18 **–13**	–27		mA
		Sinking	20 **16**	30		
V_{en_hmin}	Enable High Active Minimum Voltage			1.2		V
V_{en_lmax}	Enable Low Inactive Maximum Voltage			0.6		

5V Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_J = 25˚C, V_{DD} = 5V, V_{SS} = 0V, V_{CM} = 1V, $Enable_{1,2}$ = V_{DD}, C_L = 20 pF, R_L = 30 kΩ, $C_{COUPLING}$ = 1 nF. **Boldface** limits apply at temperature range extremes of operating condition. See (Note 4)

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
Frequency Domain Response						
SSBW	Small Signal Bandwidth	V_{IN} = 0.63 V_{PP}; –3 dB		42		MHz
FPBW	Full Power Bandwidth	V_{IN} = 1.6 V_{PP}; –3 dB		31		MHz
GFN	Gain Flatness < 0.1 dB	f > 100 kHz		4.9		MHz
Distortion and Noise Performance						
e_n	Input-Referred Voltage Noise	f = 1 MHz		27		nV/ $\sqrt{Hz}$
$I_{SOLATION}$	Output to Input	f = 1 MHz		90		dB
CT	Crosstalk Rejection	f = 26 MHz, P_{IN} = 0 dBm		61		dB
Time Domain Response						
t_r	Rise Time	0.1 V_{PP} Step (10-90%), f = 1 MHz		7		ns
t_f	Fall Time			6		ns
t_s	Settling Time to 0.1%	1 V_{PP} Step, f = 1 MHz		80		ns
OS	Overshoot	0.1V_{PP} Step, f = 1 MHz		20		%
SR	Slew Rate (Note 7)	V_{IN} = 1.6 V_{PP}, f = 26 MHz		120		V/µs
Static DC Performance						
I_S	Supply Current	$Enable_{1,2}$ = V_{DD} ; No Load		2.5	3.5 **3.8**	mA
		$Enable_{1,2}$ = V_{SS} ; No Load		62	80 **89**	µA
PSRR	Power Supply Rejection Ratio	DC (3.0V to 5.0V)	58 **57**	68		dB
A_{CL}	Small Signal Voltage Gain	V_{OUT} = 0.1 V_{PP}	0.99 **0.97**	1.00	1.01 **1.03**	V/V
V_{OS}	Output Offset Voltage			1.3	16 **17**	mV
TC V_{OS}	Temperature Coefficient Output Offset Voltage (Note 8)			3		µV/˚C
R_{OUT}	Output Resistance	f = 100 kHz		0.5		Ω
		f = 26 MHz		118		

5V Electrical Characteristics (Continued)

Unless otherwise specified, all limits are guaranteed for T_J = 25˚C, V_{DD} = 5V, V_{SS} = 0V, V_{CM} = 1V, $Enable_{1,2}$ = V_{DD}, C_L = 20 pF, R_L = 30 kΩ, $C_{COUPLING}$ = 1 nF. **Boldface** limits apply at temperature range extremes of operating condition. See (Note 4)

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
Miscellaneous Performance						
R_{IN}	Input Resistance per Buffer	Enable = V_{DD}		134		kΩ
		Enable = V_{SS}		134		
C_{IN}	Input Capacitance per Buffer	Enable = V_{DD}		2.0		pF
		Enable = V_{SS}		2.0		
Z_{IN}	Input Impedance	f = 26 MHz, Enable = V_{DD}		7.2		kΩ
		f = 26 MHz, Enable = V_{SS}		8.0		
V_O	Output Swing Positive	V_{IN} = V_{DD}	4.96 **4.94**	4.99		V
	Output Swing Negative	V_{IN} = V_{SS}		10	40 **55**	mV
I_{SC}	Output Short-Circuit Current (Note 9)	Sourcing	-40 **-28**	-68		mA
		Sinking	70 **50**	98		
V_{en_hmin}	Enable High Active Minimum Voltage			1.2		V
V_{en_lmax}	Enable Low Inactive Maximum Voltage			0.6		

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

Note 2: Human Body Model: 1.5 kΩ in series with 100 pF. Machine Model: 0Ω in series with 200 pF.

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} , and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 4: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. There is no guarantee of parametric performance as indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.

Note 5: Typical Values represent the most likely parametric norm.

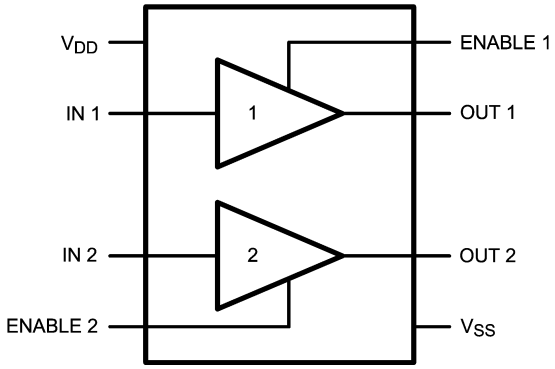
Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Slew rate is the average of the positive and negative slew rate.

Note 8: Average Temperature Coefficient is determined by dividing the changing in a parameter at temperature extremes by the total temperature change.

Note 9: Short–Circuit test is a momentary test. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C.

Block Diagram



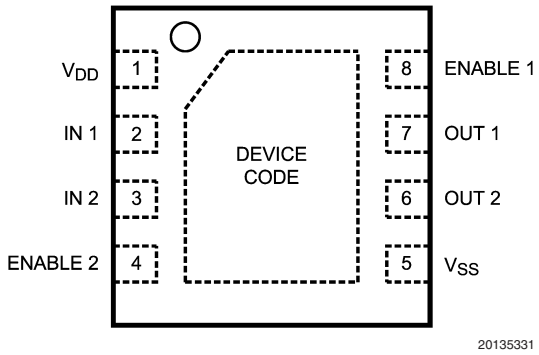
20135301

Pin Description

Pin No.	Pin Name	Description
1	V_{DD}	Voltage supply connection
2	IN 1	Input 1
3	IN 2	Input 2
4	ENABLE 2	Enable buffer 2
5	V_{SS}	Ground connection
6	OUT 2	Output 2
7	OUT 1	Output 1
8	ENABLE 1	Enable buffer 1

Connection Diagram

8-Pin LLP



20135331

Top View

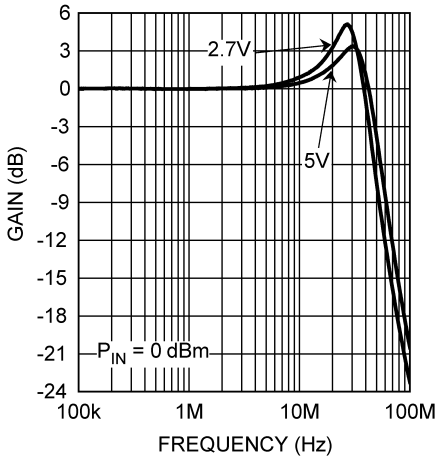
Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Pin LLP No Pull Back	LMV112SD	112SD	1k Units Tape and Reel	SDA08A
	LMV112SDX		4.5k Units Tape and Reel	

Typical Performance Characteristics

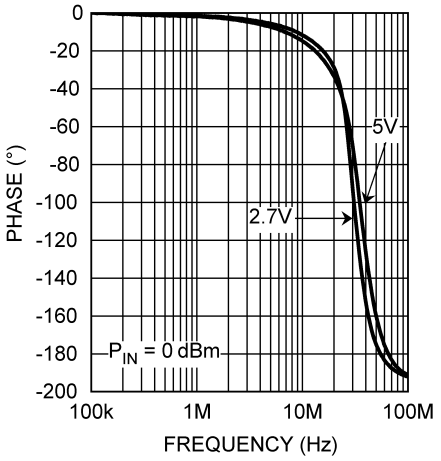
T_J = 25˚C, V_{DD} = 2.7V, V_{SS} = 0V, Enable$_{1,2}$ = V_{DD}, C_L = 20 pF, R_L = 30 kΩ and $C_{COUPLING}$ = 1 nF, unless otherwise specified.

Frequency Response



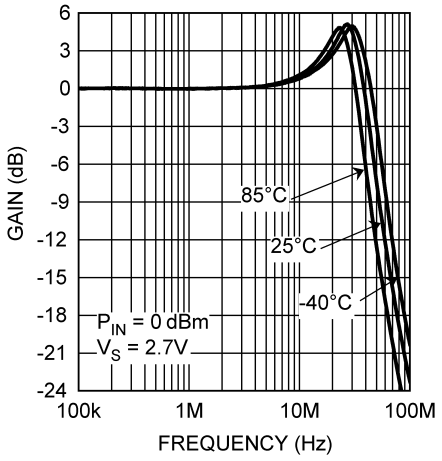
20135303

Phase Response



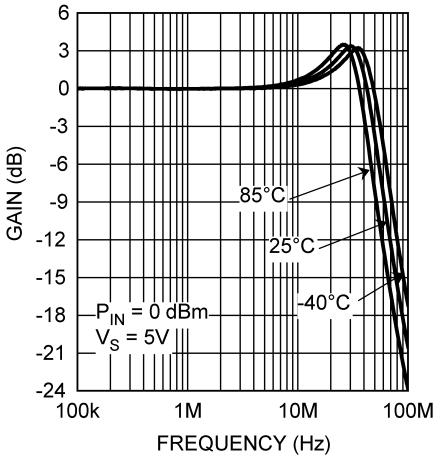
20135304

Frequency Response Over Temperature



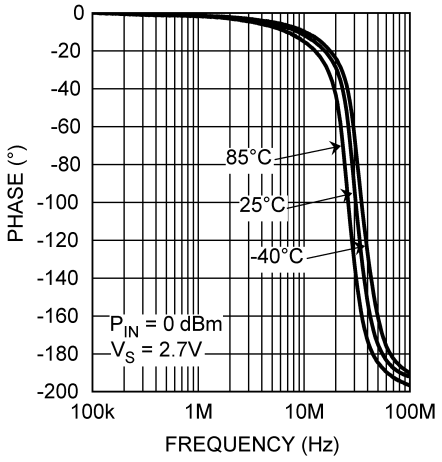
20135305

Frequency Response Over Temperature



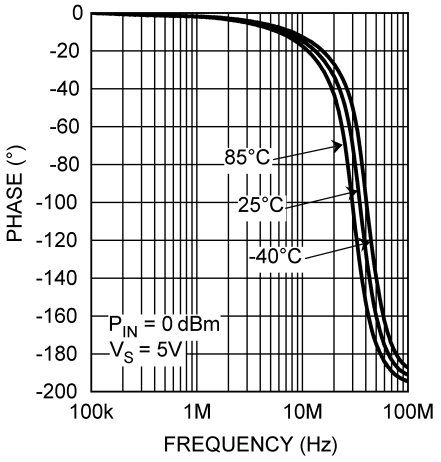
20135306

Phase Response Over Temperature



20135307

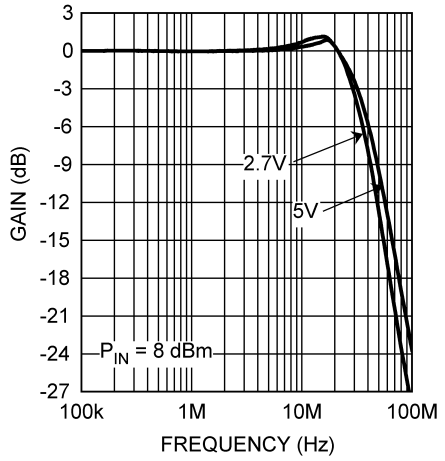
Phase Response Over Temperature



20135308

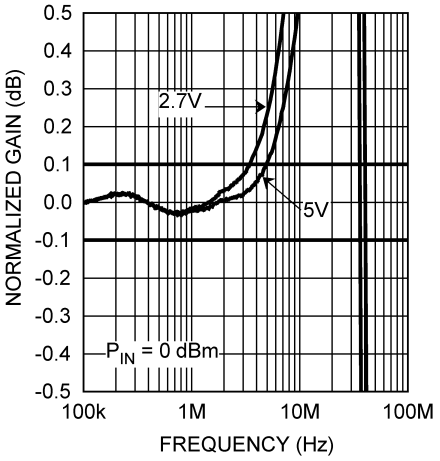
Typical Performance Characteristics T_J = 25˚C, V_{DD} = 2.7V, V_{SS} = 0V, Enable$_{1,2}$ = V_{DD}, C_L = 20 pF, R_L = 30 kΩ and $C_{COUPLING}$ = 1 nF, unless otherwise specified. (Continued)

Full Power Bandwidth



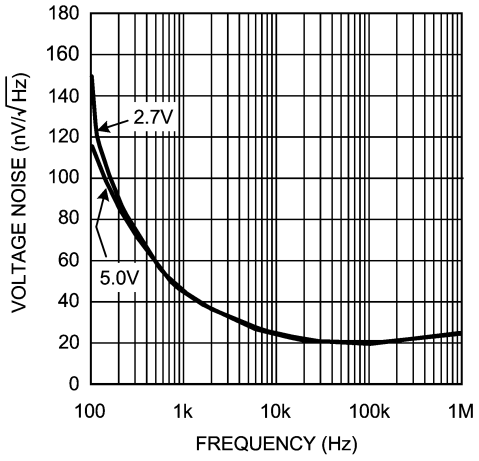
20135310

Gain Flatness 0.1 dB (GFN)



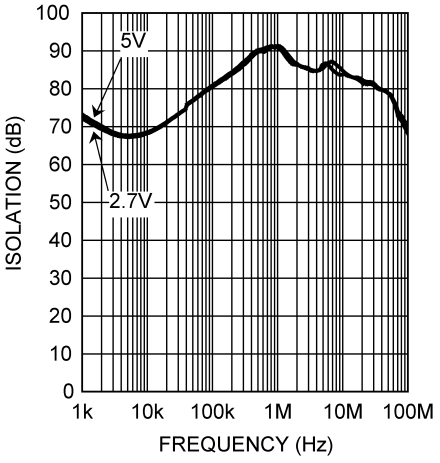
20135309

Voltage Noise



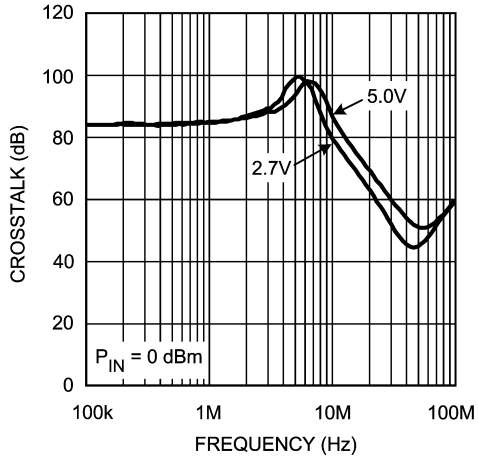
20135329

Isolation Output to Input vs. Frequency



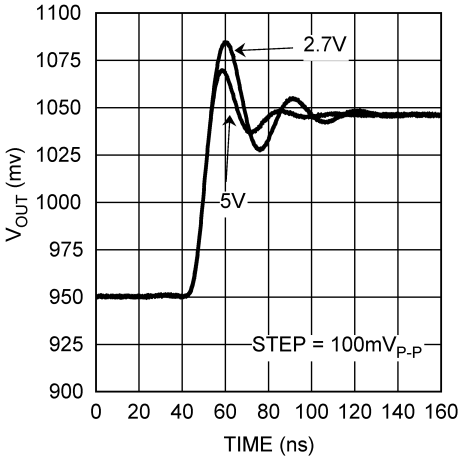
20135317

Crosstalk Rejection vs. Frequency



20135314

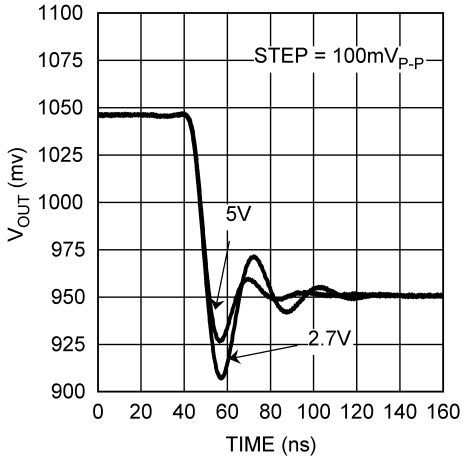
Transient Response Positive



20135311

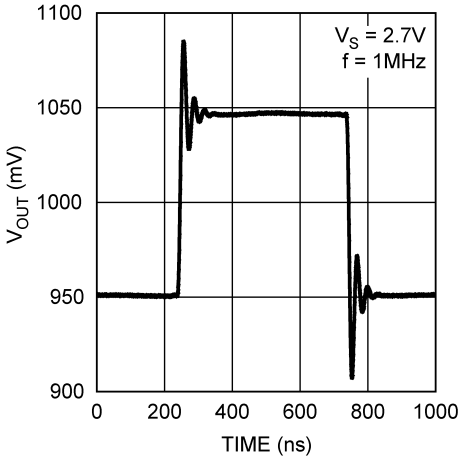
Typical Performance Characteristics T_J = 25˚C, V_{DD} = 2.7V, V_{SS} = 0V, $Enable_{1,2}$ = V_{DD}, C_L = 20 pF, R_L = 30 kΩ and $C_{COUPLING}$ = 1 nF, unless otherwise specified. (Continued)

Transient Response Negative



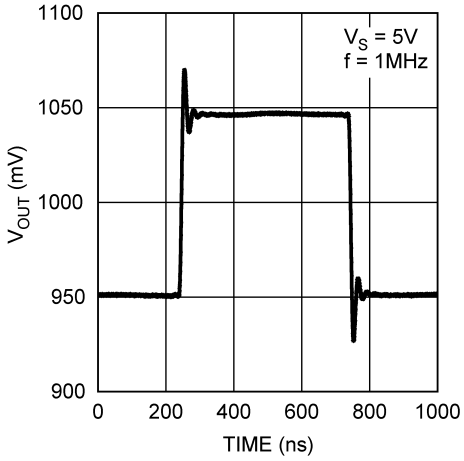
20135312

Small Signal Pulse Response



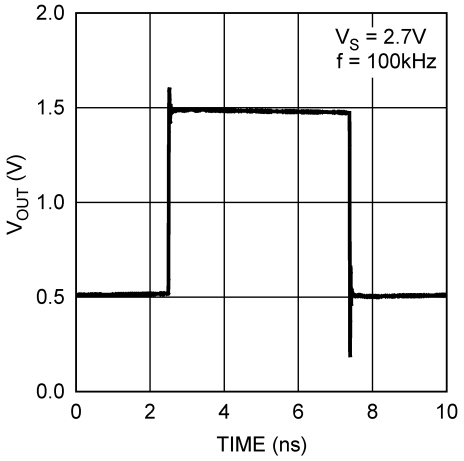
20135325

Small Signal Pulse Response



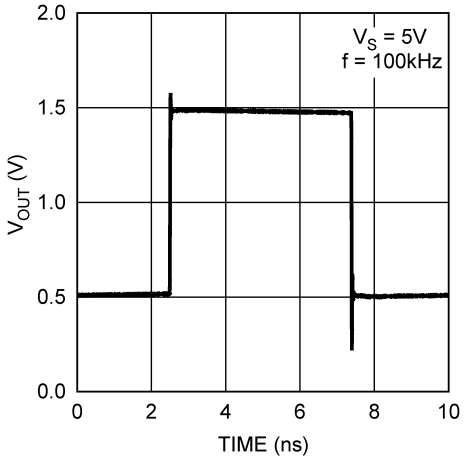
20135326

Large Signal Pulse Response



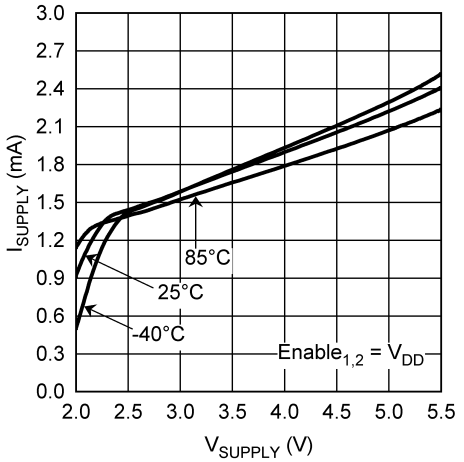
20135327

Large Signal Pulse Response



20135328

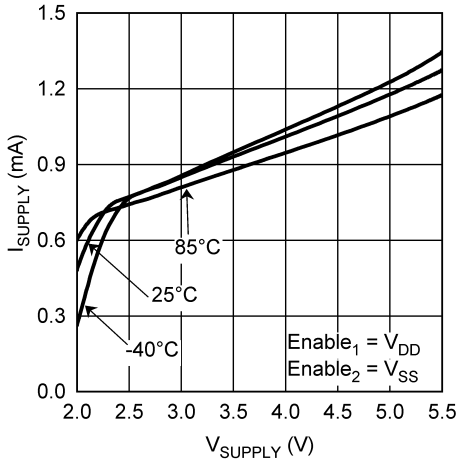
I_{SUPPLY} vs. V_{SUPPLY}



20135332

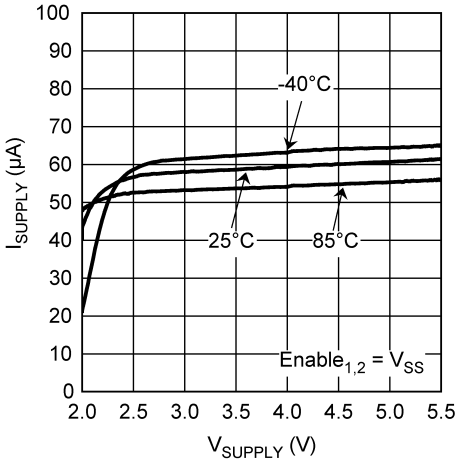
Typical Performance Characteristics T_J = 25˚C, V_{DD} = 2.7V, V_{SS} = 0V, $Enable_{1,2}$ = V_{DD}, C_L = 20 pF, R_L = 30 kΩ and $C_{COUPLING}$ = 1 nF, unless otherwise specified. (Continued)

I_{SUPPLY} vs. V_{SUPPLY}



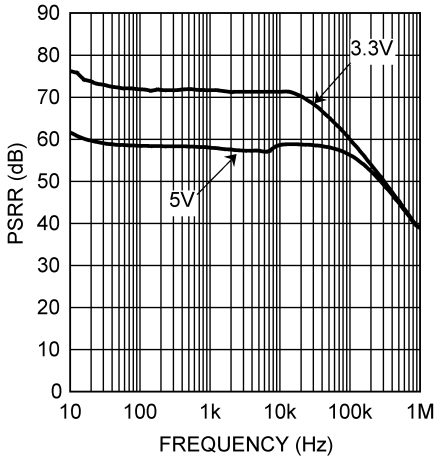
20135333

I_{SUPPLY} vs. V_{SUPPLY}



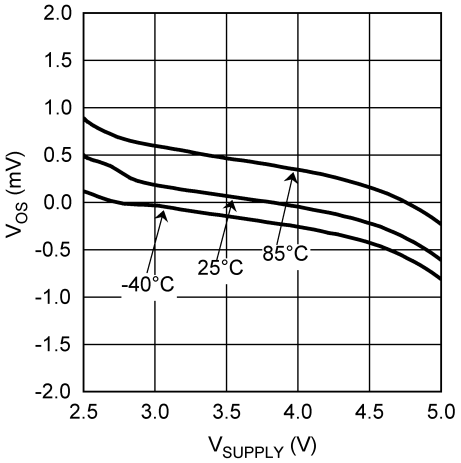
20135334

PSRR vs. Frequency



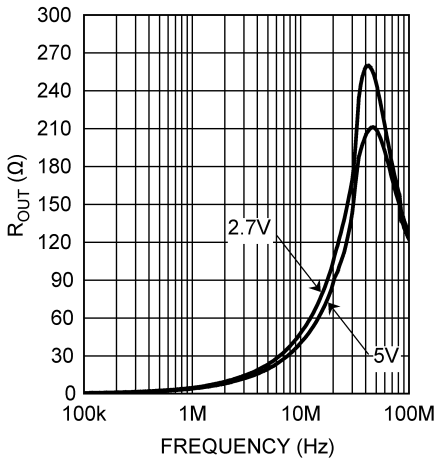
20135324

V_{OS} vs. V_{SUPPLY}



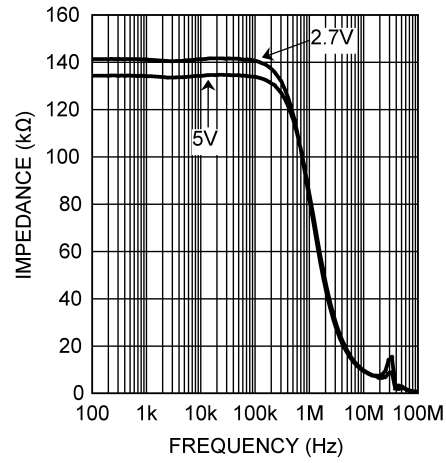
20135335

R_{OUT} vs. Frequency



20135315

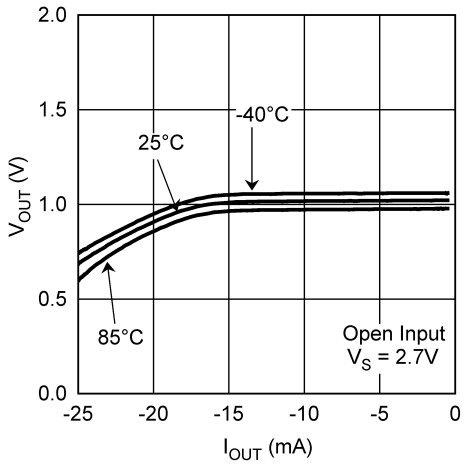
Input Impedance vs. Frequency



20135316

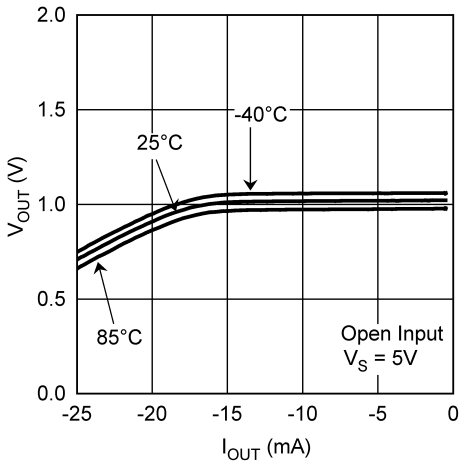
Typical Performance Characteristics T_J = 25˚C, V_{DD} = 2.7V, V_{SS} = 0V, Enable$_{1,2}$ = V_{DD}, C_L = 20 pF, R_L = 30 kΩ and $C_{COUPLING}$ = 1 nF, unless otherwise specified. (Continued)

V_{OUT} vs. I_{OUT} (Sourcing)



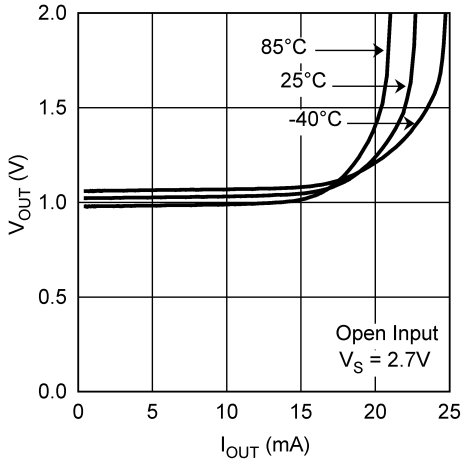
20135336

V_{OUT} vs. I_{OUT} (Sourcing)



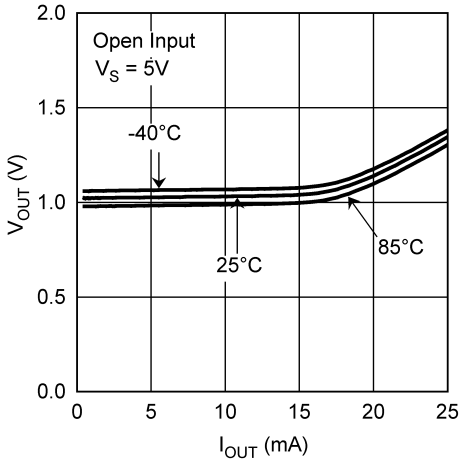
20135337

V_{OUT} vs. I_{OUT} (Sinking)



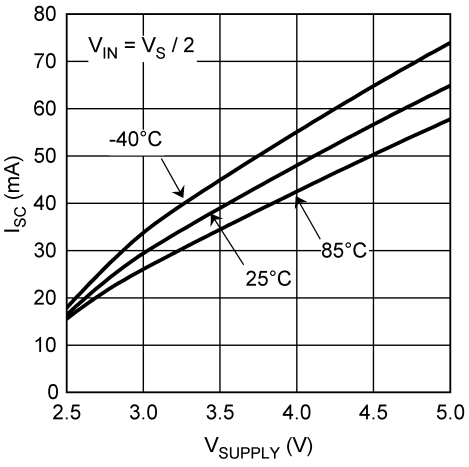
20135338

V_{OUT} vs. I_{OUT} (Sinking)



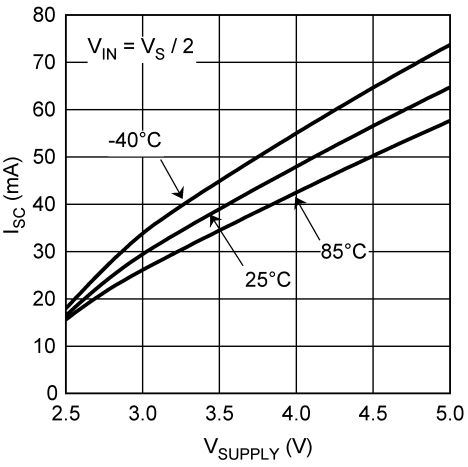
20135339

I_{SC} Sourcing vs. V_{SUPPLY} over Temperature



20135341

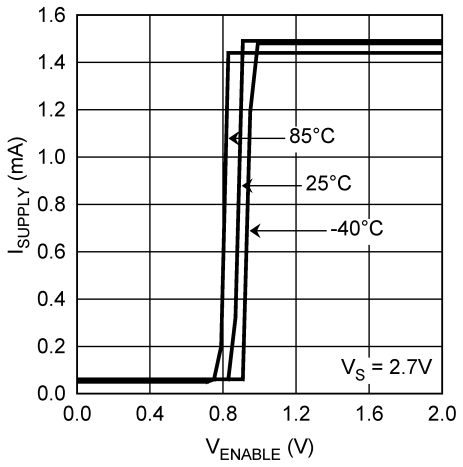
I_{SC} Sinking vs. V_{SUPPLY} over Temperature



20135342

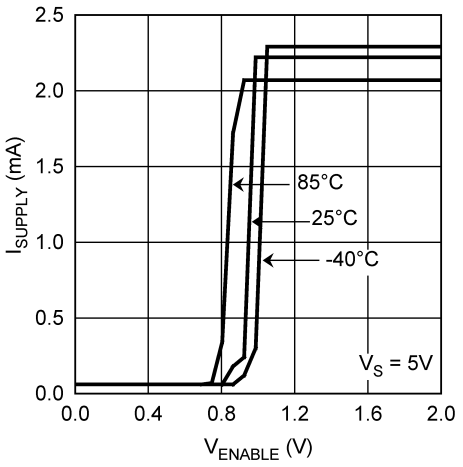
Typical Performance Characteristics T_J = 25˚C, V_{DD} = 2.7V, V_{SS} = 0V, $Enable_{1,2}$ = V_{DD}, C_L = 20 pF, R_L = 30 kΩ and $C_{COUPLING}$ = 1 nF, unless otherwise specified. (Continued)

I_{SUPPLY} vs V_{ENABLE}



20135347

I_{SUPPLY} vs V_{ENABLE}



20135348

Application Section

GENERAL

The LMV112 is designed to minimize the effects of spurious signals from the base band chip to the oscillator. Also the influence of varying load resistance and capacitance to the oscillator is minimized, while the drive capability is increased.

The inputs of the LMV112 are internally biased at 1V, making AC coupling possible without external bias resistors.

To optimize current consumption, the buffer not in use can be disabled by connecting the enable pin to V_{SS}.

The LMV112 has no internal ground reference; therefore, either single or split supply configurations can be used.

The LMV112 is an easy replacement for discrete circuitry. It simplifies board layout and minimizes the effect of layout related parasitic components.

INPUT CONFIGURATION

AC coupling is made possible by biasing the input. A large DC load at the oscillator input could change the load impedance and therefore it's oscillating frequency. To avoid external resistors the inputs are internally biased. This biasing is set at 1V as depicted in *Figure 1*. Because this biasing is set at 1V, the maximum amplitude of the AC signal is 2 V_{PP}.

The coupling capacitance should be large enough to let the AC signal pass. This is a unity gain buffer with rail-to-rail inputs and outputs.

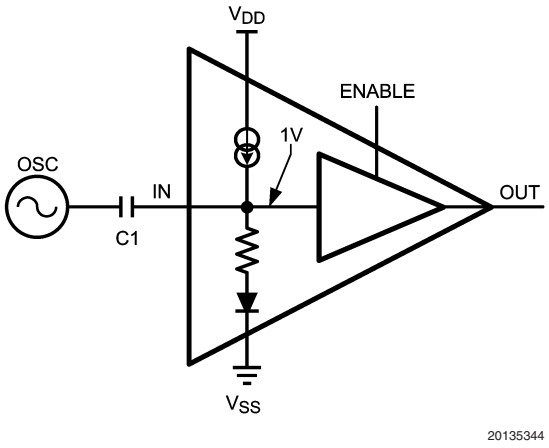


FIGURE 1. Input Configuration

FREQUENCY PULLING

Frequency pulling is the frequency variation of an oscillator caused by a varying load. In the typical application, the load of the oscillator is a fixed capacitor (C1) and the input impedance of the buffer.

To keep the input impedance as constant as possible, the input is biased at 1V, even when the part is disabled. A simplified schematic of the input configuration is shown in *Figure 1*.

ISOLATION AND CROSSTALK

Output to input isolation prevents the clock from being affected by spurious signals generated by the digital blocks at the output buffer. See the characteristic graphic entitled "Isolation Output to Input vs. Frequency."

A block diagram of the isolation is shown in *Figure 2*. Crosstalk rejection between buffers prevents signals from affecting each other. *Figure 2* shows a Base band IC and a Bluetooth module as examples of this. See the characteristic graphic labeled "Crosstalk Rejection vs. Frequency" for more information.

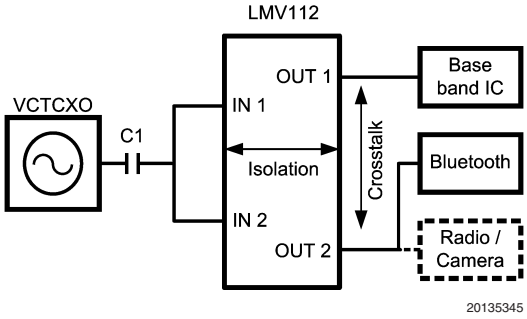


FIGURE 2. Isolation Block Diagram

DRIVING CAPACITIVE LOADS

Each buffer can drive a capacitive load. Be aware that every capacitor directly connected to the output becomes part of the loop of the buffer. In most applications the load consists of the capacitance of copper tracks and the input capacitance of the application blocks. Capacitance reduces the gain/phase margin and increases the instability. It leads to peaking in the frequency response and in extreme situations oscillations can occur. To drive a large capacitive load it is recommended that a series resistor is included between the buffer and the load capacitor. The best value for this isolation resistance is often found by experimentation.

The LMV112 datasheet reflects measurements with capacitance loads of 20 pF at the output of the buffers. Most common applications will probably use a lower capacitance load, which will result in lower peaking and significantly greater bandwidth, see *Figure 3*.

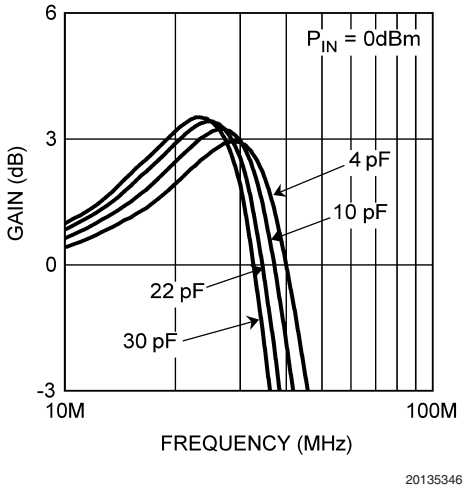


FIGURE 3. Bandwidth and Peaking

Application Section (Continued)

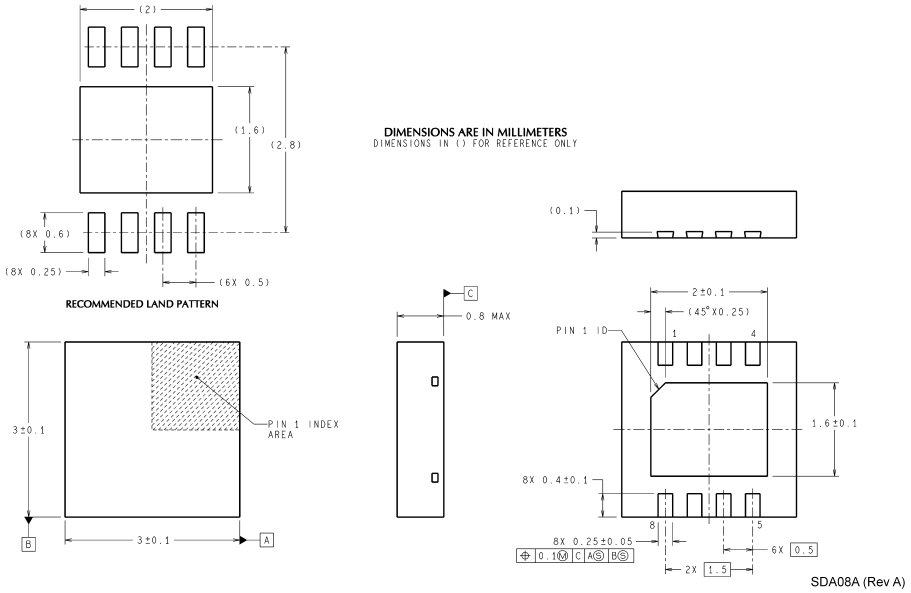
LAYOUT DESIGN RECOMMENDATION

Careful consideration for circuitry design and PCB layout will eliminate problems and will optimize the performance of the LMV112. It is best to have the same ground plane on the PCB for all power supply lines. This gives a low impedance return path for all decoupling and other ground connections.

To ensure a clean supply voltage it is best to place decoupling capacitors close to the LMV112, between V_{CC} and ground. The output of the VCO must be correctly terminated with proper load impedance.

Another important issue is the value of the components, which also determines the sensitivity to disturbances. Resistor value's should be but avoid using values that cause a significant increase in power consumption while loading inputs or outputs to heavily.

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin LLP
NS Package Number SDA08A

National Semiconductor
Americas Customer
Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

www.national.com

National Semiconductor
Europe Customer Support Center
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer
Support Center
Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560