National Semiconductor

PRELIMINARY
March 2005

LMV1024 / LMV1026
Analog to Digital Converter Amplifier for Electret Microphones in micro SMD

General Description

The LMV1024/LMV1026 integrates a pre-amplifier and a Sigma Delta modulator inside an Electret Condenser Microphone (ECM). The output of the IC is a digital serial bit stream, ideal for 4-wire Electret Condenser Microphones (ECM).

This next generation digital ECM produces an over sampled single bit stream to be connected directly to a DSP in a digital audio system. The clock input of this IC is a user adjustable clock frequency ranging between 1 and 3.25 MHz.

The LMV1024/LMV1026 enables a very robust output of an ECM by eliminating the sensitive, low-level analog signal forming the output of a conventional JFET ECM. The RF immunity is greatly improved. This eases system design and reduces external components. Furthermore this different system partitioning of the Analog-to-Digital conversion enables an all-digital baseband processor in mobile communication systems.

The LMV1024/LMV1026 is offered in a 6-bump microSMD package, suitable for the smallest ECM canisters.

Features

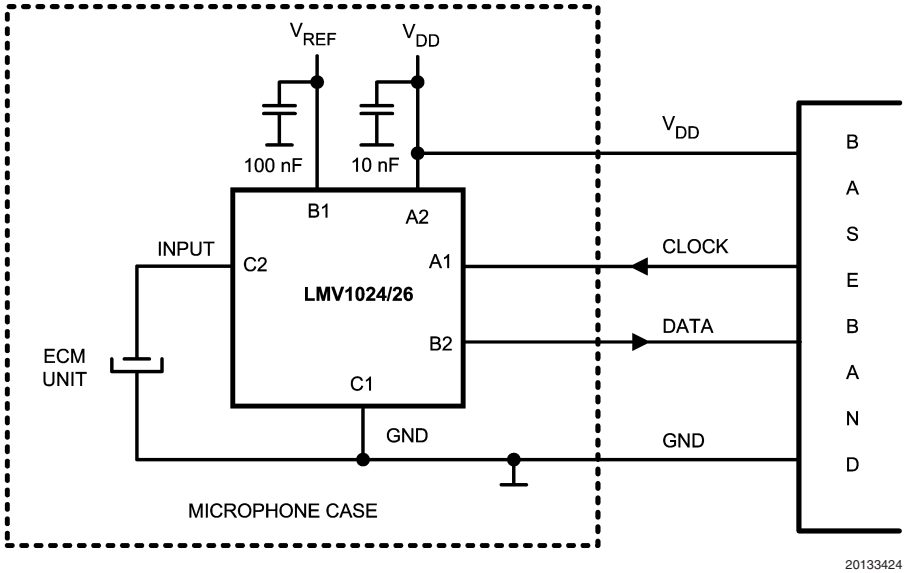
(Typical V_{DD} = 1.8V, V_{IN} = 18 mV_{PP}, unless otherwise specified)

- 1 to 3.25 MHz external clock range
- Very low noise sensitivity
- Integrated inside the ECM, reducing external components.
- Low Power, typical 600 µA I_{DD}
- 0.4 mm thickness micro SMD package for small bump

Applications

- Electret Condenser Microphone with all digital I/O
- Digital Audio subsystems
- Portable communications
- Digital Audio Computing
- Automotive subsystems

Typical Application



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	2500V
Machine Model	250V
Supply Voltage	
V_{DD} - GND	3.3V
Storage Temperature Range	−65˚C to 150˚C
Junction Temperature (Note 6)	150˚C max
Mounting Temperature	
Infrared or Convection (20 sec.)	235˚C

Operating Ratings (Note 1)

Supply Voltage	1.6V to 2.9V
Input Clock Frequency	1 MHz to 3.25 MHz
Duty Cycle	40% to 60%
Operating Temperature Range	−40˚C to 85˚C

1.8V Electrical Characteristics (Note 3)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V_{DD} = 1.8V, V_{IN} = 18 mV_{PP}, f_{CLK} = 2.4 MHz, Duty Cycle = 50% and 100 nF capacitor between V_{REF} and GND. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 4)	Typ (Note 5)	Max (Note 4)	Units
SNR	Signal to Noise Ratio	f_{IN} = 1 kHz, A-Weighted		58		dB
e_N	Digital Noise Floor (Integrated)	f = 20 Hz to 20 kHz, A-weighted, 4.7 pF Capacitor connected from Input to GND to simulate ECM		-88		dBFS(A)
THD	Total Harmonic Distortion	f_{IN} = 1 kHz, V_{IN} = 18 mV_{PP}		0.03		%
I_{DD}	Supply Current	V_{IN} = GND, CLK = ON		600		µA
		V_{IN} = GND, CLK = OFF		500		
V_{IL}	CLOCK Input Logic Low Level				**0.3**	V
V_{IH}	CLOCK Input Logic High Level		**1.5**			V
V_{OL}	DATA Output Logic Low Level				**0.1**	V
V_{OH}	DATA Output Logic High Level		**1.7**			V
V_{IN}	Max Input Signal	f_{IN} = 1 kHz, THD < 1%		300		mV_{PP}
V_{OUT}	Max Output Signal	f_{IN} = 1 kHz, THD < 1%		-5.0		dBFS
PSRR	Power Supply Rejection Ratio	V_{IN} = GND, Test signal on V_{DD} = 217 Hz, 100 mV_{PP}		82		dB
C_{IN}	Input Capacitance			2		pF
R_{IN}	Input Impedance			1000		MΩ

2.7V Electrical Characteristics (Note 3)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V_{DD} = 2.7V, V_{IN} = 18 mV_{PP}, f_{CLK} = 2.4 MHz, Duty Cycle = 50% and 100 nF capacitor between V_{REF} and GND. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 4)	Typ (Note 5)	Max (Note 4)	Units
SNR	Signal to Noise Ratio	f_{IN} = 1 kHz, A-Weighted		58		dB
e_n	Digital Noise Floor (Integrated)	f = 20 Hz to 20 kHz, A-weighted, 4.7 pF Capacitor connected from Input to GND to simulate ECM		-88		dBFS(A)
THD	Total Harmonic Distortion	f_{IN} = 1 kHz, V_{IN} = 18 mV_{PP}		0.04		%
I_{DD}	Supply Current	V_{IN} = GND, CLK = ON		650		µA
		V_{IN} = GND, CLK = OFF		550		
V_{LOW}	CLOCK Logic Low Level				**0.3**	V
V_{HIGH}	CLOCK Logic High Level		**2.4**			V
V_{OL}	DATA Output Logic Low Level				**0.1**	V
V_{OH}	DATA Output Logic High Level		**2.6**			V
V_{IN}	Max Input Signal	f_{IN} = 1 kHz, THD < 1%		320		mV_{PP}
V_{OUT}	Max Output Signal	f_{IN} = 1 kHz, THD < 1%		-4.4		dBFS

2.7V Electrical Characteristics (Note 3) (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V_{DD} = 2.7V, V_{IN} = 18 mV_{PP}, f_{CLK} = 2.4 MHz, Duty Cycle = 50% and 100 nF capacitor between V_{REF} and GND. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 4)	Typ (Note 5)	Max (Note 4)	Units
PSRR	Power Supply Rejection Ratio	V_{IN} = GND, Test signal on V_{DD} = 217 Hz, 100 mV_{PP}		82		dB
C_{IN}	Input Capacitance			2		pF
R_{IN}	Input Impedance			1000		MΩ

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human Body Model (HBM) is 1.5 kΩ in series with 100 pF.

Note 3: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.

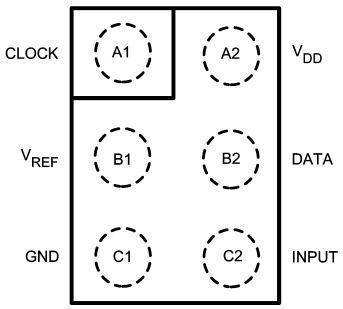
Note 4: All limits are guaranteed by design or statistical analysis.

Note 5: Typical values represent the most likely parametric norm.

Note 6: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Connection Diagram

6-Bump Ultra Thin micro SMD



Top View

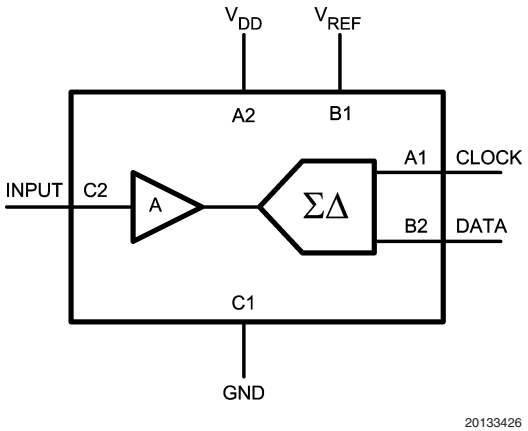
Pin Description

	Pin	Name	Description
Power Supply	A2	V_{DD}	Positive supply voltage
	C1	GND	Ground
Input	C2	Input	The microphone is connected to this input pin.
Reference	B1	V_{REF}	A capacitor of 100 nF is connected between V_{REF} and ground. This capacitor is used to filter the internal converter reference voltage.
Clock Input	A1	Clock	The user adjustable clock frequency ranges from 1 to 3.25 MHz.
Data Output	B2	Data	Over sampled bitstream output. Data is valid if clock is LOW (LMV1024). The data of the LMV1026 data is valid when clock is HIGH. When the data is not valid the data output is Hi-Z. For exact specifications see application section.

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
6-Bump Ultra Thin micro SMD (0.4 mm max height) lead free only	LMV1024UP	TBD	1k Units Tape and Reel	UPA06XXX
	LMV1024UPX		3k Units Tape and Reel	
	LMV1026UP	TBD	1k Units Tape and Reel	
	LMV1026UPX		3k Units Tape and Reel	

Block Diagram



Application Section

INTERFACE TIMING

For stereo applications, the data is only valid for one half clock cycle to allow for two microphones on the same I/O lines (Data and Clock). To avoid overlap between the drivers of the microphones, one microphone always goes into a high impedance state before the second microphone starts driving the line. This is shown in the timing chart below.

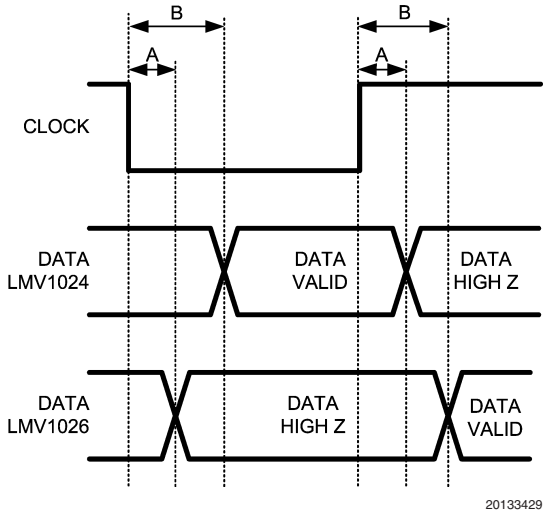


FIGURE 1. Timing Diagram

TABLE 1. Timing Characteristics

Symbol	Parameter	Typ	Unit
A	Time from rising edge of Clock to Data becoming high impedance	50	ns
B	Time from falling edge of Clock to Data becoming valid.	100	ns

STEREO MICROPHONE

Since the data on the dataline is valid for half a period of the clock (*Figure 1*) it is possible to realize an application where two IC's communicate over the same I/O lines (Data and Clock). The LMV1024 and LMV1026 are required to communicate in a different half of the clock period. Therefore, different IC's have been developed. The LMV1024 is positive edge triggered and the LMV1026 is negative edge triggered. When the data of one IC is valid, the data line of the second IC is high impedance.

This feature enables the realization of a stereo microphone where two microphones use the same communication lines. *Figure 2* shows the typical application schematic of two microphones in a stereo application.

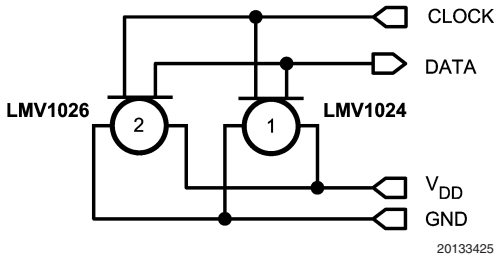


FIGURE 2. Stereo Microphone Setup

LAYOUT CONSIDERATIONS

To obtain the best possible performance of the microphone, special care needs to be taken for the design of the PCB. The V_{IN} trace is the most sensitive as it is connected to the high impedance electret element. To avoid any switching noise coupling into the input of the IC, it is essential to isolate and shield the V_{IN} trace from the digital signal traces. An example of an optimized PCB layout is given in *Figure 3*.

The microphone PCB has two capacitors. One capacitor (100 nF) is connected to the reference pin of the LMV1024/LMV1026 and the other (10 nF) is used to decouple high frequencies from the supply line. No capacitors should be placed on the data output of the LMV1024/LMV1026 since it will only load the output driver and degrade the overall performance. This is contrary to the analog phantom biased microphones, where capacitors are needed to improve RF immunity at the output of the device.

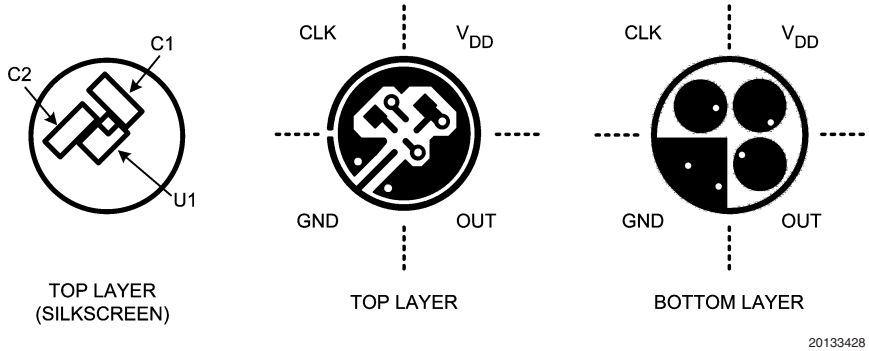
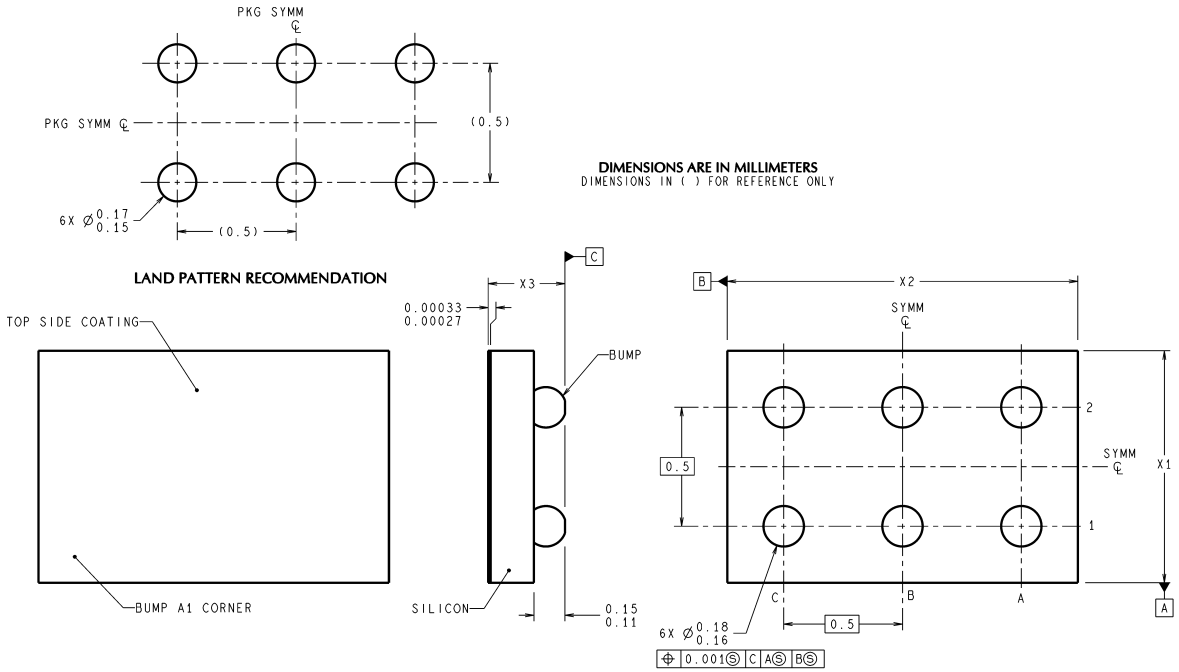


FIGURE 3. PCB Layout

Physical Dimensions inches (millimeters) unless otherwise noted



UPA06XXX (Rev A)

NOTE: UNLESS OTHERWISE SPECIFIED.

1. TITANIUM COATING
2. FOR SOLDER BUMP COMPOSITION, SEE “SOLDER INFORMATION” IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
3. RECOMMEND NON-SOLDER MASK DEFINED LANDING PAD.
4. PIN A1 IS ESTABLISHED BY LOWER LEFT CORNER WITH RESPECT TO TEXT ORIENTATION.
5. XXX IN DRAWING NUMBER REPRESENTS PACKAGE SIZE VARIATION WHERE X1 IS PACKAGE WIDTH, X2 IS PACKAGE LENGTH AND X3 IS PACKAGE HEIGHT.
6. REFERENCE JEDEC REGISTRATION MO-211. VARIATION CB.

6-Bump Ultra Thin micro SMD
NS Package Number UPA06XXX

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