October 2005

National Semiconductor

LMP7711
Precision, 17 MHz, Low Noise, CMOS Input Amplifier

General Description

The LMP7711 is a low noise, low offset, CMOS input, rail-to-rail output precision amplifier with a high gain bandwidth product and an enable pin. The LMP7711 is part of the LMP™ precision amplifier family and are ideal for a variety of instrumentation applications.

Utilizing a CMOS input stage, the LMP7711 achieves an input bias current of 100 fA, an input referred voltage noise of 5.8 nV/ $\sqrt{\text{Hz}}$, and an input offset voltage of less than ±150 µV. These features make the LMP7711 a superior choice for precision applications.

Consuming only 1.15 mA of supply current, the LMP7711 offers a high gain bandwidth product of 17 MHz, enabling accurate amplification at high closed loop gains.

The LMP7711 has a supply voltage range of 1.8V to 5.5V, which makes these ideal choices for portable low power applications with low supply voltage requirements. In order to reduce the already low power consumption the LMP7711 has an enable function. Once in shutdown, the LMP7711 draws only 140 nA of supply current.

The LMP7711 is built with National's advanced VIP50 process technology. The LMP7711 is offered in a 6-pin TSOT23 package.

Features

Unless otherwise noted, typical values at V_S = 5V.

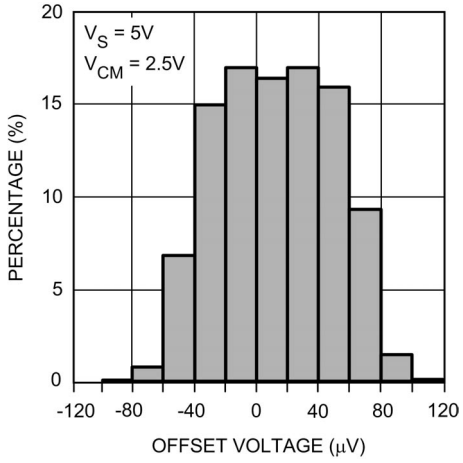
- Input offset voltage ±150 µV (max)
- Input bias current 100 fA
- Input voltage noise 5.8 nV/ $\sqrt{\text{Hz}}$
- Gain bandwidth product 17 MHz
- Supply current 1.15 mA
- Supply voltage range 1.8V to 5.5V
- THD+N @ f = 1 kHz 0.001%
- Operating temperature range –40°C to 125°C
- Rail-to-rail output swing
- Space saving TSOT23 package

Applications

- Active filters and buffers
- Sensor interface applications
- Transimpedance amplifiers

Typical Performance

Offset Voltage Distribution



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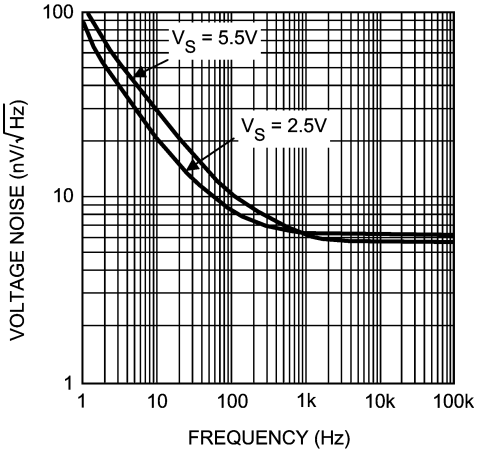
Input Referred Voltage Noise



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body	2000V
Machine Model	200V
V_{IN} Differential	±0.3V
Supply Voltage ($V_S = V^+ - V^-$)	6.0V
Voltage on Input/Output Pins	V^+ +0.3V, V^- −0.3V
Storage Temperature Range	−65˚C to 150˚C
Junction Temperature (Note 3)	+150˚C
Soldering Information	
Infrared or Convection (20 sec)	235˚C
Wave Soldering Lead Temp. (10 sec)	260˚C

Operating Ratings (Note 1)

Temperature Range (Note 3)	−40˚C to 125˚C
Supply Voltage ($V_S = V^+ - V^-$)	
0˚C ≤ T_A ≤ 125˚C	1.8V to 5.5V
−40˚C ≤ T_A ≤ 125˚C	2.0V to 5.5V
Package Thermal Resistance (θ_{JA}(Note 3))	
6-Pin TSOT23	170˚C/W

2.5V Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_A = 25˚C, V^+ = 2.5V, V^- = 0V ,$V_O = V_{CM} = V^+/2$, $V_{EN} = V^+$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
V_{OS}	Input Offset Voltage			±20	±180 **±580**	µV
TC V_{OS}	Input Offset Voltage Drift	(Note 6)		−1	±4	µV/˚C
I_B	Input Bias Current	V_{CM} = 1V (Notes 7, 8)		0.05	50 **100**	pA
I_{OS}	Input Offset Current	V_{CM} = 1V (Note 8)		0.006	25 **50**	pA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.4V	83 **80**	100		dB
PSRR	Power Supply Rejection Ratio	2.0V ≤ V^+ ≤ 5.5V V^- = 0V, V_{CM} = 0	85 **80**	100		dB
		1.8V ≤ V^+ ≤ 5.5V V^- = 0V, V_{CM} = 0	85	98		
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 80 dB CMRR ≥ 78 dB	−0.3 **−0.3**		1.5 **1.5**	V
A_{VOL}	Large Signal Voltage Gain	V_O = 0.15 to 2.2V R_L = 2 kΩ to $V^+/2$	88 **82**	98		dB
		V_O = 0.15 to 2.2V R_L = 10 kΩ to $V^+/2$	92 **88**	110		
V_O	Output Swing High	R_L = 2 kΩ to $V^+/2$	70 **77**	25		mV from V^+
		R_L = 10 kΩ to $V^+/2$	60 **66**	20		
	Output Swing Low	R_L = 2 kΩ to $V^+/2$		30	70 **73**	mV
		R_L = 10 kΩ to $V^+/2$		15	60 **62**	
I_O	Output Short Circuit Current	Sourcing to V^- V_{IN} = 200 mV (Note 9)	36 **30**	52		mA
		Sinking to V^+ V_{IN} = −200 mV (Note 9)	7.5 **5.0**	15		
I_S	Supply Current	Enable Mode V_{EN} ≥ 2.1		0.95	1.30 **1.65**	mA
		Shutdown Mode V_{EN} ≤ 0.4		0.03	1 **4**	µA

2.5V Electrical Characteristics (Continued)

Unless otherwise specified, all limits are guaranteed for T_A = 25˚C, V^+ = 2.5V, V^- = 0V ,V_O = V_{CM} = V^+/2, V_{EN} = V^+. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
SR	Slew Rate	A_V = +1, Rising (10% to 90%)		8.3		V/µs
		A_V = +1, Falling (90% to 10%)		10.3		
GBW	Gain Bandwidth Product			14		MHz
e_n	Input-Referred Voltage Noise	f = 400 Hz		7		nV/ $\sqrt{Hz}$
		f = 1 kHz		6.2		
i_n	Input-Referred Current Noise	f = 1 kHz		0.01		pA/ $\sqrt{Hz}$
t_{on}	Turn-on Time			140		ns
t_{off}	Turn-off Time			1000		ns
V_{EN}	Shutdown Pin Voltage	Enable Mode	2.1	2		V
		Shutdown Mode		0.5	0.4	
I_{EN}	Shutdown Pin Input Current	V_{EN} = 2.5V (Note 7)		1.5	3.0	µA
		V_{EN} = 0V (Note 7)		0.003	0.1	
THD + N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 1, R_L = 100 kΩ V_O = 0.9 V_{PP}		0.003		%
		f = 1 kHz, A_V = 1, R_L = 600Ω V_O = 0.9 V_{PP}		0.004		

5V Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_A = 25˚C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, V_{EN} = V^+. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
V_{OS}	Input Offset Voltage			±10	±150 **±550**	µV
TC V_{OS}	Input Offset Average Drift	(Note 6)		–1	±4	µV/˚C
I_B	Input Bias Current	(Notes 7, 8)		0.1	50 **100**	pA
I_{OS}	Input Offset Current	(Note 8)		0.01	25 **50**	pA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3.7V	85 **82**	100		dB
PSRR	Power Supply Rejection Ratio	2.0V ≤ V^+ ≤ 5.5V V^- = 0V, V_{CM} = 0	85 **80**	100		dB
		1.8V ≤ V^+ ≤ 5.5V V^- = 0V, V_{CM} = 0	85	98		
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 80 dB CMRR ≥ 78 dB	–0.3 **–0.3**		4 **4**	V
A_{VOL}	Large Signal Voltage Gain	V_O = 0.3 to 4.7V R_L = 2 kΩ to V^+/2	88 **82**	107		dB
		V_O = 0.3 to 4.7V R_L = 10 kΩ to V^+/2	92 **88**	110		

5V Electrical Characteristics (Continued)

V_O	Output Swing High	R_L = 2 kΩ to $V^+/2$	70 **77**	32		mV from V^+
		R_L = 10 kΩ to $V^+/2$	60 **66**	22		
	Output Swing Low	R_L = 2 kΩ to $V^+/2$		42	70 **73**	mV
		R_L = 10 kΩ to $V^+/2$		20	60 **62**	
I_O	Output Short Circuit Current	Sourcing to V^- V_{IN} = 200 mV (Note 9)	46 **38**	66		mA
		Sinking to V^+ V_{IN} = −200 mV (Note 9)	10.5 **6.5**	23		
I_S	Supply Current	Enable Mode $V_{EN} \geq 4.6$		1.15	1.40 **1.75**	mA
		Shutdown Mode $V_{EN} \leq 0.4$		0.14	1 **4**	µA
SR	Slew Rate	A_V = +1, Rising (10% to 90%)	6.0	9.5		V/µs
		A_V = +1, Falling (90% to 10%)	7.5	11.5		
GBW	Gain Bandwidth Product			17		MHz
e_n	Input-Referred Voltage Noise	f = 400 Hz		6.8		nV/ $\sqrt{Hz}$
		f = 1 kHz		5.8		
i_n	Input-Referred Current Noise	f = 1 kHz		0.01		pA/ $\sqrt{Hz}$
t_{on}	Turn-on Time			110		ns
t_{off}	Turn-off Time			800		ns
V_{EN}	Enable Pin Voltage	Enable Mode	4.6	4.5		V
		Shutdown Mode		0.5	0.4	
I_{EN}	Enable Pin Input Current	V_{EN} = 5V (Note 7)		5.6	10	µA
		V_{EN} = 0V (Note 7)		0.005	0.2	
THD + N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 1, R_L = 100 kΩ V_O = 4 V_{PP}		0.001		%
		f = 1 kHz, A_V = 1, R_L = 600Ω V_O = 4 V_{PP}		0.004		

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

Note 2: Human Body Model: 1.5 kΩ in series with 100 pF. Machine Model: 0Ω in series with 200 pF.

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Note 4: Typical values represent the most likely parametric norm at the time of characterization.

Note 5: Limits are 100% production tested at 25˚C. Limits over the operating temperature range are guaranteed through correlations using the Statistical Quality Control (SQC) method.

Note 6: Offset voltage average drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.

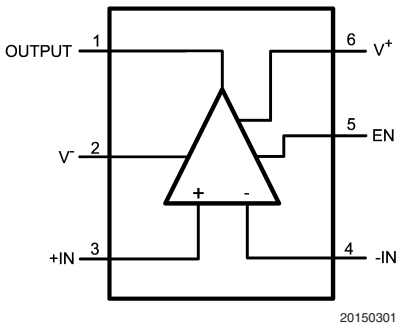
Note 7: Positive current corresponds to current flowing into the device.

Note 8: Guaranteed by design.

Note 9: The short circuit test is a momentary test.

Connection Diagram

6-Pin TSOT23



Top View

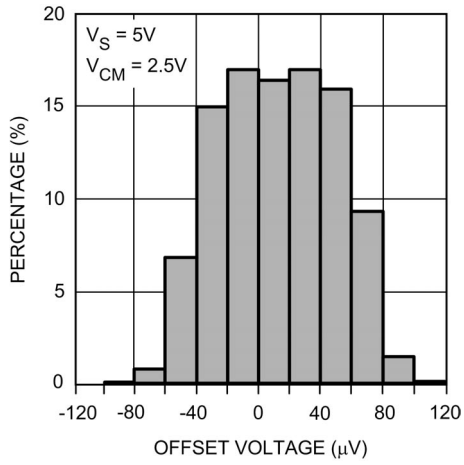
Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
6-Pin TSOT23	LMP7711MK	AC3A	1k Units Tape and Reel	MK06A
	LMP7711MKX		3k Units Tape and Reel	

Typical Performance Characteristics

Unless otherwise noted: T_A = 25˚C, V_S = 5V, V_{CM} = 2.5V

Offset Voltage Distribution



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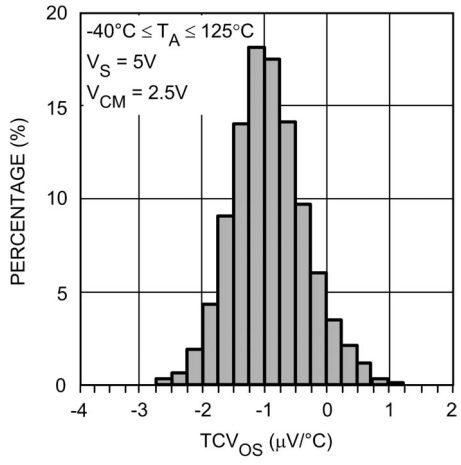
TCV_{OS} Distribution



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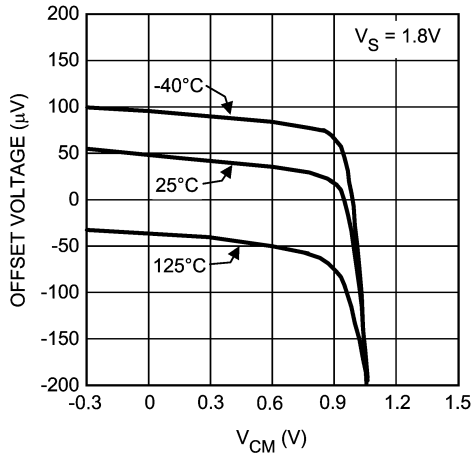
Offset Voltage vs. V_{CM}



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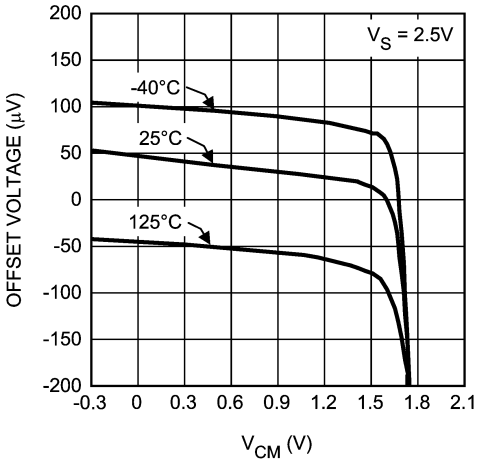
Offset Voltage vs. V_{CM}



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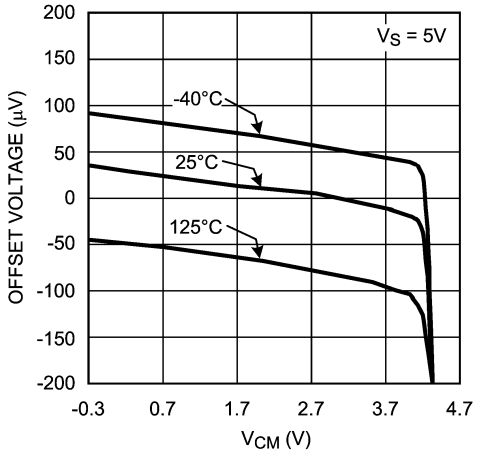
Offset Voltage vs. V_{CM}



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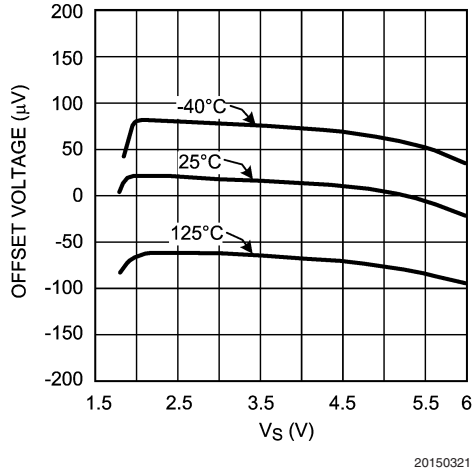
Offset Voltage vs. Supply Voltage



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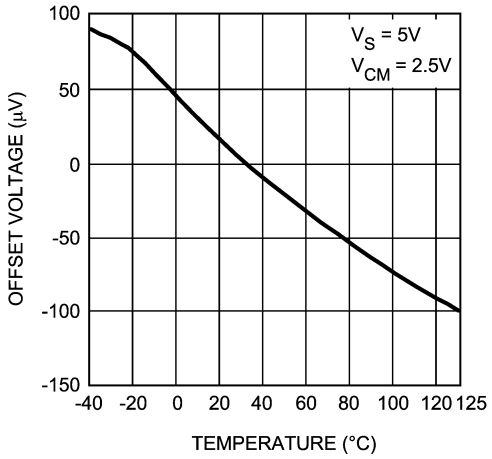
Typical Performance Characteristics Unless otherwise noted: T_A = 25˚C, V_S = 5V, V_{CM} = 2.5V (Continued)

Offset Voltage vs. Temperature



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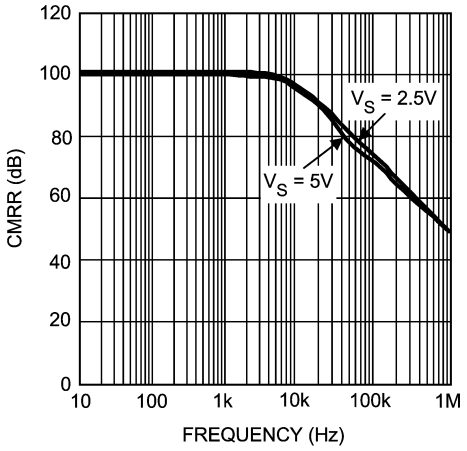
CMRR vs. Frequency



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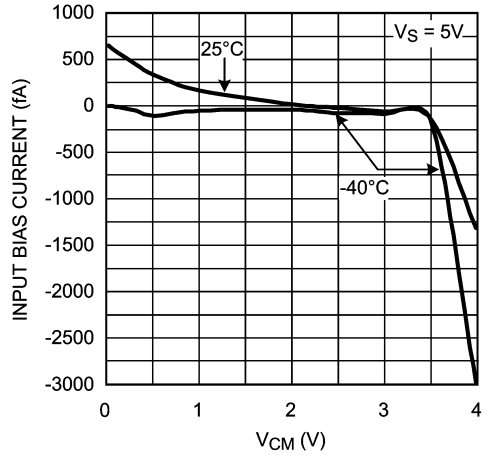
Input Bias Current Over Temperature



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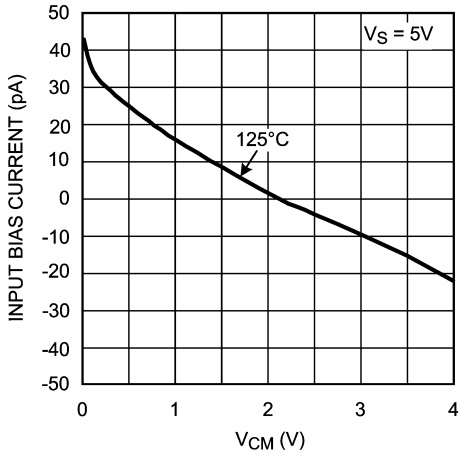
Input Bias Current Over Temperature



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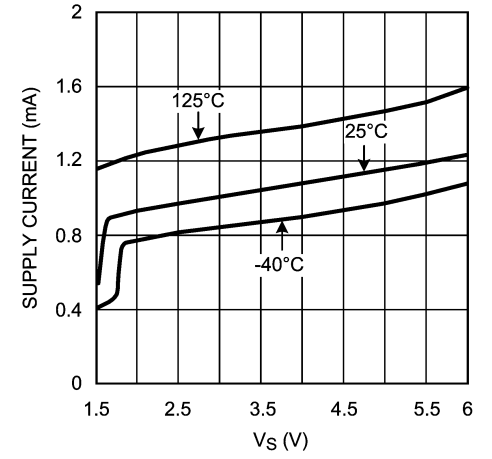
Supply Current vs. Supply Voltage



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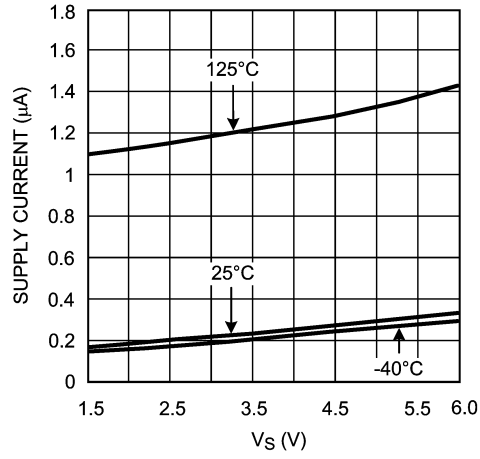
Supply Current vs. Supply Voltage (Shutdown)



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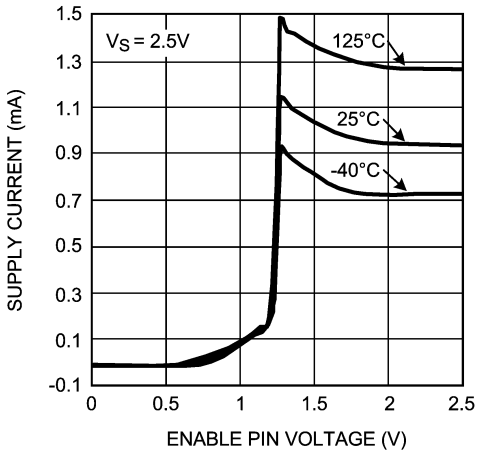
Typical Performance Characteristics Unless otherwise noted: T_A = 25˚C, V_S = 5V, V_{CM} = 2.5V (Continued)

Supply Current vs. Enable Pin Voltage



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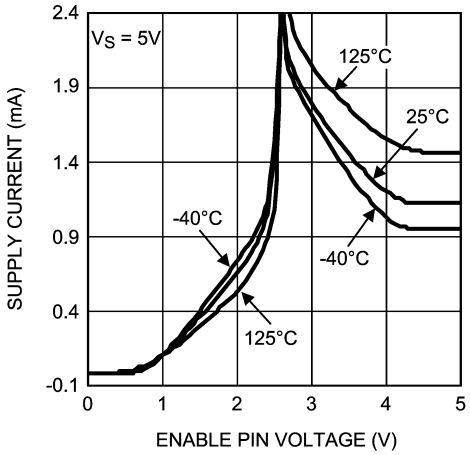
Supply Current vs. Enable Pin Voltage



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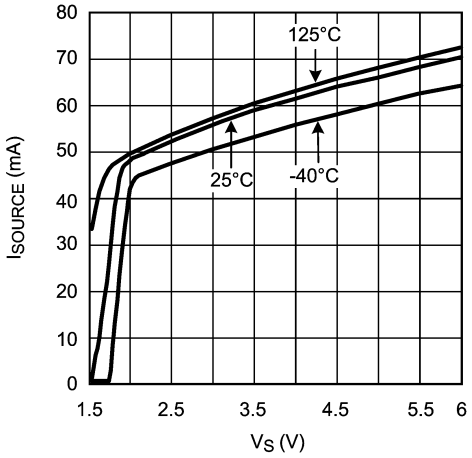
Sourcing Current vs. Supply Voltage



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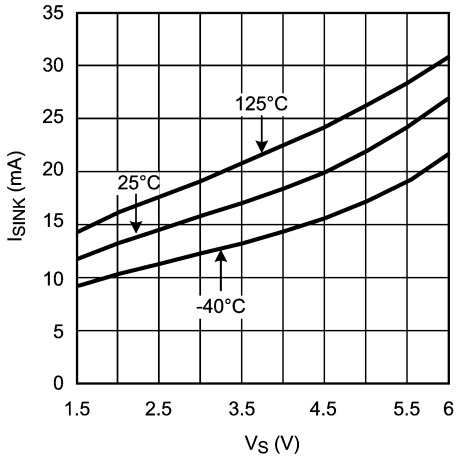
Sinking Current vs. Supply Voltage



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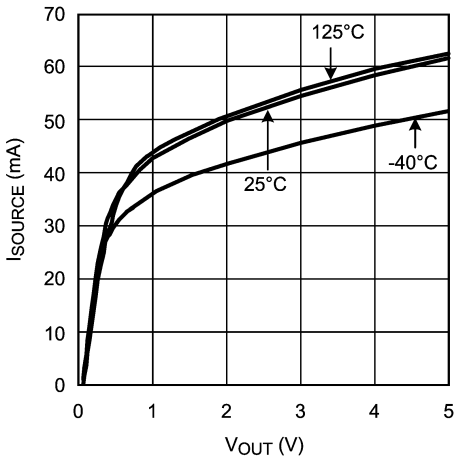
Sourcing Current vs. Output Voltage



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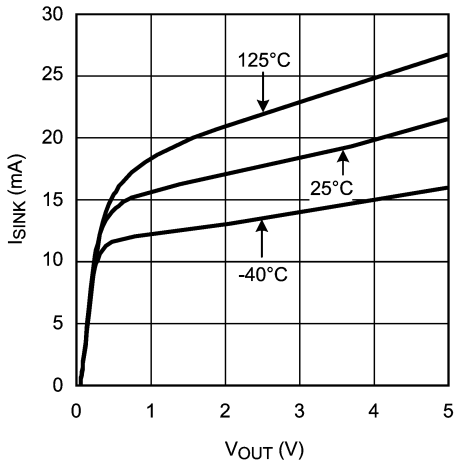
Sinking Current vs. Output Voltage



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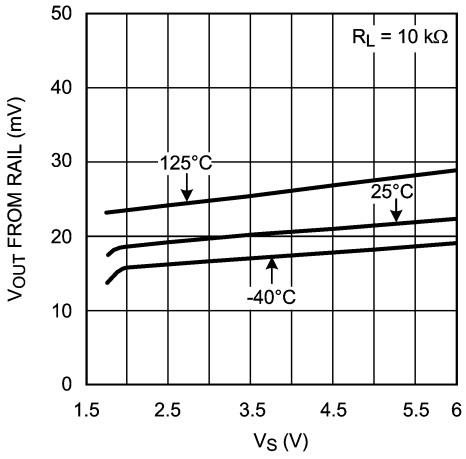
Typical Performance Characteristics Unless otherwise noted: T_A = 25˚C, V_S = 5V, V_{CM} = 2.5V (Continued)

Output Swing High vs. Supply Voltage



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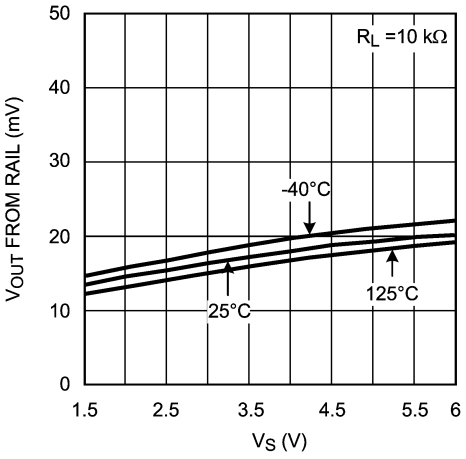
Output Swing Low vs. Supply Voltage



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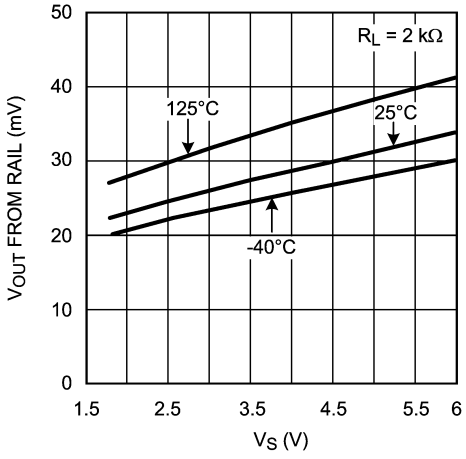
Output Swing High vs. Supply Voltage



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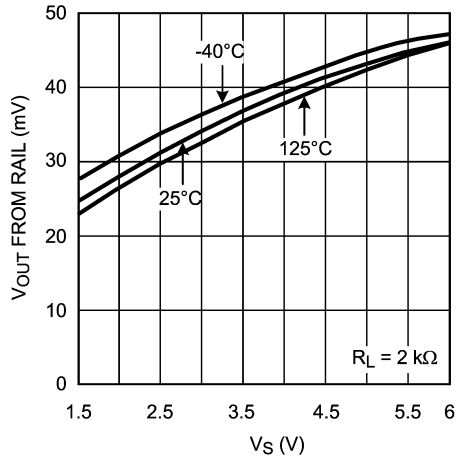
Output Swing Low vs. Supply Voltage



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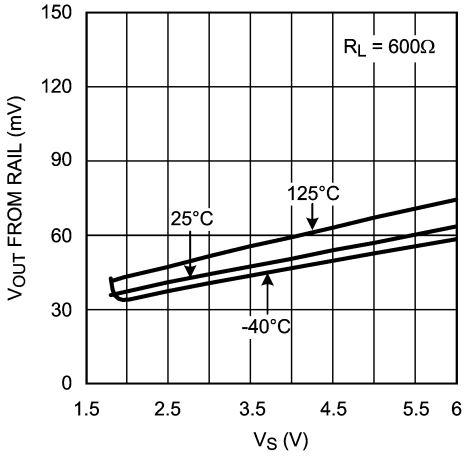
Output Swing High vs. Supply Voltage



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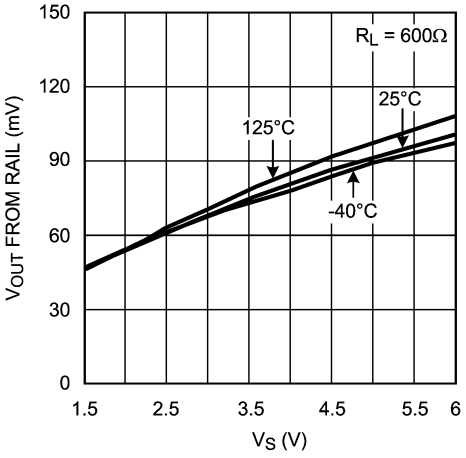
Output Swing Low vs. Supply Voltage



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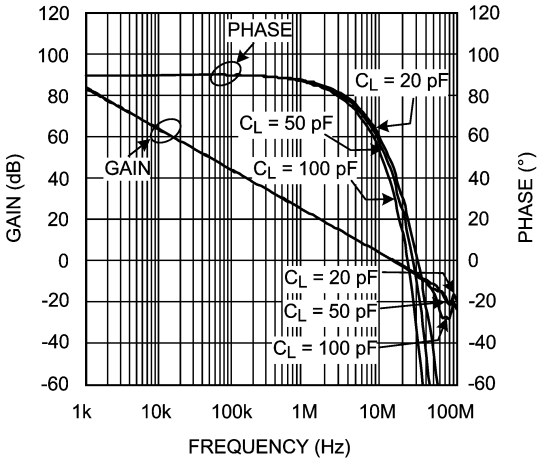
Typical Performance Characteristics Unless otherwise noted: T_A = 25˚C, V_S = 5V, V_{CM} = 2.5V (Continued)

Open Loop Frequency Response



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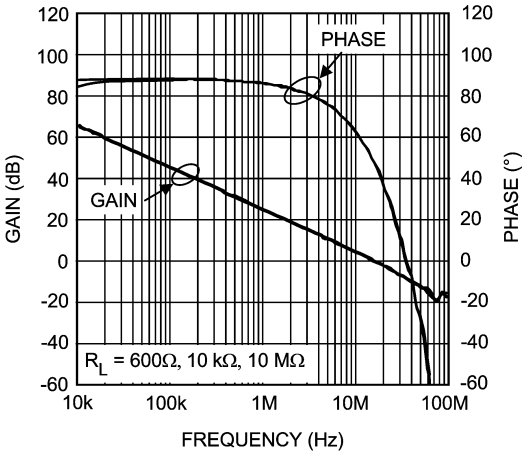
Open Loop Frequency Response



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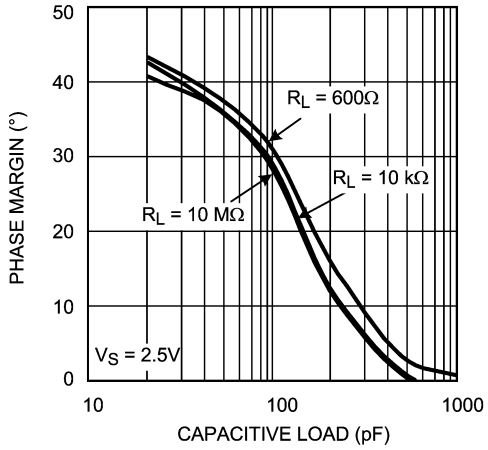
Phase Margin vs. Capacitive Load



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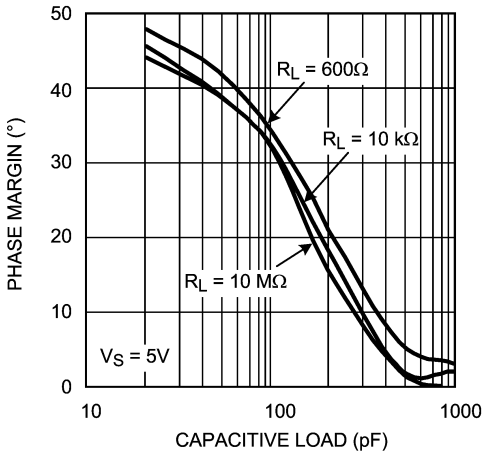
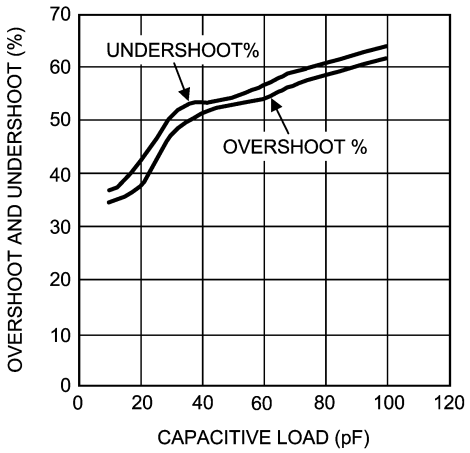
Phase Margin vs. Capacitive Load



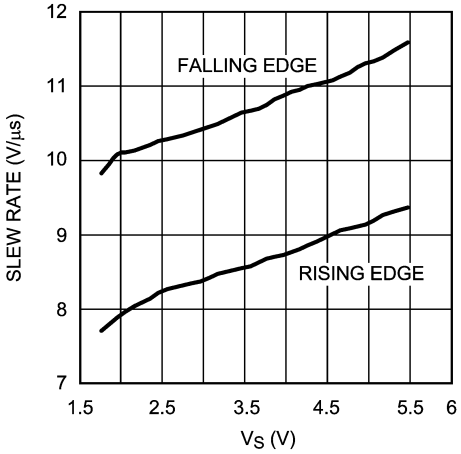
20150346

Overshoot and Undershoot vs. Capacitive Load



20150330

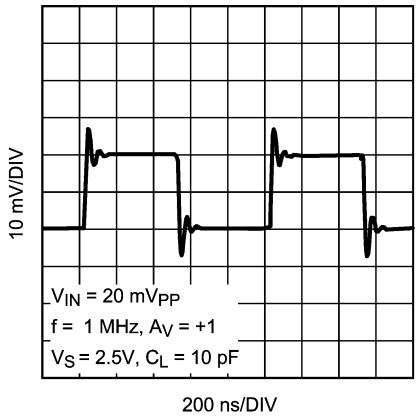
Slew Rate vs. Supply Voltage



20150329

Typical Performance Characteristics Unless otherwise noted: T_A = 25˚C, V_S = 5V, V_{CM} = 2.5V (Continued)

Small Signal Step Response, A_V = +1



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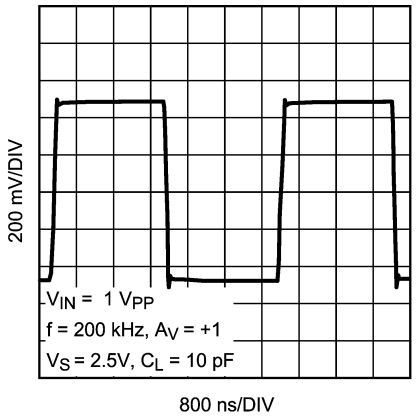
Large Signal Step Response, A_V = +1



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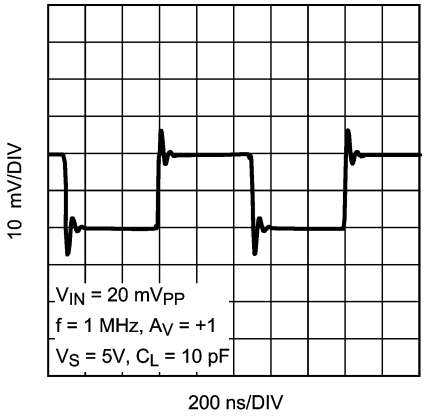
Small Signal Step Response, A_V = +1



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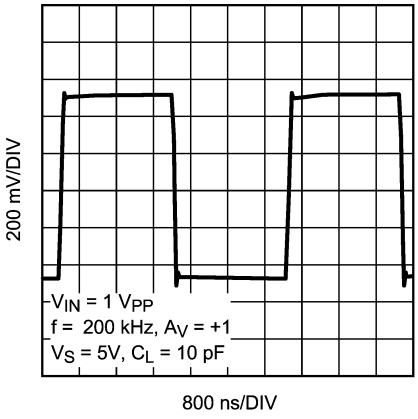
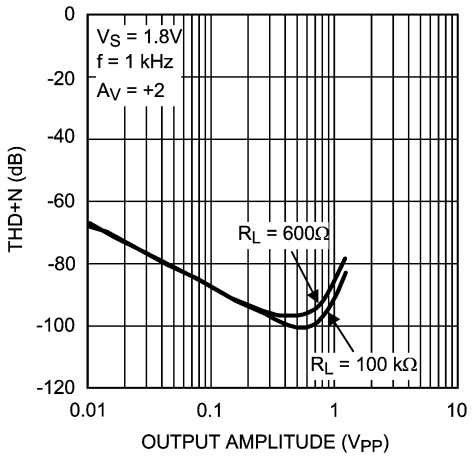
Large Signal Step Response, A_V = +1



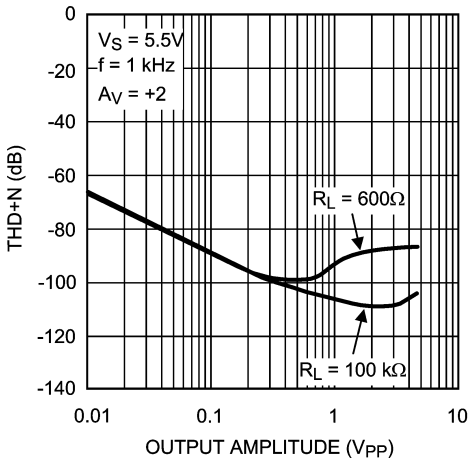
20150334

THD+N vs. Output Voltage



20150326

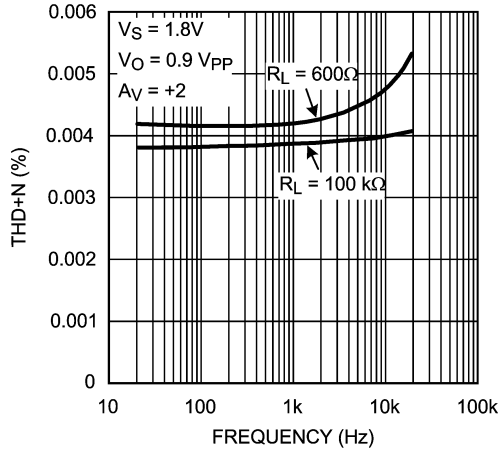
THD+N vs. Output Voltage



20150304

Typical Performance Characteristics Unless otherwise noted: T_A = 25˚C, V_S = 5V, V_{CM} = 2.5V (Continued)

THD+N vs. Frequency



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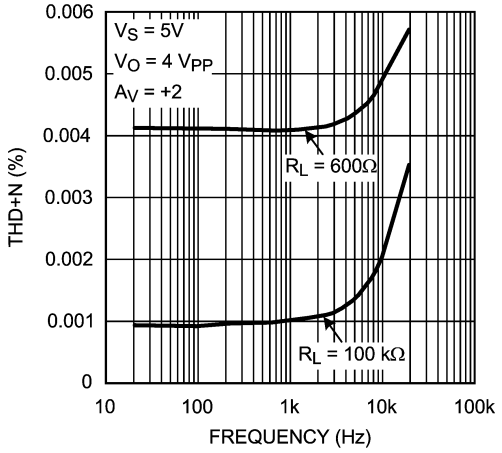
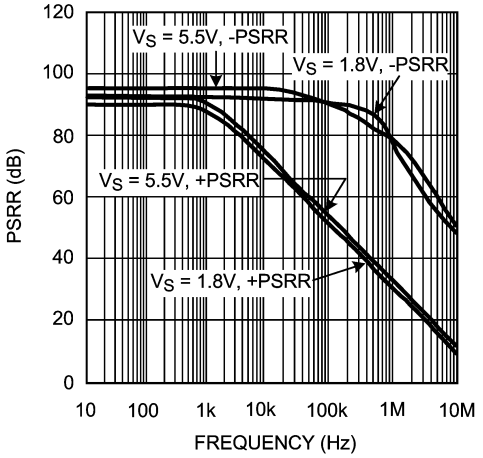
THD+N vs. Frequency



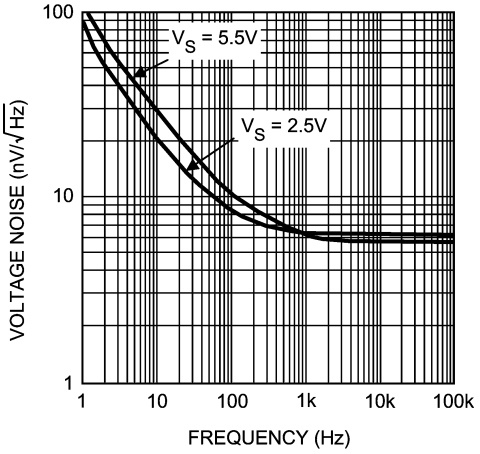
20150355

PSRR vs. Frequency



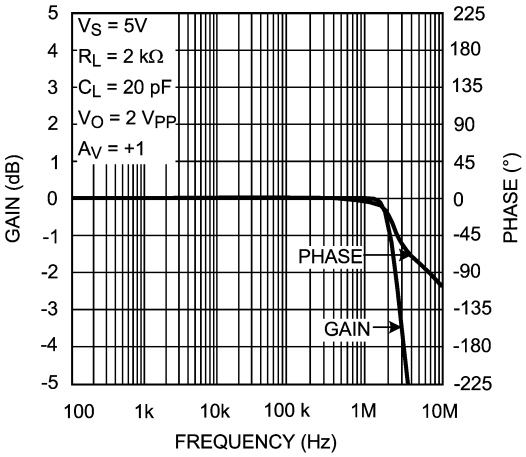
20150328

Input Referred Voltage Noise vs. Frequency



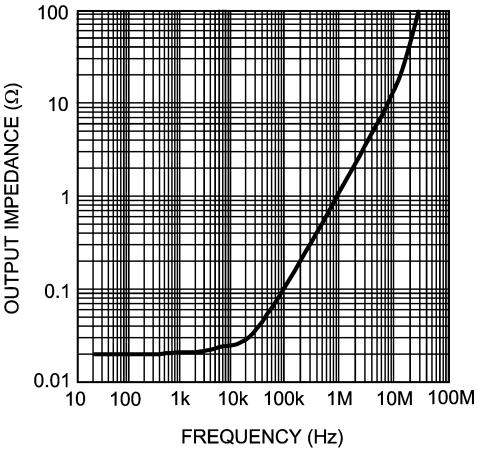
20150339

Closed Loop Frequency Response



20150336

Closed Loop Output Impedance vs. Frequency



20150332

Application Notes

LMP7711

The LMP7711 is a single, low noise, low offset, rail-to-rail output precision amplifier with a wide gain bandwidth product of 17 MHz and a low supply current of 1.15 mA. The wide bandwidth makes the LMP7711 an ideal choice for wideband amplification in portable applications. The low supply current along with the enable feature that is built-in on the LMP7711 allows for even more power efficient designs by turning the device off when not in use.

The LMP7711 is superior for sensor applications. The very low input referred voltage noise of only 5.8 nV/$\sqrt{\text{Hz}}$ at 1 kHz and very low input referred current noise of only 10 fA/$\sqrt{\text{Hz}}$ mean more signal fidelity and higher signal-to-noise ratios.

The LMP7711 has a supply voltage range of 1.8V to 5.5V over a wide temperature range of 0˚C to 125˚C. This is optimal for low voltage commercial applications. For applications where the ambient temperature might be less than 0˚C, the LMP7711 is fully operational at supply voltages of 2.0V to 5.5V over the temperature range of −40˚C to 125˚C.

The output of the LMP7711 swings within 25 mV of either rail providing maximum dynamic range in applications requiring low supply voltage. The input common mode range of the LMP7711 extends to 300 mV below ground. This feature enables users to utilize this device in single supply applications.

The use of a very innovative feedback topology has enhanced the current drive capability of the LMP7711, resulting in sourcing currents as much as 47 mA with a supply voltage of only 1.8V.

National Semiconductor is heavily committed to precision amplifiers and the market segments it serves. Technical support and extensive characterization data is available for sensitive applications or applications with constrained error budget.

The LMP7711 is offered in the space saving TSOT23 package. This small package is an ideal solution for applications requiring minimum PC board footprint.

CAPACITIVE LOAD

The unity gain follower is the most sensitive configuration to capacitive loading. The combination of a capacitive load placed directly on the output of an amplifier along with the output impedance of the amplifier creates a phase lag which in turn reduces the phase margin of the amplifier. If phase margin is significantly reduced, the response will be either underdamped or it will oscillate.

The LMP7711 can directly drive capacitive loads of up to 120 pF without oscillating. To drive heavier capacitive loads, an isolation resistor, R_{ISO} in *Figure 1*, should be used. This resistor and C_L form a pole and hence delay the phase lag or increase the phase margin of the overall system. The larger the value of R_{ISO}, the more stable the output voltage will be. However, larger values of R_{ISO} result in reduced output swing and reduced output current drive.

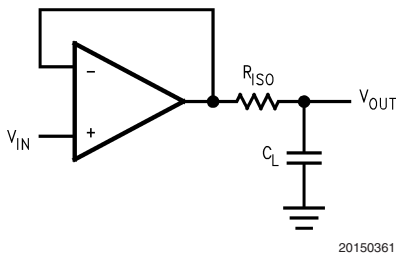


FIGURE 1.

INPUT CAPACITANCE

CMOS input stages inherently have low input bias current and higher input referred voltage noise. The LMP7711 enhances this performance by having the low input bias current of only 50 fA, as well as, a very low input referred voltage noise of 5.8 nV/$\sqrt{\text{Hz}}$. In order to achieve this a larger input stage has been used. This larger input stage increases the input capacitance of the LMP7711. This input capacitance will interact with other impedances such as gain and feedback resistors, which are seen on the inputs of the amplifier to form a pole. This pole will have little or no effect on the output of the amplifier at low frequencies and under DC conditions, but will play a bigger role as the frequency increases. At higher frequencies, the presence of this pole will decrease phase margin and also causes gain peaking. In order to compensate for the input capacitance, care must be given in choosing feedback resistors. In addition to being selective in picking values for the feedback resistor, a capacitor can be added to the feedback path to increase stability.

The DC gain of the circuit shown in *Figure 2* is simply $-R_2/R_1$.

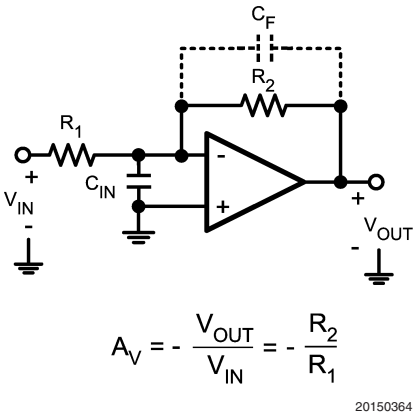


FIGURE 2.

For the time being, ignore C_F. The AC gain of the circuit in *Figure 2* can be calculated as follows:

$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{-R_2/R_1}{\left[1 + \frac{s}{\left(\frac{A_0 R_1}{R_1 + R_2}\right)} + \frac{s^2}{\left(\frac{A_0}{C_{IN} R_2}\right)}\right]} \quad (1)$$

Application Notes (Continued)

This equation is rearranged to find the location of the two poles:

$$P_{1,2} = \frac{-1}{2C_{IN}} \left[\frac{1}{R_1} + \frac{1}{R_2} \pm \sqrt{\left(\frac{1}{R_1} + \frac{1}{R_2} \right)^2 - \frac{4 A_0 C_{IN}}{R_2}} \right] \quad (2)$$

As shown in *Equation (2)*, as the values of R_1 and R_2 are increased, the magnitude of the poles are reduced, which in turn decreases the bandwidth of the amplifier. *Figure 3* shows the frequency response with different value resistors for R_1 and R_2. Whenever possible, it is best to chose smaller feedback resistors.

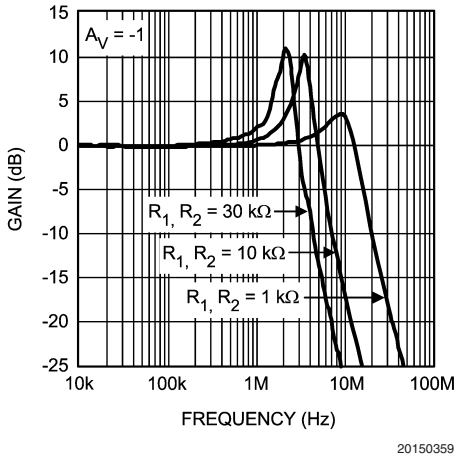


FIGURE 3.

As mentioned before, adding a capacitor to the feedback path will decrease the peaking. This is because C_F will form yet another pole in the system and will prevent pairs of poles, or complex conjugates, to form. It is the presence of pairs of poles that causes the peaking of gain. *Figure 4* shows the frequency response of the schematic presented in *Figure 2* with different values of C_F. As can be seen, using a small value capacitor significantly reduces or eliminates the peaking.

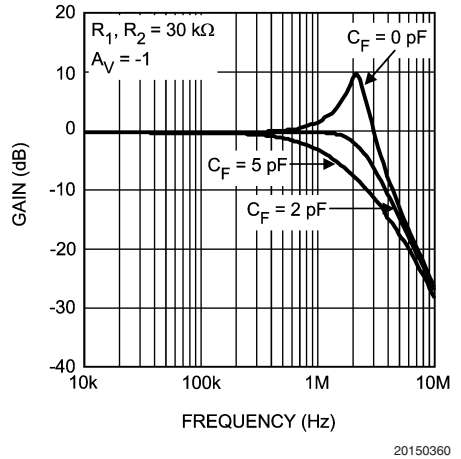


FIGURE 4.

TRANSIMPEDANCE AMPLIFIER

In many applications, the signal of interest is a very small amount of current that needs to be detected. Current that is transmitted through a photodiode is a good example. Barcode scanners, light meters, fiber optic receivers, and industrial sensors are some typical applications utilizing photodiodes for current detection. This current needs to be amplified before it can be further processed. This amplification is performed using a current-to-voltage converter configuration or transimpedance amplifier. The signal of interest is fed to the inverting input of an op amp with a feedback resistor in the current path. The voltage at the output of this amplifier will be equal to the negative of the input current times the value of feedback resistor. *Figure 5* shows a transimpedance amplifier configuration. C_D represents the photodiode parasitic capacitance and C_{CM} denotes the common-mode capacitance of the amplifier. The presence of all of these capacitances at higher frequencies might lead to less stable topologies at higher frequencies. Care must be given when designing a transimpedance amplifier to prevent the circuit from oscillating.

With a wide gain bandwidth product, low input bias current and low input voltage and current noise, the LMP7711 is ideal for wideband transimpedance applications.

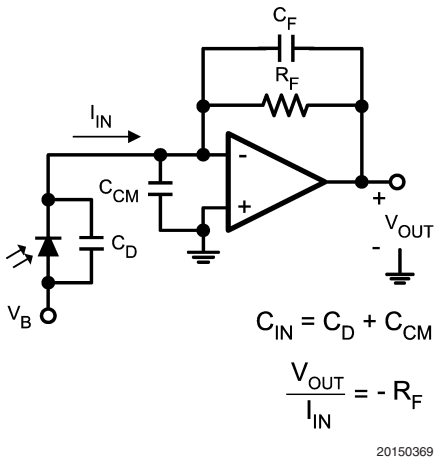


FIGURE 5.

A feedback capacitance C_F is usually added in parallel with R_F to maintain circuit stability and control the frequency response. To achieve a maximally flat, 2nd order response, R_F and C_F should be chosen by using *Equation (3)*

$$C_F = \sqrt{\frac{C_{IN}}{GBWP * 2 \pi R_F}} \quad (3)$$

Application Notes (Continued)

Calculating C_F from *Equation (3)* can sometimes result in capacitor values which are less than 2 pF. This is especially the case for high speed applications. In these instances, its often more practical to use the circuit shown in *Figure 6* in order to allow more sensible choices for C_F. The new feedback capacitor, C'_F, is $(1+ R_B/R_A)\ C_F$. This relationship holds as long as $R_A << R_F$.

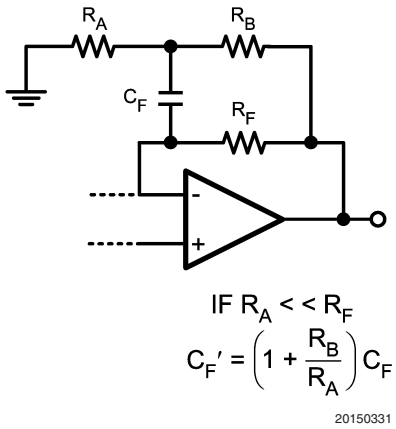


FIGURE 6.

SENSOR INTERFACE

The LMP7711 has low input bias current and low input referred noise, which make it an ideal choice for sensor interfaces such as thermopiles, Infra Red (IR) thermometry, thermocouple amplifiers, and pH electrode buffers.

Thermopiles generate voltage in response to receiving radiation. These voltages are often only a few micro volts, with currents less than one nano Amperes. As a result, the operational amplifier used for this application needs to have low voltage noise and low input bias current. *Figure 7* shows a thermopile application where the sensor detects a radiation in a distance and generates a voltage that is proportional to the intensity of the radiation. The two resistors, R_A and R_B, are selected to provide high gain to amplify this signal, while C_F removes the high frequency noise.

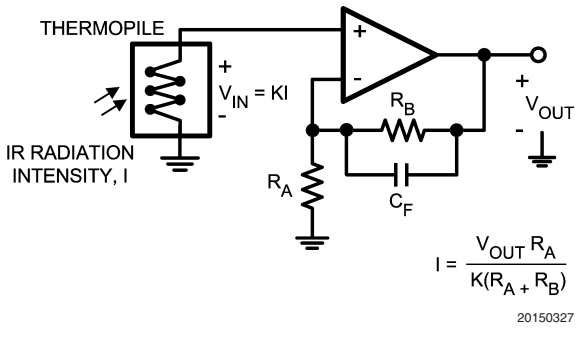


FIGURE 7.

PRECISION RECTIFIER

Rectifiers are electrical circuits used for converting AC signals to DC signals. *Figure 8* shows a full-wave precision rectifier. Each operational amplifier used in this circuit has a diode on its output. This means for the diodes to conduct, the output of the amplifier needs to be positive with respect to ground. If V_{IN} is in its positive half cycle then only the output of the bottom amplifier will be positive. As a result, the diode on the output of the bottom amplifier will conduct and the signal will show at the output of the circuit. If V_{IN} is in its negative half cycle then the output of the top amplifier will be positive, resulting in the diode on the output of the top amplifier conducting and, delivering the signal on the amplifier's output to the circuits output.

For $R_2/ R_1 \geq 2$, the resistor values can be found by using the equation shown in *Figure 8*. If $R_2/ R_1 = 1$, then R_3 should be left open, no resistor needed, and R_4 should be simply shorted.

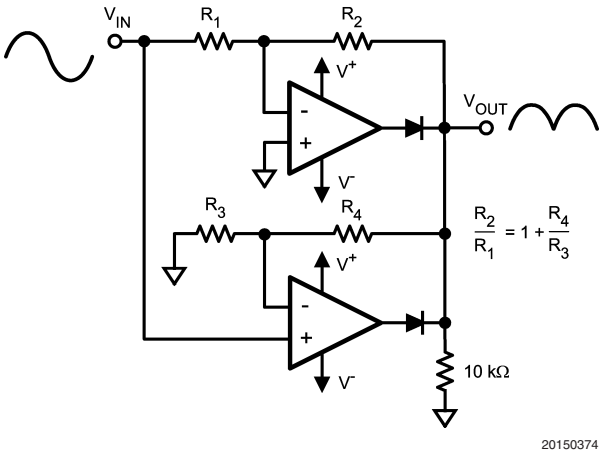
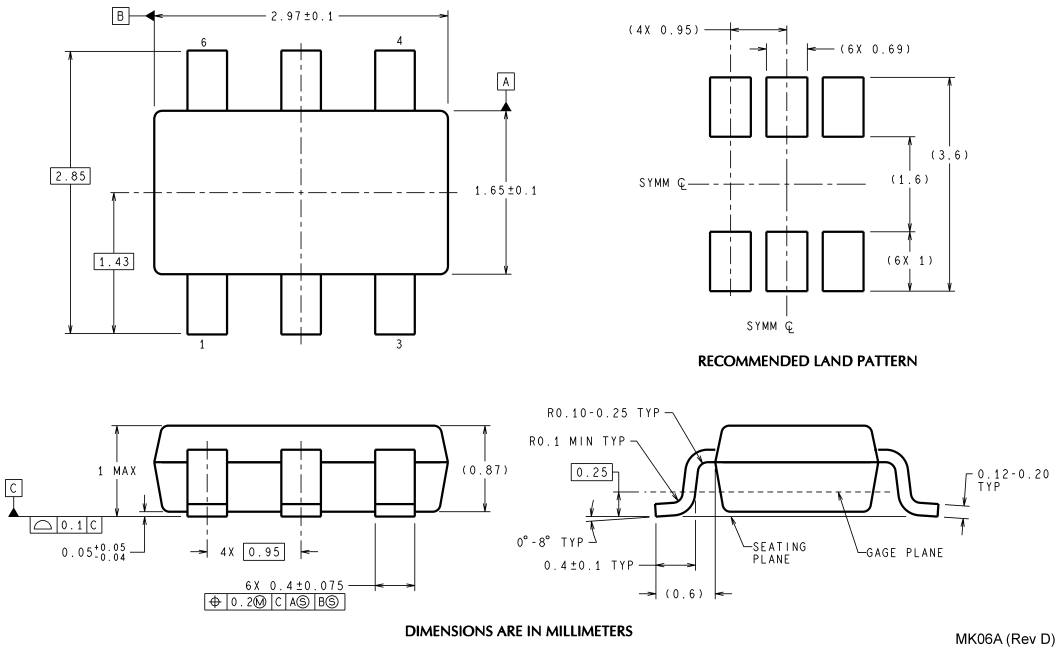


FIGURE 8.

Physical Dimensions inches (millimeters) unless otherwise noted



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