National Semiconductor

November 2005

LMH6702QML
1.7 GHz, Ultra Low Distortion, Wideband Op Amp

General Description

The LMH6702 is a very wideband, DC coupled monolithic operational amplifier designed specifically for wide dynamic range systems requiring exceptional signal fidelity. Benefiting from National's current feedback architecture, the LMH6702 offers unity gain stability at exceptional speed without need for external compensation.

With its 720MHz bandwidth (A_V = 2V/V, V_O = $2V_{PP}$), 10-bit distortion levels through 60MHz (R_L = 100Ω), 1.83nV/ $\sqrt{Hz}$ input referred noise and 12.5mA supply current, the LMH6702 is the ideal driver or buffer for high-speed flash A/D and D/A converters.

Wide dynamic range systems such as radar and communication receivers, requiring a wideband amplifier offering exceptional signal purity, will find the LMH6702's low input referred noise and low harmonic and intermodulation distortion make it an attractive high speed solution.

The LMH6702 is constructed using National's VIP10™ complimentary bipolar process and National's proven current feedback architecture.

Features

V_S = ±5V, T_A = 25˚C, A_V = +2V/V, R_L = 100Ω, V_{OUT} = $2V_{PP}$, Typical unless Noted:

- Available with radiation guarantee
- −3dB Bandwidth (V_{OUT} = 0.2 V_{PP}) 720 MHz
- Low noise 1.83nV/ $\sqrt{Hz}$
- Fast settling to 0.1% 13.4ns
- Fast slew rate 3100V/µs
- Supply current 12.5mA
- Output current 80mA
- Low Intermodulation Distortion (75MHz) −67dBc
- Improved Replacement for CLC409 and CLC449

Applications

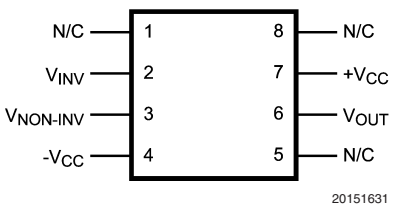
- Flash A/D driver
- D/A transimpedance buffer
- Wide dynamic range IF amp
- Radar/communication receivers
- Line driver
- High resolution video

Ordering Information

NS PART NUMBER	SMD PART NUMBER	NS PACKAGE NUMBER	PACKAGE DISCRIPTION
LMH6702J-QML	5962−0254601QPA	J08A	8LD CERDIP
LMH6702WG-QML	5962−0254601QZA	WG10A	10LD CERAMIC SOIC
LMH6702J-QMLV	5962−0254601VPA	J08A	8LD CERDIP
LMH6702WG-QMLV	5962−0254601VZA	WG10A	10LD CERAMIC SOIC
LMH6702JFQMLV	5962F0254601VPA 300k rd(Si)	J08A	8LD CERDIP
LMH6702WGFQMLV	5962F0254601VZA 300k rd(Si)	WG10A	10LD CERAMIC SOIC

Connection Diagrams

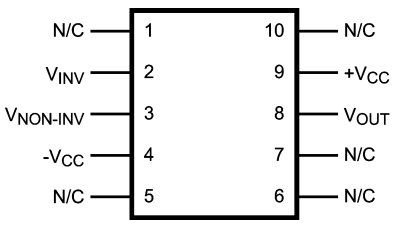
8 Lead Cerdip (J)



20151631

Top View
See NS Package Number J08A

10 Lead Ceramic SOIC (WG)



20151632

Top View
See NS Package Number WG10A

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	$\pm 6.75V_{DC}$
Common Mode Input Voltage (V_{CM})	V^- to V^+
Power Dissipation (P_D) (Note 2)	1W
Junction Temperature (T_J)	+175˚C
Lead Temperature (soldering, 10 seconds)	+300˚C
Storage Temperature Range	$-65˚C \leq T_A \leq +150˚C$
Thermal Resistance	
θ_{JA}	
Cerdip (Still Air)	170˚C/W
Cerdip (500LF/Min Air Flow)	100˚C/W
Ceramic SOIC (Still Air)	220˚C/W
Ceramic SOIC (500LF/Min Air Flow)	150˚C/W
θ_{JC}	
Cerdip	35˚C/W
Ceramic SOIC	37˚C/W
Package Weight (Typical)	
Cerdip	1078mg
Ceramic SOIC	227mg
ESD Tolerance (Note 3)	1000V

Recommended Operating Conditions

Supply Voltage (V_{CC})	$\pm 5V_{DC}$ to $\pm 6V_{DC}$
Gain Range	±1 to ±10
Ambient Operating Temperature Range (T_A)	-55˚C to +125˚C

Quality Conformance Inspection

MIL-STD-883, Method 5005, Group A

Subgroup	Description	Temp (C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

LMH6702 Electrical Characteristics

DC Parameters (Note 4), (Note 5)

The following conditions apply, unless otherwise specified.

R_L = 100Ω, V_{CC} = ±5V_{DC}, A_V = +2 feedback resistor (R_F) = 250Ω, gain resistor (R_G) = 250Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{BN}	Input Bias Current, Noninverting			-15	+15	µA	1, 2
				-21	+21	µA	3
I_{BI}	Input Bias Current, Iverting			-30	+30	µA	1, 2
				-34	+34	µA	3
V_{IO}	Input Offset Voltage			-4.5	+4.5	mV	1, 3
				-6.0	+6.0	mV	2
I_{CC}	Supply Current, no load	R_L = ∞			15	mA	1, 2, 3
PSSR	Power Supply Rejection Ratio	-V_{CC} = -4.5V to -5.0V, +V_{CC} = +4.5V to +5.0V		45		dB	1, 2, 3

AC Parameters (Note 4), (Note 5)

The following conditions apply, unless otherwise specified.

R_L = 100Ω, V_{CC} = ±5V_{DC}, A_V = +2 feedback resistor (R_F) = 250Ω, gain resistor (R_G) = 250Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
HD_3	3rd Harmonic Distortion	2V_{PP} at 20MHz	(Note 6)		-62	dBc	4
GFPL	Gain Flatness Peaking	0.1MHz to 75MHz, V_O < 0.5V_{PP}	(Note 6)		0.4	dB	4
GFPH	Gain Flatness Peaking	> 75MHz, V_O < 0.5V_{PP}	(Note 6)		2.0	dB	4
GFRH	Gain Flatness Rolloff	75MHz to 125MHz, V_O<0.5V_{PP}	(Note 6)		0.2	dB	4
HD_2	2nd Harmonic Distortion	2V_{PP} at 20MHz	(Note 6)		-52	dBc	4

Drift Values Parameters (Note 4)

The following conditions apply, unless otherwise specified.

R_L = 100Ω, V_{CC} = ±5V_{DC}, A_V = +2 feedback resistor (R_F) = 250Ω, gain resistor (R_G) = 250Ω "Delta not required on B level product. Delta required for S-level product at Group B5 only, or as specified on the Internal Processing Instruction (IPI)."

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{BN}	Input Bias Current Noninverting			-0.3	+0.3	µA	1
I_{BI}	Input Bias Current Inverting			-3.0	+3.0	µA	1
V_{IO}	Input Offset Voltage			-0.3	+0.3	mV	1

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

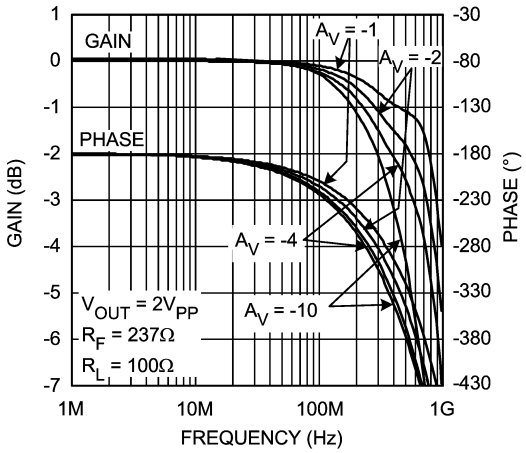
Note 3: Human body model, 1.5kΩ in series with 100pF.

Note 4: The algebraic convention, whereby the most negative value is a minimum and most positive is a maximum, is used in this table. Negative cur rent shall be defined as convential current flow out of a device terminal.

Note 5: Pre and Post irradiation limits, up to 300k rd(Si) total ionizing dose, are identical to those listed under the AC and DC parameter tables above. Post irradiation testing is conducted at room temperature, +25˚C, only. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, Method 1019.

Note 6: This parameter is not post irradiation tested.

Inverting Frequency Response

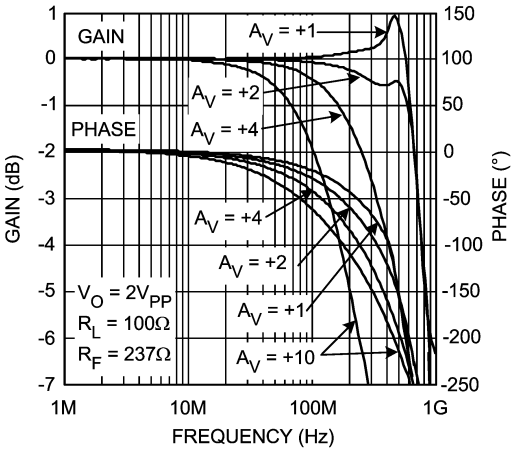


20151602

Typical Performance Characteristics

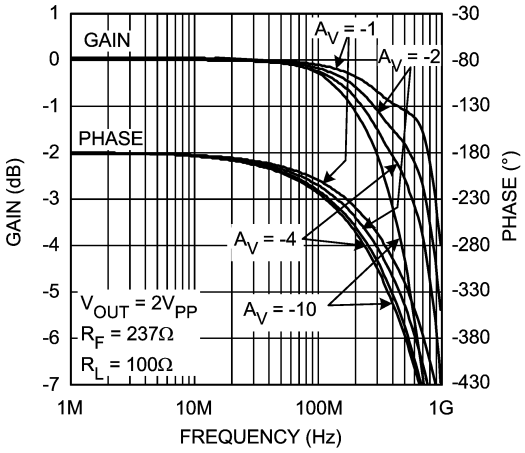
(T_A = 25˚C, V_S = ±5V, R_L = 100Ω, R_F = 237Ω; Unless Specified).

Non-Inverting Frequency Response



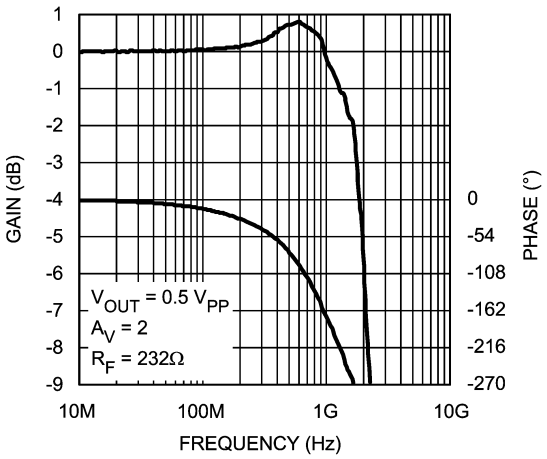
20151601

Inverting Frequency Response



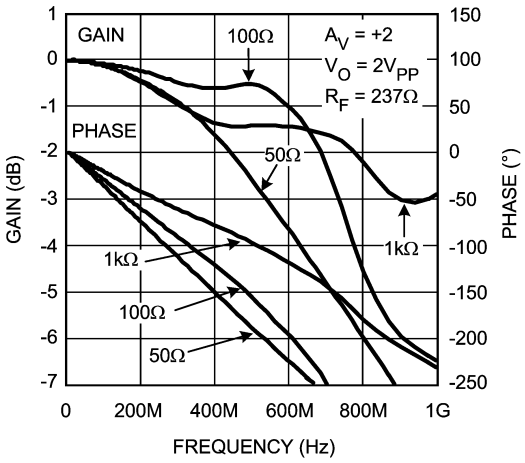
20151602

Small Signal Bandwidth



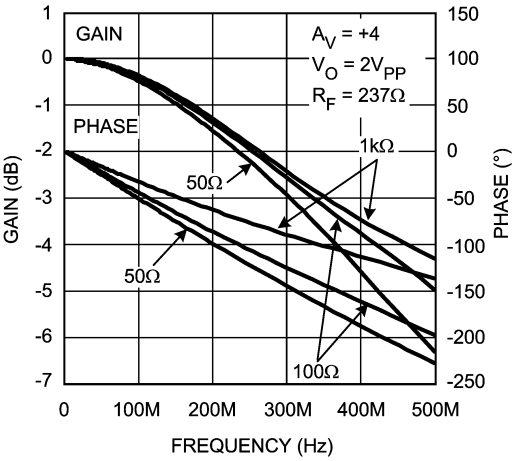
20151630

Frequency Response for Various R_L's, A_V = +2



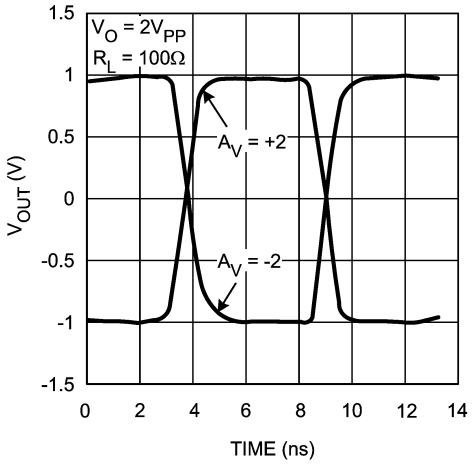
20151618

Frequency Response for Various R_L's, A_V = +4



20151617

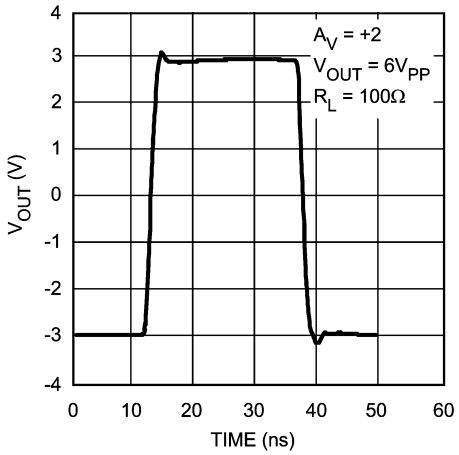
Step Response, $2V_{PP}$



20151605

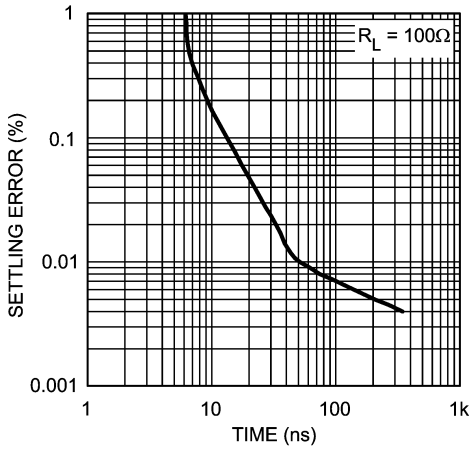
Typical Performance Characteristics (T_A = 25˚C, V_S = ±5V, R_L = 100Ω, R_F = 237Ω; Unless Specified). (Continued)

Step Response, $6V_{PP}$



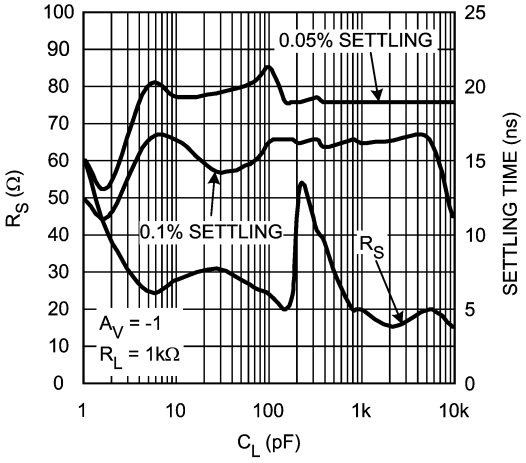
20151606

Percent Settling vs. Time



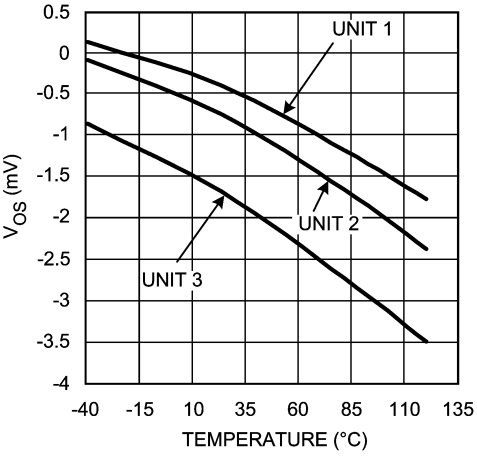
20151620

R_S and Settling Time vs. C_L



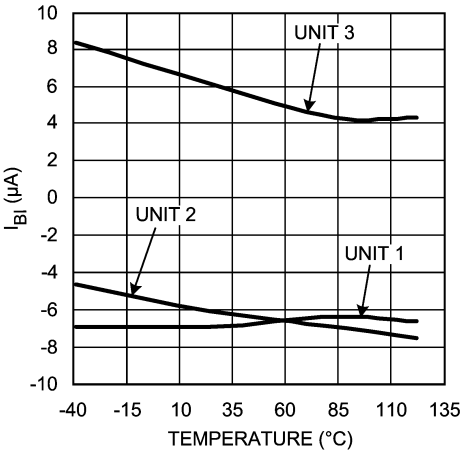
20151613

Input Offset for 3 Representative Units



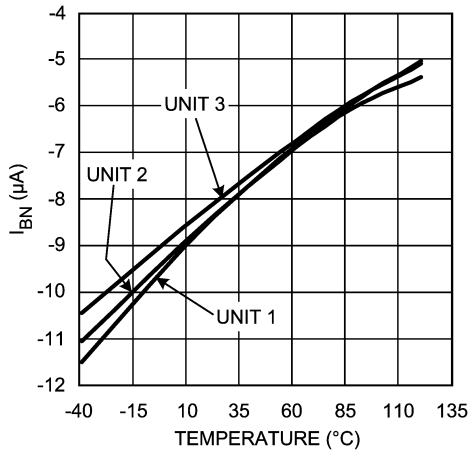
20151614

Inverting Input Bias for 3 Representative Units



20151615

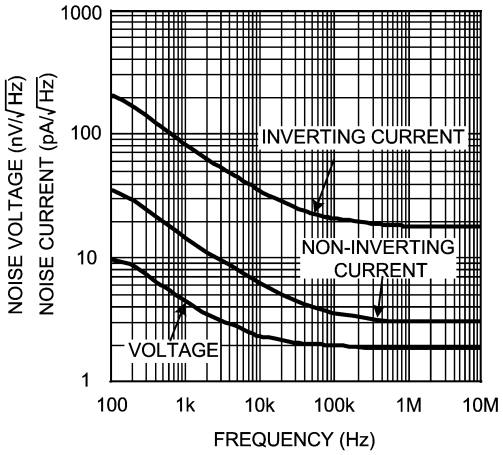
Non-Inverting Input Bias for 3 Representative Units



20151616

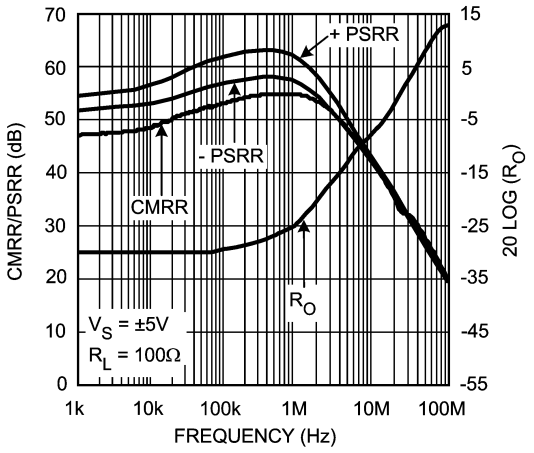
Typical Performance Characteristics (T_A = 25˚C, V_S = ±5V, R_L = 100Ω, R_F = 237Ω; Unless Specified). (Continued)

Noise



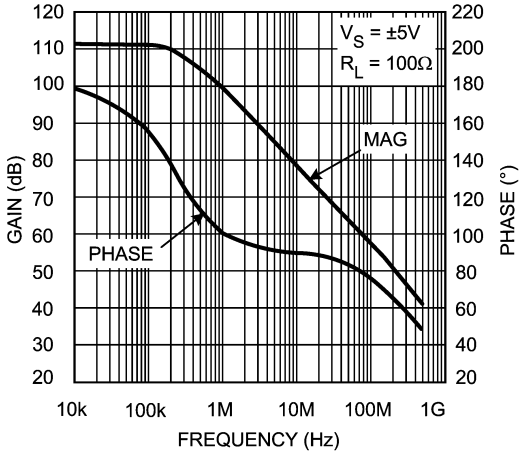
20151612

CMRR, PSRR, R_{OUT}



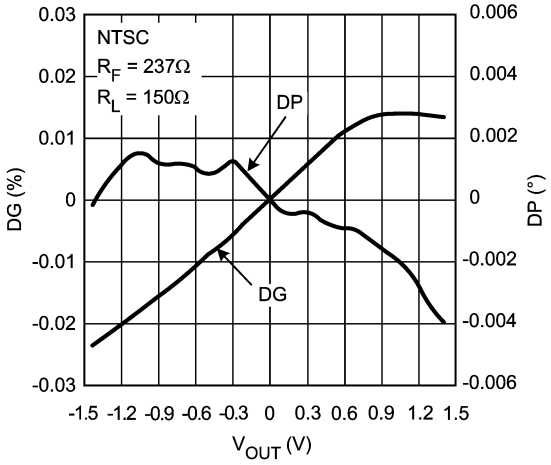
20151619

Transimpedance



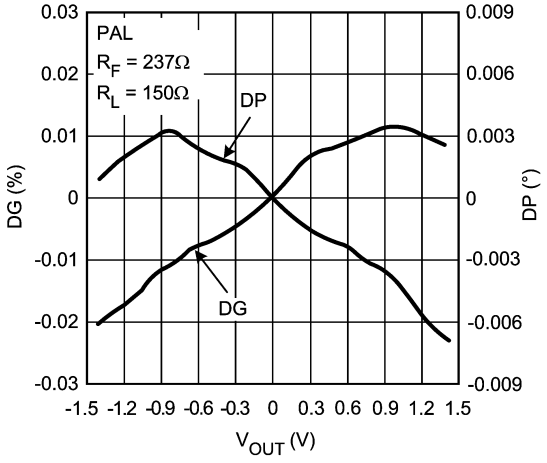
20151611

DG/DP (NTSC)



20151604

DG/DP (PAL)



20151603

Application Section

FEEDBACK RESISTOR

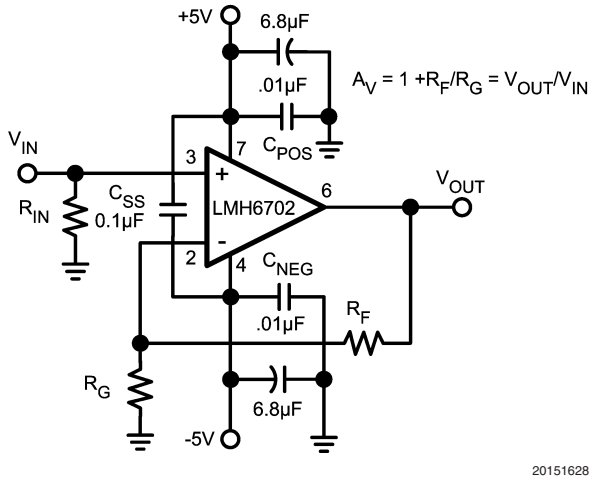


FIGURE 1. Recommended Non-Inverting Gain Circuit

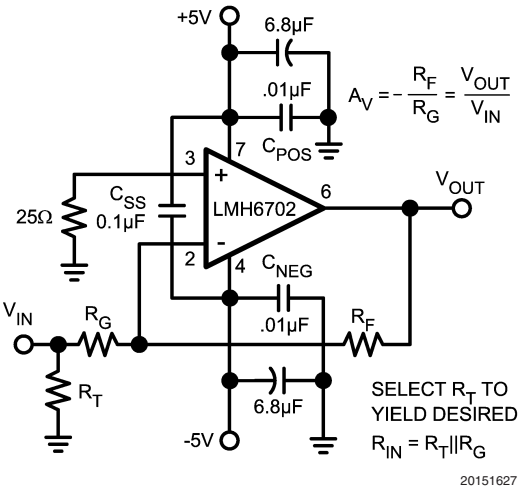


FIGURE 2. Recommended Inverting Gain Circuit

The LMH6702 achieves its excellent pulse and distortion performance by using the current feedback topology. The loop gain for a current feedback op amp, and hence the frequency response, is predominantly set by the feedback resistor value. The LMH6702 is optimized for use with a 237Ω feedback resistor. Using lower values can lead to excessive ringing in the pulse response while a higher value will limit the bandwidth. Application Note OA-13 discusses this in detail along with the occasions where a different R_F might be advantageous.

HARMONIC DISTORTION

The LMH6702 has been optimized for exceptionally low harmonic distortion while driving very demanding resistive or capacitive loads. Generally, when used as the input amplifier to very high speed flash ADCs, the distortions introduced by the converter will dominate over the low LMH6702 distortions. The capacitor C_{SS}, shown across the supplies in *Figure 1* and *Figure 2*, is critical to achieving the lowest 2nd harmonic distortion. For absolute minimum distortion levels, it is also advisable to keep the supply decoupling currents (ground connections to C_{POS}, and C_{NEG} in *Figure 1* and *Figure 2*) separate from the ground connections to sensitive input circuitry (such as R_G, R_T, and R_{IN} ground connections). Splitting the ground plane in this fashion and separately routing the high frequency current spikes on the decoupling caps back to the power supply (similar to "Star Connection" layout technique) ensures minimum coupling back to the input circuitry and results in best harmonic distortion response (especially 2nd order distortion).

If this lay out technique has not been observed on a particular application board, designer may actually find that supply decoupling caps could adversely affect HD2 performance by increasing the coupling phenomenon already mentioned. *Figure 3* below shows actual HD2 data on a board where the ground plane is "shared" between the supply decoupling capacitors and the rest of the circuit. Once these capacitors are removed, the HD2 distortion levels reduce significantly, especially between 10MHz-20MHz, as shown in *Figure 3* below:

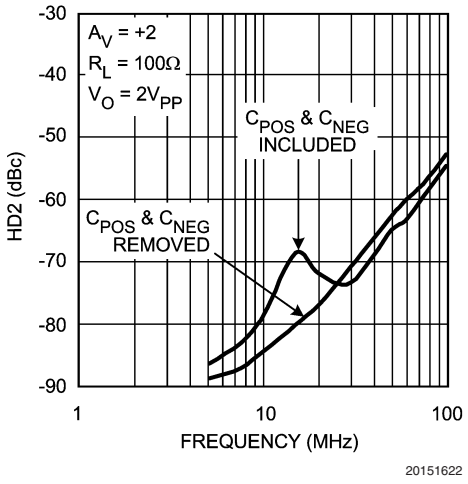


FIGURE 3. Decoupling Current Adverse Effect on a Board with Shared Ground Plane

At these extremely low distortion levels, the high frequency behavior of decoupling capacitors themselves could be significant. In general, lower value decoupling caps tend to have higher resonance frequencies making them more effective for higher frequency regions. A particular application board which has been laid out correctly with ground returns "split" to minimize coupling, would benefit the most by having low value and higher value capacitors paralleled to take advantage of the effective bandwidth of each and extend low distortion frequency range.

Application Section (Continued)

CAPACITIVE LOAD DRIVE

Figure 4 shows a typical application using the LMH6702 to drive an ADC.

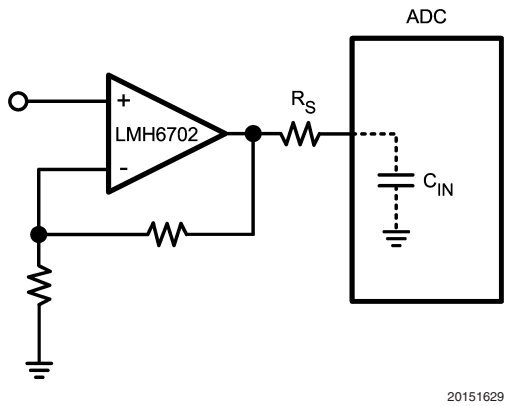


FIGURE 4. Input Amplifier to ADC

The series resistor, R_S, between the amplifier output and the ADC input is critical to achieving best system performance. This load capacitance, if applied directly to the output pin, can quickly lead to unacceptable levels of ringing in the pulse response. The plot of "R_S and Settling Time vs. C_L" in the Typical Performance Characteristics section is an excellent starting point for selecting R_S. The value derived in that plot minimizes the step settling time into a fixed discrete capacitive load with the output driving a very light resistive load (1kΩ). Sensitivity to capacitive loading is greatly reduced once the output is loaded more heavily. Therefore, for cases where the output is heavily loaded, R_S value may be reduced. The exact value may best be determined experimentally for these cases.

In applications where the LMH6702 is replacing the CLC409, care must be taken when the device is lightly loaded and some capacitance is present at the output. Due to the much higher frequency response of the LMH6702 compared to the CLC409, there could be increased susceptibility to low value output capacitance (parasitic or inherent to the board layout or otherwise being part of the output load). As already mentioned, this susceptibility is most noticeable when the LMH6702's resistive load is light. Parasitic capacitance can be minimized by careful lay out. Addition of an output snubber R-C network will also help by increasing the high frequency resistive loading.

Referring back to *Figure 4*, it must be noted that several additional constraints should be considered in driving the capacitive input of an ADC. There is an option to increase R_S, band-limiting at the ADC input for either noise or Nyquist band-limiting purposes. Increasing R_S too much, however, can induce an unacceptably large input glitch due to switching transients coupling through from the "convert" signal. Also, C_{IN} is oftentimes a voltage dependent capacitance. This input impedance non-linearity will induce distortion terms that will increase as R_S is increased. Only slight adjustments up or down from the recommended R_S value should therefore be attempted in optimizing system performance.

Application Section (Continued)

DC ACCURACY AND NOISE

Example below shows the output offset computation equation for the non-inverting configuration using the typical bias current and offset specifications for A_V = + 2:

Output Offset : $V_O = (\pm I_{BN} \cdot R_{IN} \pm V_{IO}) (1 + R_F/R_G) \pm I_{BI} \cdot R_F$

Where R_{IN} is the equivalent input impedance on the non-inverting input.

Example computation for A_V = +2, R_F = 237Ω, R_{IN} = 25Ω:

$V_O = (\pm 6\mu A \cdot 25\Omega \pm 1mV) (1 + 237/237) \pm 8\mu A \cdot 237 = \pm 4.20mV$

A good design, however, should include a worst case calculation using Min/Max numbers in the data sheet tables, in order to ensure "worst case" operation.

Further improvement in the output offset voltage and drift is possible using the composite amplifiers described in Application Note OA-7. The two input bias currents are physically unrelated in both magnitude and polarity for the current feedback topology. It is not possible, therefore, to cancel their effects by matching the source impedance for the two inputs (as is commonly done for matched input bias current devices).

The total output noise is computed in a similar fashion to the output offset voltage. Using the input noise voltage and the two input noise currents, the output noise is developed through the same gain equations for each term but combined as the square root of the sum of squared contributing elements. See Application Note OA-12 for a full discussion of noise calculations for current feedback amplifiers.

PRINTED CIRCUIT LAYOUT

Generally, a good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 for more information). National Semiconductor suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

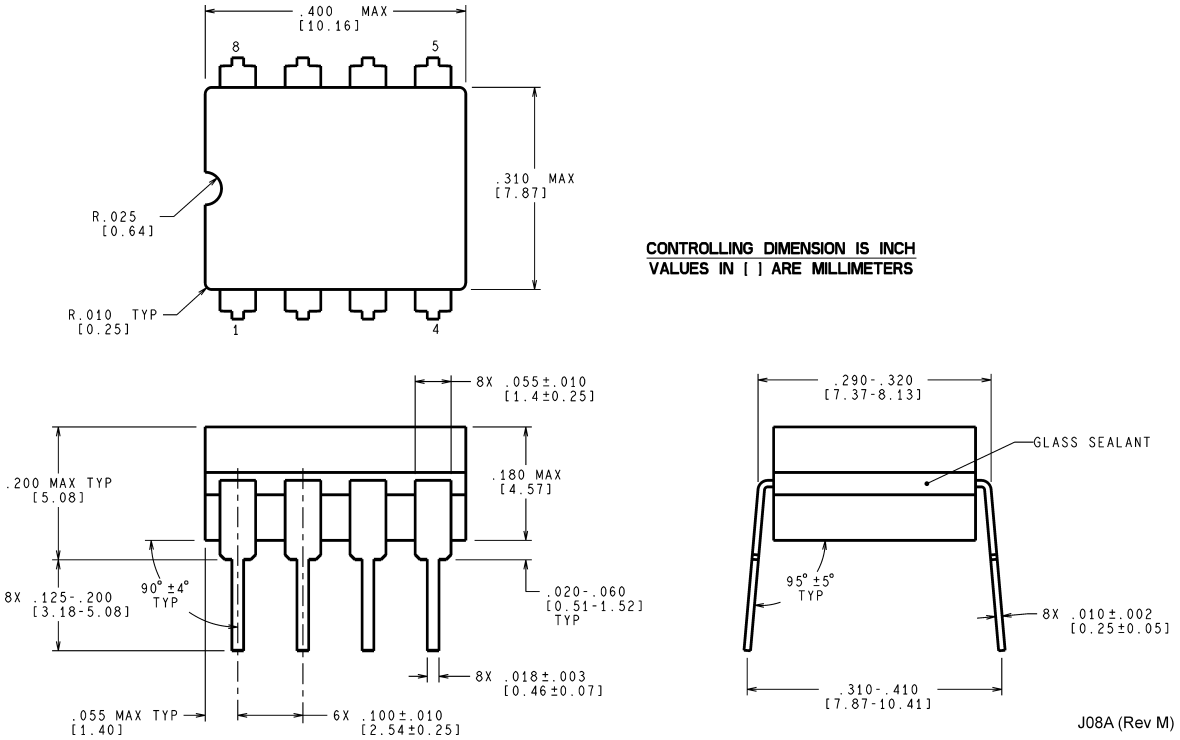
Device	Package	Evaluation Board Part Number
LMH6702QMLMF	SOT23-5	CLC730216
LMH6702QMLMA	Plastic SOIC	CLC730227

These free evaluation boards are shipped when a device sample request is placed with National Semiconductor.

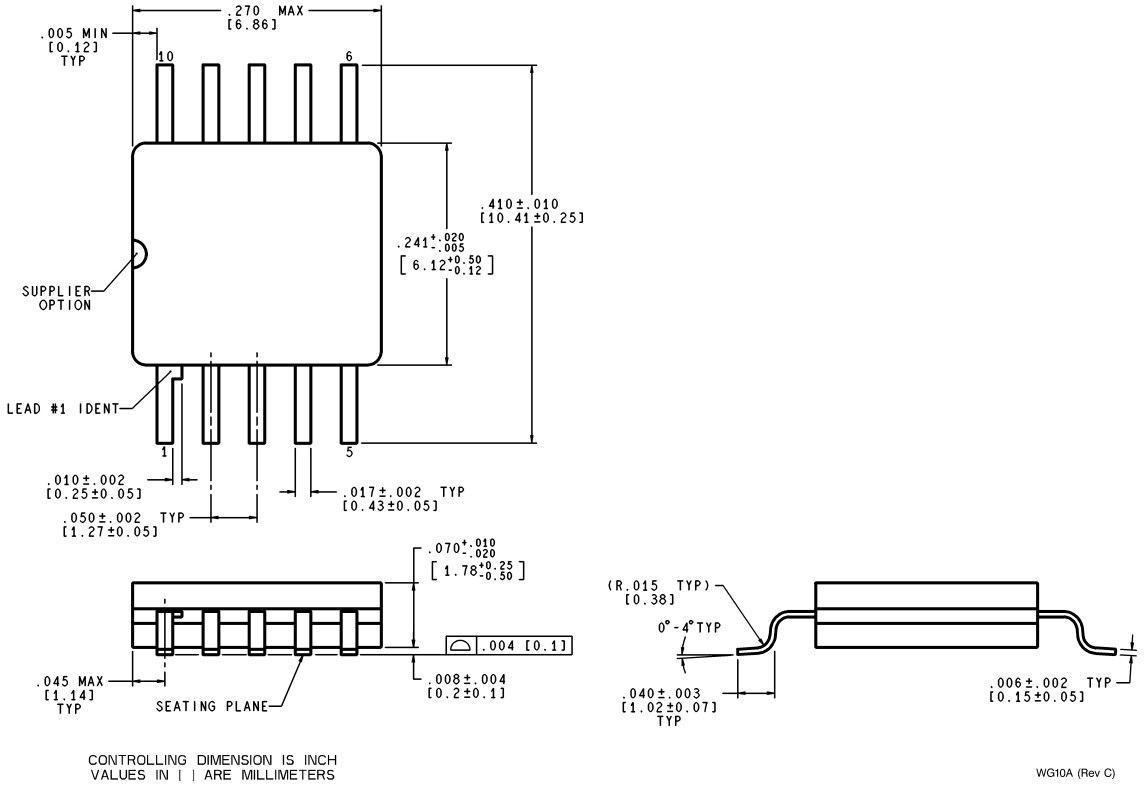
Revision History

Date Released	Revision	Section	Originator	Changes
07/12/05	A	New Corporate format Release	R. Malone	1 MDS data sheet converted in corporate data sheet format. Added reference to QMLV products and Drift Table. MDS MNLMH6702–X, Rev. 1A0 will be archived.
09/28/05	B	Features, Ordering Information Table and Notes	R. Malone	Added radiation reference to Features, Rad NSID & SMD to Ordering Table and Note 5 to AC & DC Electrical tables. Note 5 to note section.
11/07/05	C	Update AC electrical's and Notes	R. Malone	Added note 6 to AC electrical's and note section. LMH6702QML Revision B data sheet will be archived.

Physical Dimensions inches (millimeters) unless otherwise noted



8 Lead Cerdip (J)
NS Package Number J08A



10 Lead Ceramic SOIC
NS Package Number WG10A

Notes

National Semiconductor
Americas Customer
Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

www.national.com

National Semiconductor
Europe Customer Support Center
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer
Support Center
Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560