National Semiconductor

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LM9801
8-Bit Greyscale/24-Bit Color Linear CCD Sensor Processor

General Description

The LM9801 is a high performance integrated signal processor/digitizer for linear CCD image scanners. The LM9801 performs all the analog processing (correlated double sampling for black level and offset compensation, pixel-by-pixel gain (shading) correction, and 8-bit analog-to-digital conversion) necessary to maximize the performance of a wide range of linear CCD sensors.

The LM9801 can be digitally programmed to work with a wide variety of CCDs from different manufacturers. An internal configuration register sets CCD and sampling timing to maximize performance, simplifying the design and manufacturing processes.

The LM9801 can be used with parallel output color CCDs. A signal inversion mode eases use with CIS sensors. For complementary voltage reference see the LM4041.

Applications

- Color and Greyscale Flatbed and Sheetfed Scanners
- Fax and Multifunction Peripherals
- Digital Copiers
- General Purpose Linear CCD Imaging

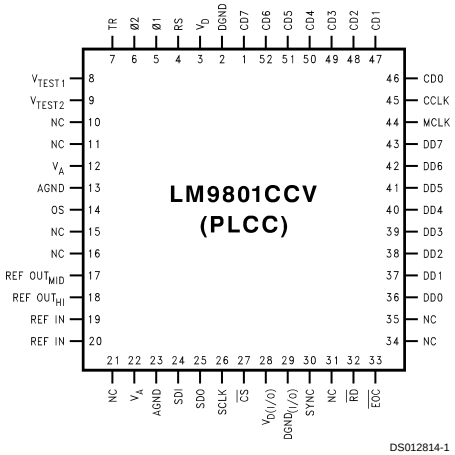
Features

- 2.5 Million pixels/s conversion rate
- Pixel-rate shading correction for individual pixels maximizes dynamic range and resolution, even on "weak" pixels
- Implements Correlated Double Sampling for minimum noise and offset error
- Reference and signal sampling points digitally controlled in 25 ns increments for maximum performance
- Generates all necessary CCD clock signals
- Compatible with a wide range of linear CCDs
- Supports some Contact Image Sensors (CIS)
- TTL/CMOS input/output compatible

Key Specifications

■ Resolution:	8 Bits
■ Pixel Conversion Rate:	2.5 MHz
■ Supply Voltage:	+5V ± 5%
■ Supply Voltage (Digital I/O):	+3.3V ± 10% or +5V ± 5%
■ Power Dissipation:	260 mW (max)

Connection Diagrams



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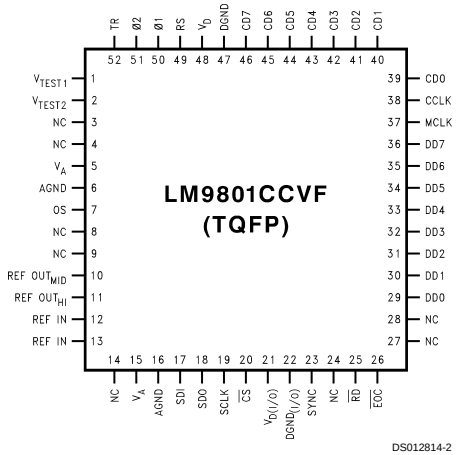

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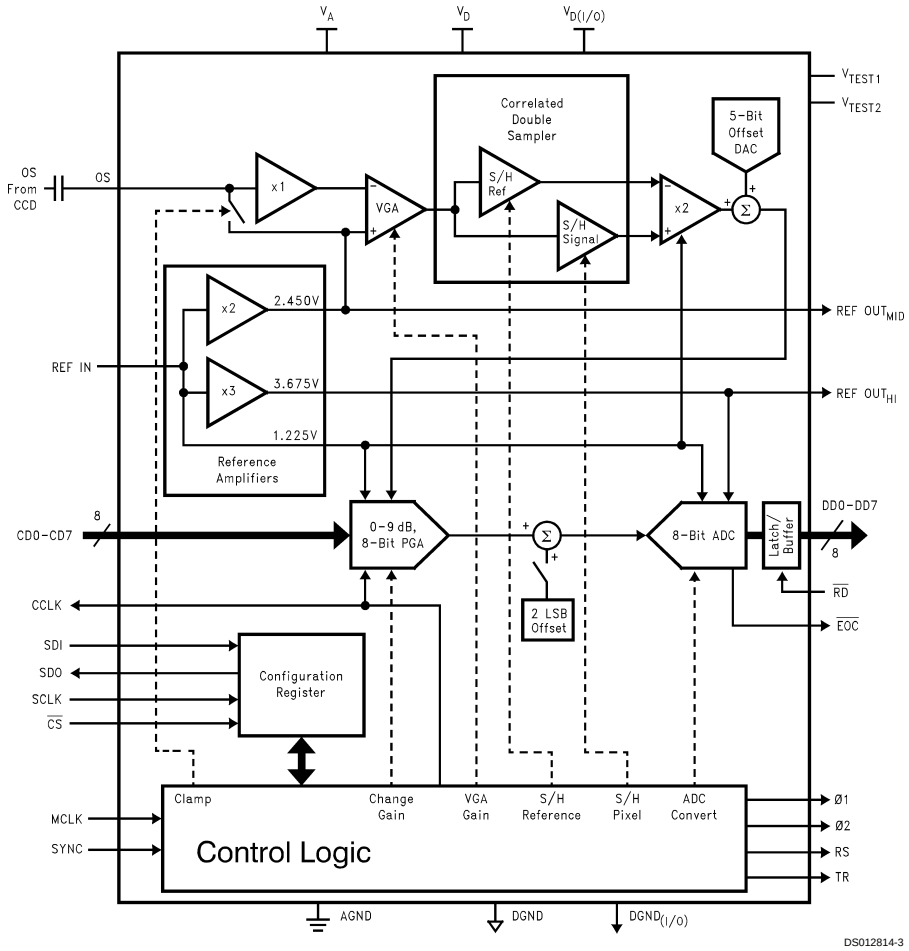
Block Diagram



Ordering Information

Commercial ($0^{\circ}C \leq T_A \leq +70^{\circ}C$)	Package
LM9801CCV	V52A 52-Pin Plastic Leaded Chip Carrier
LM9801CCVF	VEG52A 52-Pin Thin Quad Flatpack

Absolute Maximum Ratings (Notes 2, 1)

Positive Supply Voltage ($V^+ = V_A = V_D = V_{D(I/O)}$) with Respect to GND = AGND = DGND = $DGND_{(I/O)}$	6.5V
Voltage on any Input or Output Pin	0.3V to V^+ +0.3V
Input Current at any Pin (Note 3)	±25 mA
Package Input Current (Note 3)	±50 mA
Package Dissipation at T_A = 25˚C	(Note 4)
ESD Susceptibility (Note 5)	
Human Body Model	2000V
Soldering Information (Note 6)	
Infrared, 10 seconds	
LM9801CCV	300˚C
LM9801CCVF	220˚C
Storage Temperature	−65˚C to +150˚C

Operating Ratings (Notes 1, 2)

Operating Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LM9801CCV, LM9801CCVF	$0^\circ C \le T_A \le +70^\circ C$
V_A Supply Voltage	+4.75V to +5.25V
V_D Supply Voltage	+4.75V to +5.25V
$V_{D(I/O)}$ Supply Voltage	+2.7V to +5.25V
$\lvert V_A - V_D \rvert$	≤ 100 mV
$V_A - V_{D(I/O)}$	≥ −100 mV
OS, REF IN Voltage Range	−0.05V to V_A + 0.05V
CD0–CD7, MCLK, SYNC, SDI, SCLK, $\overline{CS}$, $\overline{RD}$ Voltage Range	−0.05V to $V_{D(I/O)}$ + 0.05V

Electrical Characteristics

The following specifications apply for AGND = DGND = DGND(I/O) = 0V, $V_A = V_D$ = +5.0V_{DC}, $V_{D(I/O)}$ = +5.0 or +3.0V_{DC}, REF IN = +1.225V_{DC}, f_{MCLK} = 20 MHz, R_S = 25Ω. All LSB units are ADC LSBs unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J$ = 25˚C. (Note 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
CCD SOURCE REQUIREMENTS FOR FULL SPECIFIED ACCURACY AND DYNAMIC RANGE (Note 11)					
V_{WHITE}	Maximum Peak CCD Differential Signal Range	VGA Gain = 0 dB		**1.1**	V (min)
		VGA Gain = 9 dB		**0.4**	V (min)
V_{RFT}	Maximum CCD Reset FeedThrough Amplitude		2		V (min)
ADC CHARACTERISTICS					
	Resolution with No Missing Codes			**8**	Bits (min)
ILE	Integral Linearity Error (Note 12)			**±1.5**	LSB (max)
DNL	Differential Non-Linearity			**±1.0**	LSB (max)
PGA CHARACTERISTICS					
	Monotonicity			**8**	Bits (min)
	PGA Adjustment Range	$\frac{Gain_{PGA\ =\ 255}}{Gain_{PGA\ =\ 0}}$	2.95	**2.8**	V/V (min)
	Gain Error at any Gain (Note 14)			**1.4**	% (max)
VGA CHARACTERISTICS					
	Monotonicity			**4**	Bits (min)
	VGA Adjustment Range	$20\log\left(\frac{Gain_{VGA\ =\ 15}}{Gain_{VGA\ =\ 0}}\right)$	8.95	**8.5**	dB (min)
	Gain Error at any Gain (Note 15)			**±0.15**	dB (max)
OFFSET TRIM CHARACTERISTICS					
	Offset DAC LSB Size	In Units of ADC LSBs	0.42		LSB
	Offset DAC DNL	In Units of Offset DAC LSBs	±0.25	**±0.9**	LSB (max)
	Offset Add Magnitude	In Units of ADC LSBs	2.0	**1.6**	LSB (min)
				2.5	LSB (max)
SYSTEM CHARACTERISTICS					
	Full Channel Gain Error	VGA Gain = 1, PGA Gain = 1	±0.6	**±3.0**	% (max)
V_{OS1}	Pre-PGA Offset Error	VGA Gain = 1, Offset DAC = 0	±1		LSB
V_{OS2}	Post-PGA Offset Error	Offset Add = 0	±1		LSB
REFERENCE AND ANALOG INPUT CHARACTERISTICS (Note 7)					
	OS Input Capacitance		5		pF
	OS Input Leakage Current	Measured with OS = 2.45V_{DC}	2	**20**	nA (max)

Electrical Characteristics (Continued)

The following specifications apply for AGND = DGND = DGND(I/O) = 0V, $V_A = V_D = +5.0V_{DC}$, $V_{D(I/O)} = +5.0$ or $+3.0V_{DC}$, REF IN = $+1.225V_{DC}$, f_{MCLK} = 20 MHz, $R_S = 25\Omega$. All LSB units are ADC LSBs unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25^\circ C$. (Note 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
REFERENCE AND ANALOG INPUT CHARACTERISTICS (Note 7)					
R_{REF}	ADC Reference Ladder (REF OUT_{HI} to REF IN) Impedance		950	**500**	Ω (min)
				2000	Ω (max)
REF IN	Reference Voltage (Note 13)		1.225	**1.19**	V (min)
				1.26	V (max)

DC and Logic Electrical Characteristics

The following specifications apply for AGND = DGND = $DGND_{(I/O)}$ = 0V, $V_A = V_D = +5.0V_{DC}$, $V_{D(I/O)} = +5.0$ or $+3.0V_{DC}$, REF IN = $+1.225V_{DC}$, f_{MCLK} = 20 MHz, $R_s = 25\Omega$. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25^\circ C$.

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
CD0–CD7, MCLK, SYNC, SDI, SCLK, $\overline{CS}$, $\overline{RD}$ DIGITAL INPUT CHARACTERISTICS					
$V_{IN(1)}$	Logical “1” Input Voltage	$V_{D(I/O)} = 5.25V$		**2.0**	V (min)
		$V_{D(I/O)} = 3.6V$		**2.0**	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage	$V_{D(I/O)} = 4.75V$		**0.8**	V (max)
		$V_{D(I/O)} = 2.7V$		**0.7**	V (max)
I_{IN}	Input Leakage Current	$V_{IN} = V_D$	0.1		µA
		V_{IN} = DGND	−0.1		µA
C_{IN}	Input Capacitance		5		pF
DD0–DD7, $\overline{EOC}$, CCLK, SDO DIGITAL OUTPUT CHARACTERISTICS					
$V_{OUT(1)}$	Logical “1” Output Voltage	$V_{D(I/O)} = 4.75V$, $I_{OUT} = -360$ µA		**2.4**	V (min)
		$V_{D(I/O)} = 4.75V$, $I_{OUT} = -10$ µA		**4.4**	V (min)
		$V_{D(I/O)} = 2.7V$, $I_{OUT} = -360$ µA		**2.1**	V (min)
		$V_{D(I/O)} = 2.7V$, $I_{OUT} = -10$ µA		**2.5**	V (min)
$V_{OUT(0)}$	Logical “0” Output Voltage	$V_{D(I/O)} = 5.25V$, $I_{OUT} = 1.6$ mA		**0.4**	V (max)
		$V_{D(I/O)} = 3.6V$, $I_{OUT} = 1.6$ mA		**0.4**	V (max)
I_{OUT}	TRI-STATE® Output Current (DD0–DD7 only)	V_{OUT} = DGND	0.1		µA
		$V_{OUT} = V_D$	−0.1		µA
C_{OUT}	TRI-STATE Output Capacitance		5		pF
ϕ1, ϕ2, RS, TR DIGITAL OUTPUT CHARACTERISTICS					
$V_{OUT(1)}$	Logical “1” Output Voltage	$V_D = 4.75V$, $I_{OUT} = -360$ µA		**2.4**	V (min)
		$V_D = 4.75V$, $I_{OUT} = -10$ µA		**4.4**	V (min)
$V_{OUT(0)}$	Logical “0” Output Voltage	$V_D = 5.25V$, $I_{OUT} = 1.6$ mA		**0.4**	V (max)
POWER SUPPLY CHARACTERISTICS					
I_A	Analog Supply Current	Operating	25	**38**	mA (max)
		Standby	50		µA
I_D	Digital Supply Current	Operating	6	**8**	mA (max)
		MCLK = 0	65		µA
$I_{D(I/O)}$	Digital I/O Supply Current	Operating, $V_{D(I/O)} = 5.0V$	3.1	**6**	mA (max)
		Operating, $V_{D(I/O)} = 3.0V$	1.6	**4**	mA (max)
		MCLK = 0, $V_{D(I/O)} = 5.0V$ or 3.0V	1.7		mA

AC Electrical Characteristics, MCLK Independent

The following specifications apply for AGND = DGND = $DGND_{(I/O)}$ = 0V, V_A = V_D = $V_{D(I/O)}$ = +5.0V_{DC}, REF IN = +1.225V_{DC}, f_{MCLK} = 20 MHz, t_{MCLK} = 1/f_{MCLK}, t_r = t_f = 5 ns, R_s = 25Ω, C_L (databus loading) = 50 pF/pin. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX}**; all other limits T_A = T_J = 25˚C.

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
f_{MCLK}	Maximum MCLK Frequency			**20**	MHz (min)
	Minimum MCLK Frequency			**1**	MHz (max)
	MCLK Duty Cycle		30	**40**	% (min)
			70	**60**	% (max)
t_A	SYNC Setup of MCLK		5	**10**	ns (min)
$t_{CDSETUP}$	Correction Data Valid to CLK Setup		14	**20**	ns (min)
t_{CDHOLD}	Correction Data Valid to CLK Hold		−12	**0**	ns (min)
t_{D1H}, t_{D0H}	$\overline{RD}$ High to DD0–DD7 TRI-STATE		5	**15**	ns (max)
t_{DACC}	Access Time Delay from $\overline{RD}$ Low to DD0–DD7 Data Valid		15	**30**	ns (max)
f_{SCLK}	Maximum SCLK Frequency			**8**	MHz (min)
	SCLK Duty Cycle			**40**	% (min)
				60	% (max)
t_{SDI}	SDI Set-Up Time from SCLK Rising Edge		3	**10**	ns (min)
t_{HDI}	SDI Hold Time from SCLK Rising Edge		2	**15**	ns (min)
t_{DDO}	Delay from SCLK Falling Edge to SDO Data Valid		25	**55**	ns (max)
t_{HDO}	SDO Hold Time from SCLK Falling Edge	R_L = 3k, C_L = 25 pF	30	**55**	ns (max)
				5	ns (min)
t_{DELAY}	DELAY from SCLK Falling Edge to $\overline{CS}$ Rising or Falling Edge		5	**10**	ns (min)
t_{SETUP}	Set-Up Time of $\overline{CS}$ Rising or Falling Edge to SCLK Rising Edge		0	**10**	ns (min)
t_{S1H}, t_{S0H}	Delay from $\overline{CS}$ Rising Edge to SDO TRI-STATE	R_L = 3k, C_L = 50 pF	25	**50**	ns (max)
t_{RDO}	SDO Rise Time, TRI-STATE to High	R_L = 3k, C_L = 50 pF	20		ns
	SDO Rise Time, Low to High		20		ns
t_{FDO}	SDO Fall Time, TRI-STATE to Low	R_L = 3k, C_L = 50 pF	20		ns
	SDO Fall Time, High to Low		20		ns

AC Electrical Characteristics, MCLK Dependent

The following specifications apply for AGND = DGND = $DGND_{(I/O)}$ = 0V, V_A = V_D = $V_{D(I/O)}$ = +5.0V_{DC}, REF IN = +1.225V_{DC}, f_{MCLK} = 20 MHz, t_{MCLK} = 1/f_{MCLK}, t_r = t_f = 5 ns, R_s = 25Ω, C_L (databus loading) = 50 pF/pin. Refer to *Table 2*, **Configuration Register Parameters,** for limits labelled **C.R. Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX}**; all other limits T_A = T_J = 25˚C.

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
t_{START}	MCLK to first ϕ1 High		50 ns	**1**	t_{MCLK}
t_ϕ	ϕ1, ϕ2 Clock Period	Standard CCD Mode	400 ns	**8**	t_{MCLK}
		Even/Odd CCD Mode	800 ns	**16**	t_{MCLK}
$t_{TRWIDTH}$	Transfer Pulse (TR) Width			**C.R.**	µs
t_{GUARD}	ϕ1 to TR, TR to ϕ1 Guardband			**C.R.**	ns
$t_{RSWIDTH}$	Reset Pulse (RS) Width			**C.R.**	ns
t_{RS}	Falling Edge of ϕ1 to RS	Standard CCD Mode		**C.R.**	ns
	Either Edge of ϕ1 to RS	Even/Odd CCD Mode			
$t_{S/HREF}$	Falling Edge of ϕ1 to Ref. Sample	Standard CCD Mode		**C.R.**	ns
	Either Edge of ϕ1 to Ref. Sample	Even/Odd CCD Mode			

AC Electrical Characteristics, MCLK Dependent (Continued)

The following specifications apply for AGND = DGND = $DGND_{(I/O)}$ = 0V, V_A = V_D = $V_{D(I/O)}$ = +5.0V_{DC}, REF IN = +1.225V_{DC}, f_{MCLK} = 20 MHz, t_{MCLK} = 1/f_{MCLK}, t_r = t_f = 5 ns, R_s = 25Ω, C_L (databus loading) = 50 pF/pin. Refer to *Table 2*, **Configuration Register Parameters,** for limits labelled **C.R. Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX}**; all other limits T_A = T_J = 25˚C.

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
$t_{S/HSIG}$	Falling Edge of φ1 to Sig. Sample Either Edge of φ1 to Sig. Sample	Standard CCD Mode Even/Odd CCD Mode		**C.R.**	ns
$t_{S/HWIDTH}$	Sample Pulse Width (Acquisition Time)		50 ns	**1**	t_{MCLK}
$t_{SYNCLOW}$	SYNC Low Between Lines		100 ns	**2**	t_{MCLK} (min)
t_B	SYNC Setup of φ1 to End Line			**2**	t_{MCLK} (max)
$t_{CCLKWIDTH}$	CCLK Pulse Width		250 ns	**5**	t_{MCLK}
$t_{DATAVALID}$	Data Valid Time from $\overline{EOC}$ Low			**300**	ns (min)
$t_{\overline{EOC}WIDTH}$	$\overline{EOC}$ Pulse Width		250 ns	**5**	t_{MCLK}
	φ1 and φ2 Frequency	Standard CCD Mode Even/Odd CCD Mode	2.5 MHz 1.25 MHz	f_{MCLK}/**8** f_{MCLK}/**16**	Hz Hz
	φ1 and φ2 Duty Cycle			**50**	%

Electrical Characteristics (Notes)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND = AGND = DGND = $DGND_{(I/O)}$ = 0V, unless otherwise specified.

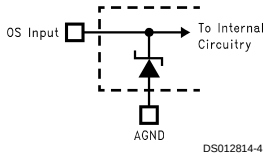
Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < GND or V_{IN} > V_A or V_D), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can simultaneously safely exceed the power supplies with an input current of 25 mA to two.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is P_D = (T_{Jmax}–T_A)/θ_{JA}. T_{Jmax} = 150˚C for this device. The typical thermal resistance (θ_{JA}) of this part when board mounted is 52˚C/W for the V52A PLCC package, and 70˚C/W for the VEG52A TQFP package.

Note 5: Human body model, 100pF capacitor discharged through a 1.5 kΩ resistor.

Note 6: See AN450 “Surface Mounting Methods and Their Effect on Product Reliability” or the section titled “Surface Mount” found in any National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Note 7: A Zener diode clamps the OS analog input to AGND as shown below. This input protection, in combination with the external clamp capacitor and the output impedance of the CCD, prevents damage to the LM9801 from transients during power-up.



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Note 8: To guarantee accuracy, it is required that V_A and V_D be connected together to the same power supply with separate bypass capacitors at each supply pin.

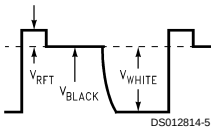
Note 9: Typicals are at T_J = T_A = 25˚C, f_{MCLK} = 20 MHz, and represent most likely parametric norm.

Note 10: Tested limits are guaranteed to National’s AOQL (Average Outgoing Quality Level).

Electrical Characteristics (Notes) (Continued)

Note 11: For CCDs, V_{BLACK} is defined as the CCD OS voltage for the reference period following the reset feedthrough pulse. V_{WHITE} is defined as the peak CCD pixel output voltage for a white (full scale) image with respect to the reference level, V_{BLACK} - V_{RFT} is defined as the peak positive deviation above V_{BLACK} of the reset feedthrough pulse. For CIS, V_{WHITE} is defined as the peak CCD pixel output voltage for a white (full scale) image with respect to GND (0V). The maximum correctable range of pixel-to-pixel V_{WHITE} variation is defined as the maximum variation in V_{WHITE} (due to PRNU, light source intensity variation, optics, etc.) that the LM9801 can correct for using its internal PGA.

CCD Output Signal



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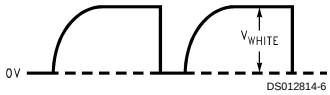
CIS Output Signal



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Note 12: Integral linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that best fits the actual transfer function of the ADC.

Note 13: Reference voltages below 1.19V may decrease SNR. Reference voltages above 1.26V may cause clipping errors inside the LM9801. The LM4041EIM3-1.2 (SOT-23 package) or the LM4041EIZ-1.2 (TO-92 package) bandgap voltage references are recommended for this application.

Note 14: PGA Gain Error is the maximum difference between the measured gain for any PGA code and the ideal gain calculated by using the formula

$$\text{Gain}_{PGA}\left(\frac{V}{V}\right) = 1 + C\frac{\text{PGA code}}{256} \quad \text{where } C = (\text{PGA RANGE} - 1)\frac{256}{255}$$

and PGA RANGE = the PGA adjustment range (in V/V) of the LM9801 under test.

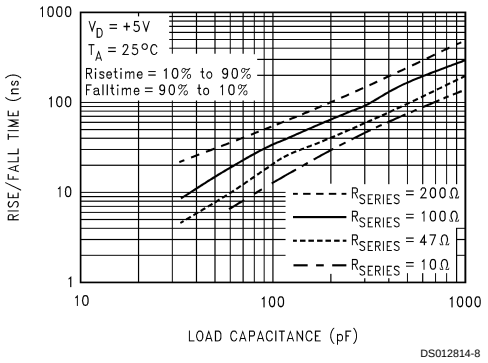
Note 15: VGA Gain Error is the maximum difference between the measured gain for any VGA code and the ideal gain calculated by using the formula

$$\text{Gain}_{VGA}(dB) = C\frac{\text{VGA code}}{16} \quad \text{where } C = (\text{VGA RANGE})\frac{16}{15}$$

and VGA RANGE = the VGA adjustment range (in dB) of the LM9801 under test.

Typical Performance Characteristics

ϕ1, ϕ2, RS, and TR Rise and Fall Times Through A Series Resistance vs Load Capacitance



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Pin Descriptions

CCD Driver Signals	
ϕ1	Digital Output. CCD clock signal, phase 1.
ϕ2	Digital Output. CCD clock signal, phase 2.
RS	Digital Output. Reset pulse for the CCD.
TR	Digital Output. Transfer pulse for the CCD.
Analog I/O	
OS	Analog Input. This is the OS (Output Signal) from the CCD. The maximum peak signal that can be accurately digitized is equal to the voltage at REF IN, typically 1.225V.
REF IN	Analog Inputs. These two pins are the system reference voltage inputs and should be tied together to a 1.225V voltage source and bypassed to AGND with a 0.1 µF monolithic capacitor.
REF OUT_{HI}	Analog Output. This reference voltage is developed internally by the LM9801, and is equal to 3 times REF IN. It should be bypassed to AGND with a 0.1 µF monolithic capacitor.
REF OUT_{MID}	Analog Output. This reference voltage is developed internally by the LM9801, and is equal to 2 times REF IN. It should be bypassed to AGND using a 0.1 µF monolithic capacitor.
V_{TEST1}, V_{TEST2}	Analog Inputs/Outputs. These pins are used for testing the device during manufacture and should be left unconnected.
Configuration Register I/O	
SDI	Digital Input. Serial Data Input pin.
SDO	Digital Output. Serial Data Output pin.
SCLK	Digital Input. This is the serial data clock, used to clock data in through SDI and out through SDO. SCLK is asynchronous to MCLK. Input data is latched and output data is changed on the rising edge of SCLK.
$\overline{CS}$	Digital Input. This is the Chip Select signal for writing to the Configuration Register through the serial interface. This input must be low in order to communicate with the Configuration Register. This pin is used for serial I/O only–it has no effect on any other section of the chip.
Digital Coefficient I/O	
CD0 (LSB)–CD7 (MSB)	Digital Inputs. Correction Coefficient Databus. This is the 8-bit data path for the gain adjust PGA, used during line scan.
CCLK	Digital Output. This is the signal that is used to clock the Gain coefficients into the LM9801. Data is latched on the rising edge of CCLK.
Digital Output I/O	
DD0 (LSB)–DD7 (MSB)	Digital Outputs. Pixel Output Databus. This data bus outputs the 8-bit digital output data during line scan.
$\overline{EOC}$	Digital Output. This is the End of Conversion signal from the ADC indicating that new pixel data is available.
$\overline{RD}$	Digital Input. Taking this input low places the data stored in the output latch on the bus. When this input is high the DD0–DD7 bus is in TRI-STATE.
General Digital I/O	
MCLK	Digital Input. This is the 20 MHz (typical) master system clock.
SYNC	Digital Input. A low-to-high transition on this input begins a line scan operation. The line scan operation terminates when this input is taken low.
Analog Power	
V_A	This is the positive supply pin for the analog supply. It should be connected to a voltage source of +5V and bypassed to AGND with a 0.1 µF monolithic capacitor in parallel with a 10 µF tantalum capacitor.
AGND	This is the ground return for the analog supply.
Digital Power	
V_D	This is the positive supply pin for the digital supply. It should be connected to a voltage source of +5V and bypassed to DGND with a 0.1 µF monolithic capacitor.
DGND	This is the ground return for the digital supply.
$V_{D(I/O)}$	This is the positive supply pin for the digital supply for the LM9801's I/O. It should be connected to a voltage source of +3V to +5V and bypassed to $DGND_{(I/O)}$ with a 0.1 µF monolithic capacitor. If the supply for this pin is different than the supply for V_A and V_D, it should also be bypassed with a 10 µF tantalum capacitor.
$DGND_{(I/O)}$	This is the ground return for the digital supply for the LM9801's I/O.
NC	
NC	All pins marked NC (no connect) should be left floating. Do not tie NC pins to ground., power supplies, or any other potential or signal.

Timing Diagrams

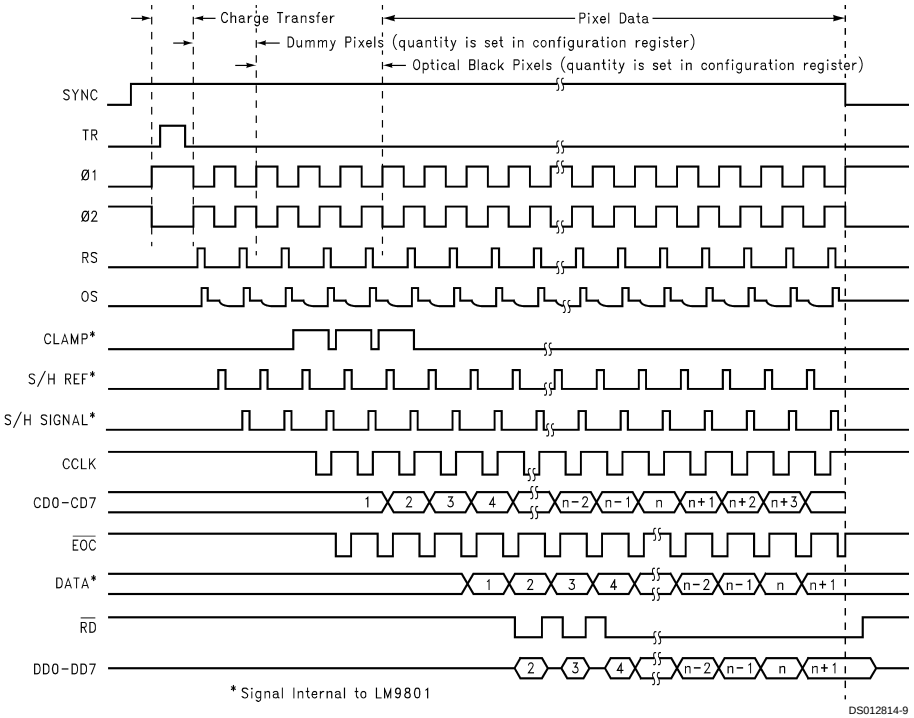


FIGURE 1. Line Scan Timing Overview

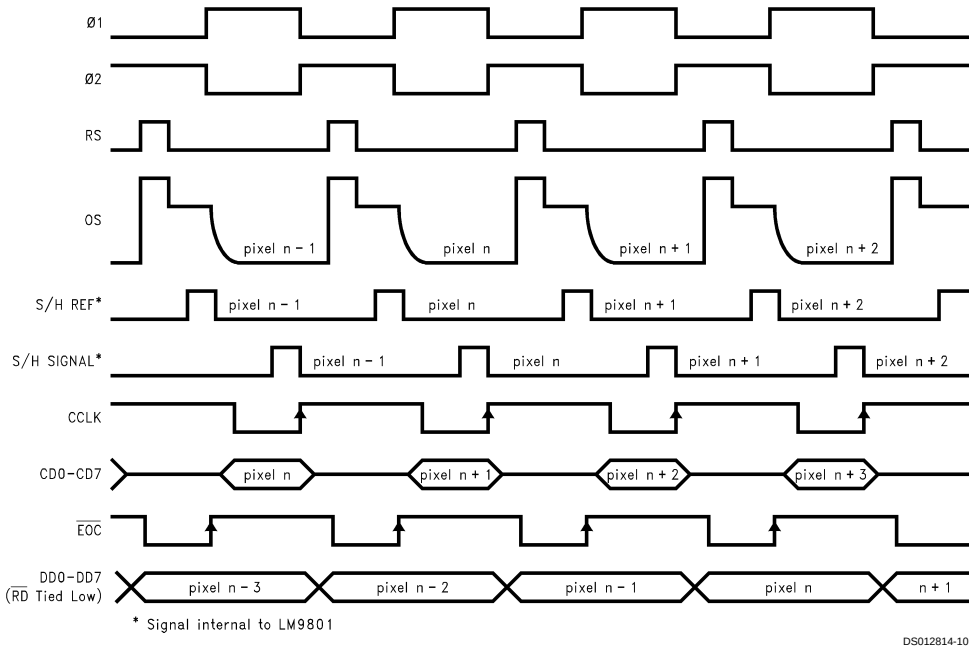


FIGURE 2. Pixel Pipeline Timing Overview

Timing Diagrams (Continued)

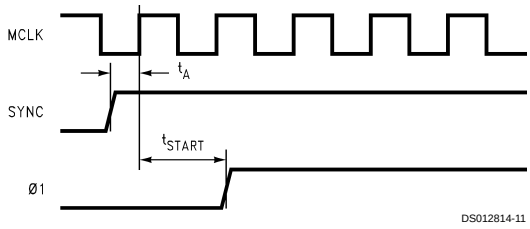


FIGURE 3. Timing for Start of Line Scan

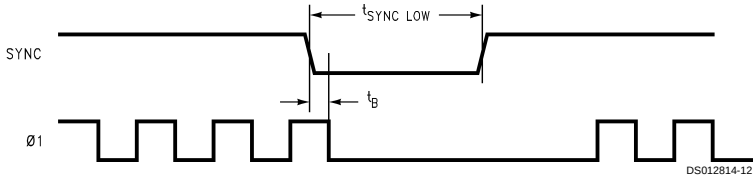


FIGURE 4. Timing for End of Line/Start of Next Line

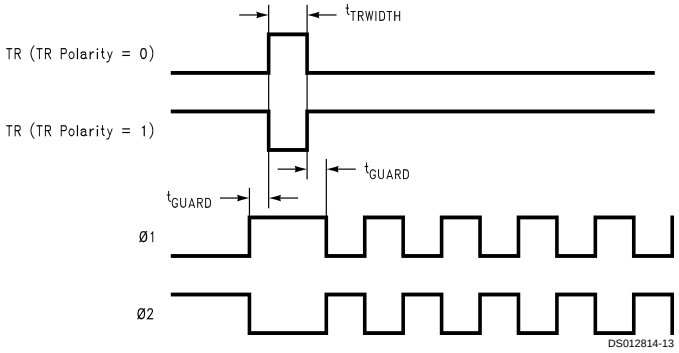


FIGURE 5. TR Pulse Timing

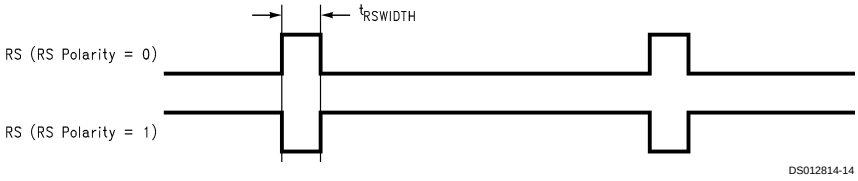
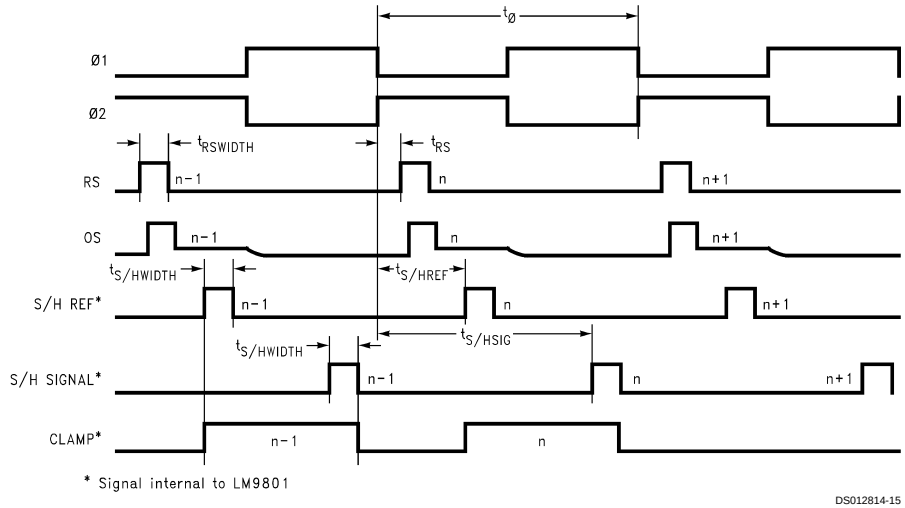


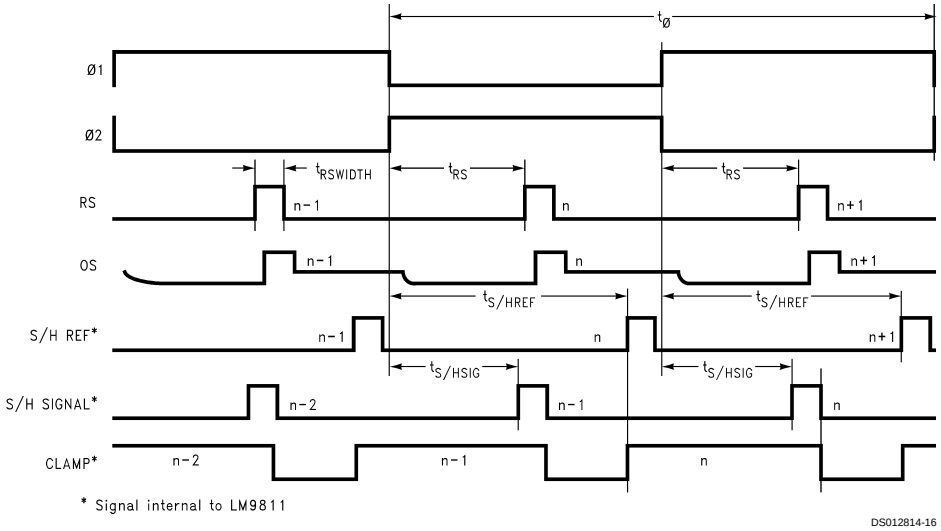
FIGURE 6. RS Pulse Polarity

Timing Diagrams (Continued)



Note: Clamp signal only active during optical black pixels at beginning of line.

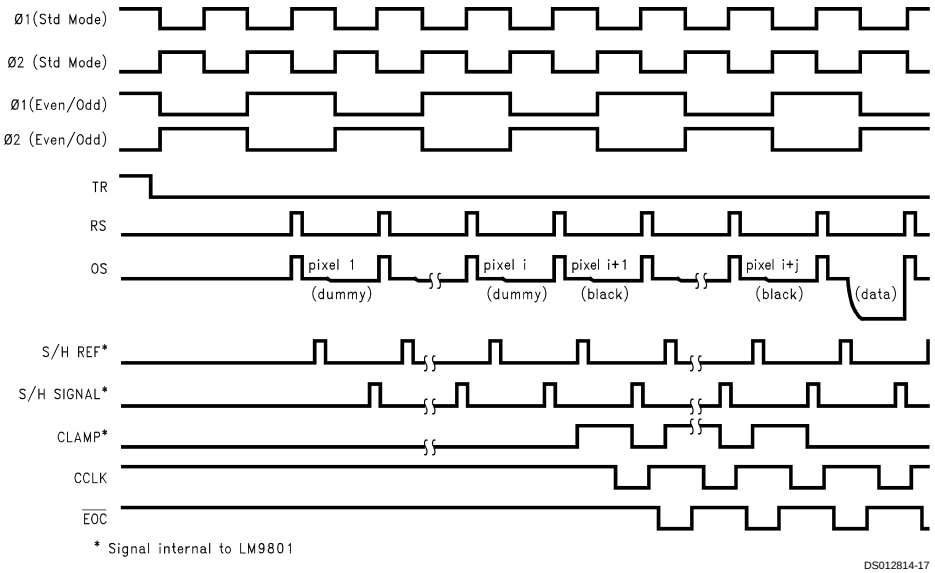
FIGURE 7. CCD Timing



Note: Clamp signal only active during optical black pixels at beginning of line.

FIGURE 8. CCD Timing (Even/Odd CCDs)

Timing Diagrams (Continued)



j = value programmed in Optical Black Register.
i = value programmed in Dummy Pixel Register - 1 (for example: Dummy Pixel Register = 17→i = 16→16 dummy pixels).

FIGURE 9. Dummy Pixel and Optical Black Pixel Timing

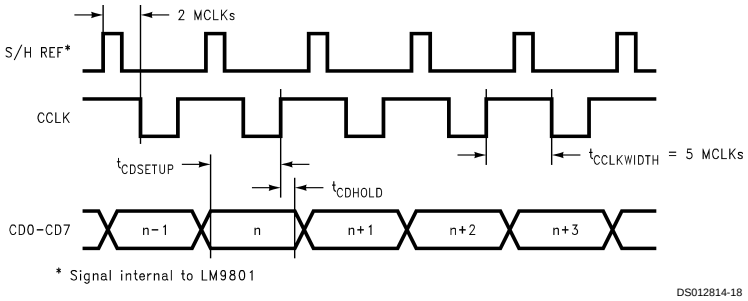


FIGURE 10. Coefficient Data Timing

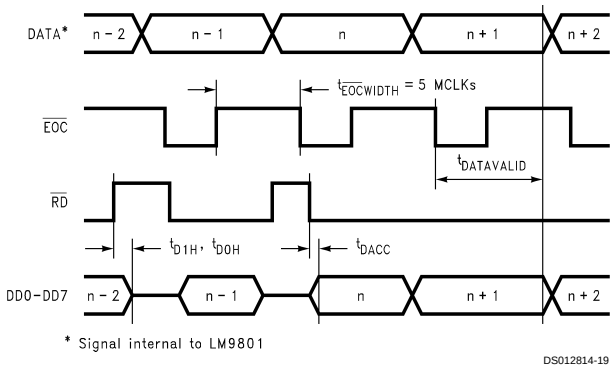


FIGURE 11. Output Data Timing

Timing Diagrams (Continued)

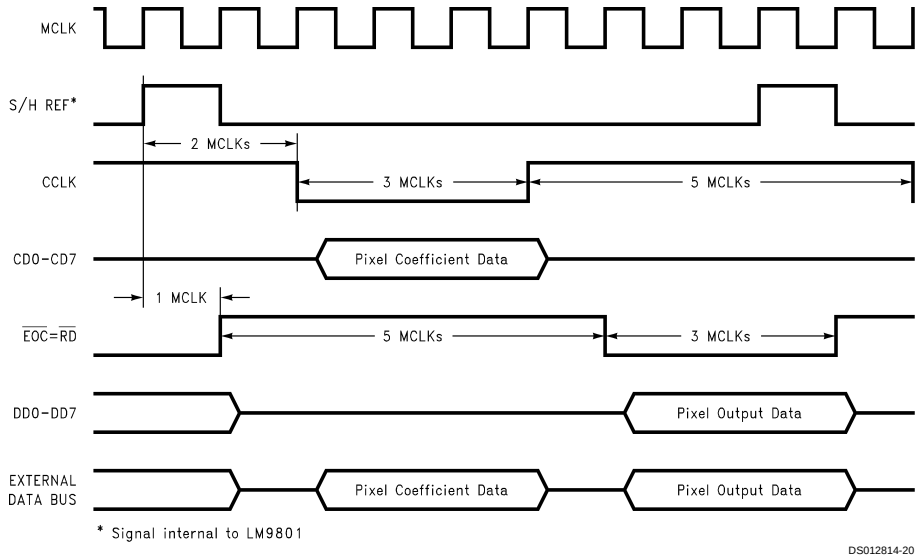


FIGURE 12. Data Timing (Output and Coefficient Data Sharing Same Bus)

Serial Configuration Register Timing Diagrams

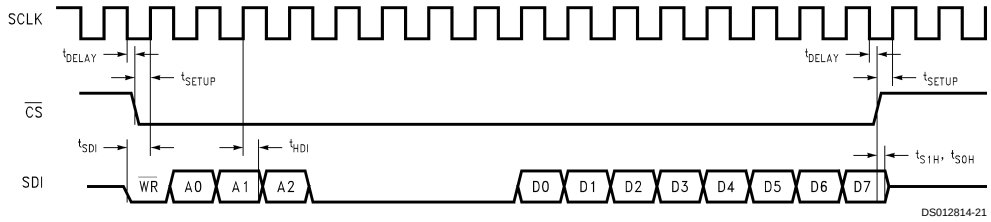


FIGURE 13. Configuration Register Write Timing using $\overline{CS}$, Continuous SCLK (16-Bit Word)

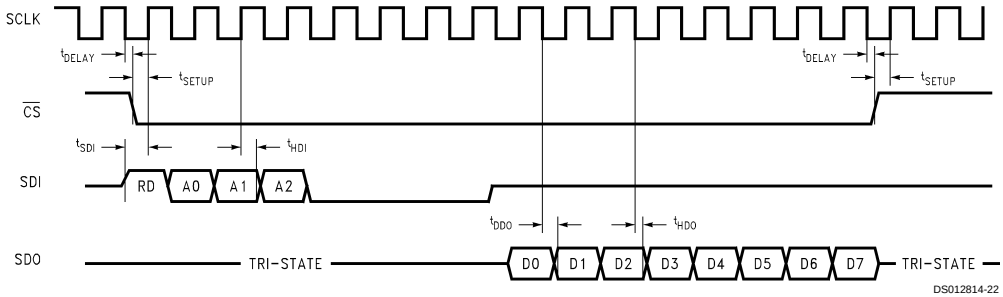


FIGURE 14. Configuration Register Read Timing using $\overline{CS}$, Continuous SCLK (16-Bit Word)

Serial Configuration Register Timing Diagrams (Continued)

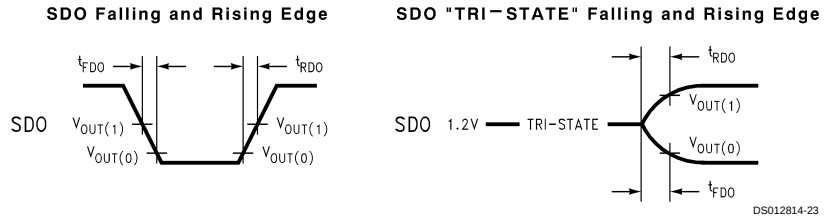


FIGURE 15. SDO Timing

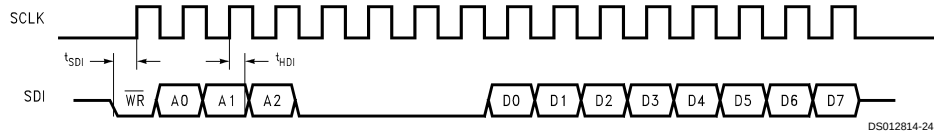


FIGURE 16. Configuration Register Write Timing with $\overline{CS}$ Continuously Low (16-Bit Word)

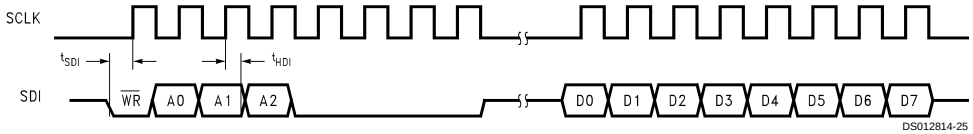


FIGURE 17. Configuration Register Write Timing with $\overline{CS}$ Continuously Low (Two 8-Bit Bytes)

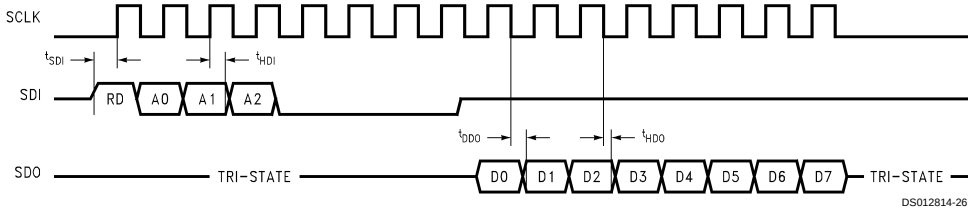


FIGURE 18. Configuration Register Read Timing with $\overline{CS}$ Continuously Low (16-Bit Word)

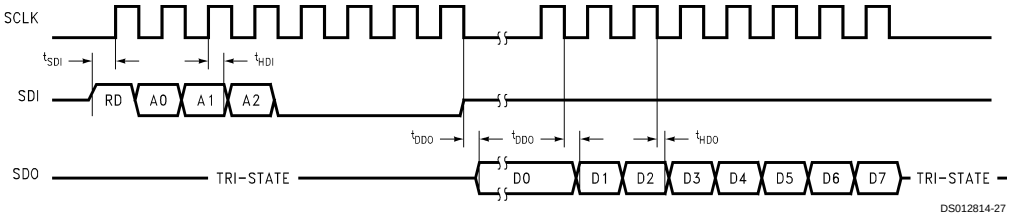


FIGURE 19. Configuration Register Read Timing with $\overline{CS}$ Continuously Low (Two 8-Bit Bytes)

Configuration Register

$t_{MCLK} = 1/f_{MCLK}$ = 1 MCLK period. Examples given in parenthesis are for f_{MCLK} = 20 MHz (t_{MCLK} = 50 ns).

TABLE 1. Configuration Register Address Table

A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	Standard Mode or Even/Odd Mode	RS Pulse Width		RS Pulse Polarity	RS Pulse Position			
			MODE	RSW1	RSW0	RSPOL	RSPOS3	RSPOS2	RSPOS1	RSPOS0
0	0	1	Sample Reference Position (Maximum Register Value is 14)				Sample Signal Position			
			SR3	SR2	SR1	SR0	SS3	SS2	SS1	SS0
0	1	0	ϕ1 Enable	ϕ2 Enable	RS Enable	TR Enable	TR Pulse Width		TR–ϕ1 Guardband	TR Polarity
			ϕ1EN	ϕ2EN	RSEN	TREN	TRW1	TRW0	TRGRD	TRPOL
0	1	1	Signal Polarity	Dummy Pixels (Minimum Register Value is 2)						
			SIGPOL	BLS6	BLS5	BLS4	BLS3	BLS2	BLS1	BLS0
1	0	0	Optical Black Pixels (Minimum Register Value is 1)							
			BLL7	BLL6	BLL5	BLL4	BLL3	BLL2	BLL1	BLL0
1	0	1	PGA Gain Coefficient							
			GAIN7	GAIN6	GAIN5	GAIN4	GAIN3	GAIN2	GAIN1	GAIN0
1	1	0	PGA Gain Source	Offset DAC Sign	Power-down	Offset Add	VGA Gain MSB	VGA Gain	VGA Gain	VGA Gain LSB
			PGASRC	ODSIGN	PD	OFFADD	VGA3	VGA2	VGA1	VGA0
1	1	1	Offset DAC MSB	Offset DAC	Offset DAC	Offset DAC LSB	Test Modes			
			VOS3	VOS2	VOS1	VOS0	0	0	0	0

Configuration Register

$t_{MCLK} = 1/f_{MCLK}$ = 1 MCLK period. Examples given in parenthesis are for f_{MCLK} = 20 MHz (t_{MCLK} = 50 ns). (Continued)

TABLE 2. Configuration Register Parameters

Parameter	Control Bits				Result
MODE	MODE				
	0				Standard CCD (ϕ frequency = $f_{MCLK}/8$)
	1				Even/Odd CCD (ϕ frequency = $f_{MCLK}/16$)
RS Pulse Width ($t_{RSWIDTH}$)	RS1	RS0			
	0	0			1 t_{MCLK} (50 ns)
	0	1			2 t_{MCLK} (100 ns)
	1	0			3 t_{MCLK} (150 ns)
	1	1			4 t_{MCLK} (200 ns)
RS Pulse Polarity	RSPOL				
	0				RS
	1				$\overline{RS}$
RS Pulse Position (t_{RS})	RSPOS3	RSPOS2	RSPOS1	RSPOS0	
	0	0	0	0	0.0t_{MCLK} (0 ns)
	0	0	0	1	0.5t_{MCLK} (25 ns)
	0	0	1	0	1.0t_{MCLK} (50 ns)
	0	0	1	1	1.5t_{MCLK} (75 ns)
	0	1	0	0	2.0t_{MCLK} (100 ns)
	0	1	0	1	2.5t_{MCLK} (125 ns)
	0	1	1	0	3.0t_{MCLK} (150 ns)
	0	1	1	1	3.5t_{MCLK} (175 ns)
	1	0	0	0	4.0t_{MCLK} (200 ns)
	1	0	0	1	4.5t_{MCLK} (225 ns)
	1	0	1	0	5.0t_{MCLK} (250 ns)
	1	0	1	1	5.5t_{MCLK} (275 ns)
	1	1	0	0	6.0t_{MCLK} (300 ns)
	1	1	0	1	6.5t_{MCLK} (325 ns)
	1	1	1	0	7.0t_{MCLK} (350 ns)
	1	1	1	1	7.5t_{MCLK} (375 ns)
Sample Reference Position ($t_{S/HREF}$)	SR3	SR2	SR1	SR0	
	0	0	0	0	0.0t_{MCLK} (0 ns)
	0	0	0	1	0.5t_{MCLK} (25 ns)
	0	0	1	0	1.0t_{MCLK} (50 ns)
	0	0	1	1	1.5t_{MCLK} (75 ns)
	0	1	0	0	2.0t_{MCLK} (100 ns)
	0	1	0	1	2.5t_{MCLK} (125 ns)
	0	1	1	0	3.0t_{MCLK} (150 ns)
	0	1	1	1	3.5t_{MCLK} (175 ns)
	1	0	0	0	4.0t_{MCLK} (200 ns)
	1	0	0	1	4.5t_{MCLK} (225 ns)
	1	0	1	0	5.0t_{MCLK} (250 ns)
	1	0	1	1	5.5t_{MCLK} (275 ns)
	1	1	0	0	6.0t_{MCLK} (300 ns)
	1	1	0	1	6.5t_{MCLK} (325 ns)
	1	1	1	0	7.0t_{MCLK} (350 ns)
	1	1	1	1	Not Valid

Configuration Register $t_{MCLK} = 1/f_{MCLK}$ = 1 MCLK period. Examples given in parenthesis are for f_{MCLK} = 20 MHz (t_{MCLK} = 50 ns). (Continued)

TABLE 2. Configuration Register Parameters (Continued)

Parameter	Control Bits				Result
	SS3	SS2	SS1	SS0	
Sample Signal Position ($t_{S/HSIG}$)	0	0	0	0	$0.0t_{MCLK}$ (0 ns)
	0	0	0	1	$0.5t_{MCLK}$ (25 ns)
	0	0	1	0	$1.0t_{MCLK}$ (50 ns)
	0	0	1	1	$1.5t_{MCLK}$ (75 ns)
	0	1	0	0	$2.0t_{MCLK}$ (100 ns)
	0	1	0	1	$2.5t_{MCLK}$ (125 ns)
	0	1	1	0	$3.0t_{MCLK}$ (150 ns)
	0	1	1	1	$3.5t_{MCLK}$ (175 ns)
	1	0	0	0	$4.0t_{MCLK}$ (200 ns)
	1	0	0	1	$4.5t_{MCLK}$ (225 ns)
	1	0	1	0	$5.0t_{MCLK}$ (250 ns)
	1	0	1	1	$5.5t_{MCLK}$ (275 ns)
	1	1	0	0	$6.0t_{MCLK}$ (300 ns)
	1	1	0	1	$6.5t_{MCLK}$ (325 ns)
	1	1	1	0	$7.0t_{MCLK}$ (350 ns)
	1	1	1	1	$7.5t_{MCLK}$ (375 ns)
ϕ1 Enable	ϕ1EN				
	0				ϕ1 Output Off
	1				ϕ1 Output On
ϕ2 Enable	ϕ2EN				
	0				ϕ2 Output Off
	1				ϕ2 Output On
RS Enable	RSEN				
	0				RS Output Off
	1				RS Output On
TR Enable	TREN				
	0				TR Output Off
	1				TR Output On
TR Pulse Width ($t_{TRWIDTH}$)	TRW1	TRW0			
	0	0			20 t_{MCLK} (1.0 µs)
	0	1			30 t_{MCLK} (1.5 µs)
	1	0			40 t_{MCLK} (2.0 µs)
	1	1			50 t_{MCLK} (2.5 µs)
TR-ϕ1 Guardband (t_{GUARD})	TRGRD				
	0				1 t_{MCLK} (50 ns)
	1				2 t_{MCLK} (100 ns)
TR Polarity	TRPOL				
	0				TR
	1				$\overline{TR}$
Signal Polarity	SIGPOL				
	0				Positive (CIS)
	1				Negative (CCD)

Configuration Register $t_{MCLK} = 1/f_{MCLK}$ = 1 MCLK period. Examples given in parenthesis are for f_{MCLK} = 20 MHz (t_{MCLK} = 50 ns). (Continued)

TABLE 2. Configuration Register Parameters (Continued)

Parameter	Control Bits								Result
	BLS6	BLS5	BLS4	BLS3	BLS2	BLS1	BLS0		Dummy Pixels
Dummy Pixels **Note:** Minimum Register Value is 2. Actual number of dummy pixels in CCD should be one less than number in this register.	0	0	0	0	0	0	0		Not Valid
	0	0	0	0	0	0	1		Not Valid
	0	0	0	0	0	1	0		1
	0	0	0	0	0	1	1		2
	•	•	•	•	•	•	•		•
	1	1	1	1	1	0	1		124
	1	1	1	1	1	1	0		125
	1	1	1	1	1	1	1		126
	BLL7	BLL6	BLL5	BLL4	BLL3	BLL2	BLL1	BLL0	Optical Black Pixels
Optical Black Pixels **Note:** Minimum Register Value is 1.	0	0	0	0	0	0	0	0	Not Valid
	0	0	0	0	0	0	0	1	1
	0	0	0	0	0	0	1	0	2
	0	0	0	0	0	0	1	1	3
	•	•	•	•	•	•	•	•	•
	1	1	1	1	1	1	0	1	253
	1	1	1	1	1	1	1	0	254
	1	1	1	1	1	1	1	1	255
	GAIN7	GAIN6	GAIN5	GAIN4	GAIN3	GAIN2	GAIN1	GAIN0	dB [V/V] (typical)
Internal PGA Gain Coefficient	0	0	0	0	0	0	0	0	0.00 1.000
	0	0	0	0	0	0	0	1	0.07 1.008
	0	0	0	0	0	0	1	0	0.13 1.015
	•	•	•	•	•	•	•	•	•
	1	1	1	1	1	1	0	1	9.35 2.935
	1	1	1	1	1	1	1	0	9.37 2.942
	1	1	1	1	1	1	1	1	9.40 2.950
PGA Gain Coefficient Source	PGASRC								
	0								Internal
	1								External
Offset DAC Sign	ODSIGN								
	0								Negative
	1								Positive
Power Down	PD								
	0								Operating
	1								Powered Down
Offset Add	OFF ADD								
	0								Offset ~0 LSB
	1								Offset ~+2 LSB

Configuration Register

$t_{MCLK} = 1/f_{MCLK}$ = 1 MCLK period. Examples given in parenthesis are for f_{MCLK} = 20 MHz (t_{MCLK} = 50 ns). (Continued)

TABLE 2. Configuration Register Parameters (Continued)

Parameter	Control Bits				Result
	VGA3	VGA2	VGA1	VGA0	dB [V/V] (typical)
VGA Gain	0	0	0	0	0.00 1.00
	0	0	0	1	0.60 1.07
	0	0	1	0	1.20 1.15
	0	0	1	1	1.79 1.23
	0	1	0	0	2.39 1.32
	0	1	0	1	2.99 1.41
	0	1	1	0	3.59 1.51
	0	1	1	1	4.19 1.62
	1	0	0	0	4.79 1.74
	1	0	0	1	5.38 1.86
	1	0	1	0	5.98 1.99
	1	0	1	1	6.58 2.13
	1	1	0	0	7.18 2.29
	1	1	0	1	7.78 2.45
	1	1	1	0	8.38 2.62
	1	1	1	1	8.97 2.81

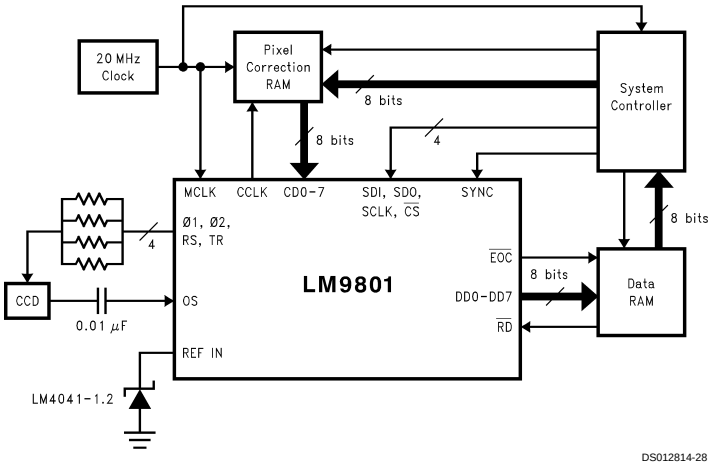
Configuration Register

$t_{MCLK} = 1/f_{MCLK}$ = 1 MCLK period. Examples given in parenthesis are for f_{MCLK} = 20 MHz (t_{MCLK} = 50 ns). (Continued)

TABLE 2. Configuration Register Parameters (Continued)

Parameter	Control Bits						Result
	ODSIGN	VOS3	VOS2	VOS1	VOS0		Offset (LSB) (typical)
Offset DAC	0	0	0	0	0		0.00
	0	0	0	0	1		−0.42
	0	0	0	1	0		−0.84
	0	0	0	1	1		−1.26
	0	0	1	0	0		−1.68
	0	0	1	0	1		−2.10
	0	0	1	1	0		−2.52
	0	0	1	1	1		−2.94
	0	1	0	0	0		−3.36
	0	1	0	0	1		−3.78
	0	1	0	1	0		−4.20
	0	1	0	1	1		−4.62
	0	1	1	0	0		−5.04
	0	1	1	0	1		−5.46
	0	1	1	1	0		−5.88
	0	1	1	1	1		−6.30
	1	0	0	0	0		0.00
	1	0	0	0	1		+0.42
	1	0	0	1	0		+0.84
	1	0	0	1	1		+1.26
	1	0	1	0	0		+1.68
	1	0	1	0	1		+2.10
	1	0	1	1	0		+2.52
	1	0	1	1	1		+2.94
	1	1	0	0	0		+3.36
	1	1	0	0	1		+3.78
	1	1	0	1	0		+4.20
	1	1	0	1	1		+4.62
	1	1	1	0	0		+5.04
	1	1	1	0	1		+5.46
	1	1	1	1	0		+5.88
	1	1	1	1	1		+6.30

Block Diagram of LM9801-Based System



Note: Power supplies and bypass capacitors not shown for clarity.

FIGURE 20. LM9801 System Block Diagram

Applications Information

1.0 THEORY OF OPERATION

The LM9801 removes errors from and digitizes a linear CCD pixel stream, while providing all the necessary clock signals to drive the CCD. Offset and gain errors for individual pixels are removed at the pixel rate. Offset errors are removed through correlated double sampling (CDS). Gain errors (which may come from any combination of PRNU, uneven illumination, $\cos^4$ effect, RGB filter mismatch, etc.) are removed through the use of a 8-bit programmable gain amplifier (PGA) in front of the ADC.

1.1 The Analog Signal Path (See Block Diagram)

The analog output signal from the CCD is connected to the OS input of the LM9801 through a 0.01 µF (typical, see Section 4.2, *Clamp Capacitor Selection*) DC blocking capacitor. During the CCD's optical black pixel segment at the beginning of every line, this input is clamped to the REF OUT_{MID} voltage (approximately 2.45V). This DC restore operation fixes the reference level of the CCD pixel stream at REF OUT_{MID}.

The signal is then buffered and fed to a digitally-programmed 4-bit VGA (variable gain amplifier). The gain of the VGA is digitally programmable in 16 steps from 1V/V to 3V/V. The VGA is used to compensate for peak white CCD outputs less than the 1.225V full-scale required by the LM9801 for maximum dynamic range. When used with parallel output CCDs, the VGA can fine-tune the amplitude of the red, green, and blue signals. For a detailed explanation of the VGA, see Section 4.3.

The output of the VGA goes into the CDS (Correlated Double Sampling) stage, consisting of two sample/hold amplifiers: S/H Ref (Reference) and S/H Signal. The reference level of the signal is sampled and held by the S/H Ref circuit and the active pixel data is sampled and held by the S/H Signal circuit. The output of S/H Ref is subtracted from the S/H Signal output and amplified by 2. The full-scale signal range at this point is approximately 2.45Vp-p. CDS reduces or eliminates many sources of noise, including reset noise, flicker noise, and both high and low frequency pixel-to-pixel offset variation. For more information on the CDS stage, see Section 4.4.

At this point an offset voltage can be injected by the 5-bit (4 bits + sign) Offset DAC. This voltage is designed to compensate for any small fixed DC offset introduced by the CDS S/Hs and the x2 amplifier. The LSB size of the DAC is approximately 0.42 ADC LSBs (4 mV). The adjustment range is ±6.3 ADC LSBs. For a detailed explanation of the Offset DAC, see Section 4.6.

The next stage is the PGA. This is a programmable gain amplifier that changes the gain *at the pixel rate* to correct for gain errors due to PRNU, uneven illumination (such as $\cos^4$ effect), RGB filter mismatch, etc. The gain adjustment range is 0 dB to 9 dB (1V/V to 3V/V) with 8 bits of resolution. The gain data (correction coefficients) is provided on the CD0–CD7 bus. The gain may also be fixed at any value between 0 dB and 9 dB with the **PGA Gain Coefficient** configuration register. For additional information on the PGA, see Section 4.7.

An approximately 2 LSB (19 mV) offset can be added at the output of the PGA stage if necessary to ensure that the offset is greater than zero. This eliminates the possibility of a negative offset clipping the darkest output pixels. For more information on the Offset Add Bit, see Section 4.8.

Finally, the output of the PGA is digitized by the ADC and made available on the DD0–DD7 bus (Section 4.9).

Three reference voltages are used throughout the signal path: the externally supplied REF IN (1.225V), and the internally generated REF OUT_{MID} (2.45V) and REF OUT_{HI} (3.675V).

1.2 The CCD Clocking Signals

To maximize the flexibility of the LM9801, the CCD's ϕ1, ϕ2, RS, and TR pulses are internally generated, with a wide range of options, making these signals compatible with most commercial linear CCDs. In many cases, these output sig-

Applications Information (Continued)

nals can drive the CCD clock inputs directly, with only series resistors (for slew rate control) between the LM9801's outputs and the CCD clock inputs.

1.3 The Digital Interface

There are three main sections to the digital interface of the LM9801: a serial interface to the Configuration Register, where all device programming is done, an 8 bit-wide input databus for gain correction coefficients with a synchronous clock output (CCLK), and an 8-bit output databus for the final pixel output data with a synchronous end of conversion output signal ($\overline{EOC}$) and an output enable input ($\overline{RD}$). Please note that the $\overline{CS}$ input affects only the serial I/O–it has no effect on the output databus, input coefficient bus, or any other section of the LM9801.

2.0 DIGITAL INTERFACE

2.1 Reading and Writing to the Configuration Register

Communication with the Configuration Register is done through a standard MICROWIRE™ serial interface. This interface is also compatible with the Motorola SPI™ standard and is simple enough to easily be implemented in custom hardware if desired.

The serial interface timing is shown in *Figures 13, 14* and *Figures 16, 17, 18, 19*. Data is sent serially, LSB first. (Please note that some microcontrollers output data MSB first. When using these microcontrollers the bits in the configuration register are effectively reversed.) Input data is latched on the rising edge of SCLK, and output data changes on the falling edge of SCLK. $\overline{CS}$ must be low to enable serial I/O.

If SCLK is only clocked when sending or receiving data from the LM9801, and held low at all other times, then $\overline{CS}$ can be tied low permanently as shown in *Figures 16, 17, 18, 19*. If SCLK is continuous, then $\overline{CS}$ must be used to determine the beginning and the end of a serial byte or word (see *Figures 13, 14*). Note that $\overline{CS}$ must make its high-to-low and low-to-high transitions when SCLK is low, otherwise the internal bit counter may receive an erroneous pulse, causing an error in the write or read operation.

Data may be transmitted and received in two 8-bit bytes (typical with microcontroller interfaces) or one 16-bit word (for custom serial controllers).

The Configuration Register is programmed by sending a control byte to the serial port. This byte indicates whether this is a read or a write operation, and gives the 3-bit address of the register bank to be read from or written to. If this is a read operation, the next 8 SCLKs will output the data at the requested location on the SDO pin. If this is a write operation, the data to be sent to the specified location should be clocked in on the SDI input during the next 8 SCLKs. Data is sent and received using the LSB (Least Significant Bit) first format.

For maximum system reliability, each configuration register location can be read back and verified after a write.

If the serial I/O to the configuration register falls out of sync for any reason, it can be reset by sending 8 or more SCLKs with $\overline{CS}$ held high.

2.2 Writing Correction Coefficient Data in the CD0–CD7 Bus

Correction coefficient data for each pixel is latched on the rising edge of the CCLK output signal (see *Figure 10*). Note that there is a 3 pixel latency between when the coefficient data is latched and when the output data is available. As *Figure 2*, *Pixel Pipeline Timing Overview* shows, coefficient data for pixel n is latched shortly before the output data for pixel n-2 becomes available on the output databus (DD0–DD7). Note that there is no way to provide a correction coefficient for pixel 1, the first pixel in the CCD array. This is not a problem since the first several pixels of a CCD are usually optical black pixels, and used for clamping.

2.3 Reading Output Data on the DD0–DD7 Bus

The corrected digital output data representing each pixel is available on the DD0–DD7 databus. The data is valid after the falling edge of the $\overline{EOC}$ output. The $\overline{RD}$ input takes the databus in and out of TRI-STATE. $\overline{RD}$ can be held low at all times if there are no other devices needing the bus, or it can be used to TRI-STATE the bus between pixels, allowing other devices access to the bus. *Figure 12*, *Data Timing (Output and Coefficient Data Sharing Same Bus)*, shows how $\overline{EOC}$ can be tied to $\overline{RD}$ to automatically multiplex between coefficient data and conversion data.

2.4 MCLK

This is the master clock input that controls the LM9801. The pixel conversion rate is fixed at 1/8 of this frequency. Many of the timing parameters are also relative to the frequency of this clock.

2.5 SYNC

This input signals the beginning of a line. When SYNC goes high, the LM9801 generates a TR pulse, then begins converting pixels until the SYNC line is brought low again. Since there is no pixel counter in the LM9801, it will work with CCDs of any length.

3.0 DIGITAL CCD INTERFACE

3.1 Buffering ϕ1, ϕ2, RS, and TR

The LM9801 can drive the ϕ1, ϕ2, RS, and TR inputs of many CCDs directly, without the need for external buffers between the LM9801 and the CCD. Most linear CCDs designed for scanner applications require 0V to 5V signal swings into 20 pF to 500 pF input loading. Series resistors are typically inserted between the driver and the CCD to control slew rate and isolate the driver from the large load capacitances. The values of these resistors are usually given in the CCD's datasheet.

4.0 ANALOG INTERFACE

4.1 Voltage Reference

The two REF IN pins should be connected to a 1.225V ±2% reference voltage capable of sinking between 2 mA and 5 mA of current coming from the 500Ω–1400Ω resistor string between REF OUT_{HI} and REF IN. The LM4041-1.2 1.225V bandgap reference is recommended for this application as shown in *Figure 21*. The inexpensive "E" grade meets all the requirements of the application and is available in a TO-92 (LM4041EIZ-1.2) package as well as a SOT-23 package (LM4041EIM3-1.2) to minimize board space.

Applications Information (Continued)

Due to the transient currents generated by the LM9801's ADC, PGA, and CDS circuitry, the REF IN pins, the REF OUT_{MID} pin and the REF OUT_{HI} pin should all be bypassed to AGND with 0.1 µF monolithic capacitors.

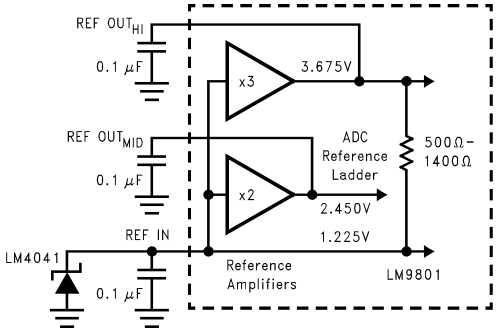


FIGURE 21. Voltage Reference Generation

4.2 Clamp Capacitor Selection

This section is very long because it is relatively complicated to explain, but the answer is short and simple: A clamp capacitor value of 0.01 µF should work in almost all applications. The rest of this section describes exactly how this value is selected.

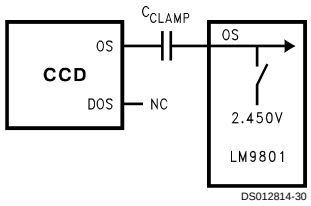


FIGURE 22. OS Clamp Capacitor and Internal Clamp

The output signal of many CCDs rides on a large DC offset (typically 8V to 10V) which is incompatible with the LM9801's 5V operation. To eliminate this offset without resorting to additional higher voltage components, the output of the CCD is AC coupled to the LM9801 through a DC blocking capacitor, C_{CLAMP} (the CCD's DOS output is not used). The value of this capacitor is determined by the leakage current of the LM9801's OS input and the output impedance of the CCD. The leakage through the OS input determines how quickly the capacitor value will drift from the clamp value of REF OUT_{MID}, which then determines how many pixels can be processed before the droop causes errors in the conversion (±0.1V is the recommended limit). The output impedance of the CCD determines how quickly the capacitor can be charged to the clamp value during the black reference period at the beginning of every line.

The minimum clamp capacitor value is determined by the maximum droop the LM9801 can tolerate while converting one CCD line. The following equation takes the maximum leakage current into the OS input, the maximum allowable droop (100 mV), the number of pixels on the CCD, and the pixel conversion rate (f_{MCLK}/8) and provides the minimum clamp capacitor value:

$$C_{CLAMP\ MIN} = \frac{i}{dV}\,dt$$

$$= \frac{\text{leakage current (A)}}{\text{max droop (V)}}\,\frac{\text{number of pixels}}{\text{conversion rate (Hz)}}$$

For example, if the OS input leakage current is 20 nA worst-case, the CCD has 2700 active pixels, the conversion rate is 2.5 MHz (f_{MCLK} = 20 MHz), and the max droop desired is 0.1V, the minimum clamp capacitor value is:

$$C_{CLAMP\ MIN} = \frac{20\ nA}{0.1V}\,\frac{2700}{2.5\ MHz}$$

$$= 216\ pF$$

The maximum size of the clamp capacitor is determined by the amount of time available to charge it to the desired value during the optical black portion of the CCD output. The internal clamp is on for each pixel from the rising edge of the S/H ref pulse to the falling edge of the S/H signal pulse (see *Figures 7, 8*). This time can be calculated using the values stored in the Sample Signal and Sample Reference configuration registers and the MCLK frequency. For normal CCDs:

$$t_{DARK}(s) = \frac{2 + SS - SR}{2f_{MCLK}(Hz)}$$

And for even/odd CCDs:

$$t_{DARK}(s) = \frac{18 + SS - SR}{2f_{MCLK}(Hz)}$$

Where SS is the value in the Sample Signal Position register (0–15), SR is the value in the Sample Reference Position register (0–14), f_{MCLK} is the MCLK frequency, and t_{DARK} is the amount of time (per pixel) that the clamp is on.

The following equation takes the number of optical black pixels, the amount of time (per pixel) that the clamp is closed, the CCD's output impedance, and the desired accuracy of the final clamp voltage and provides the maximum clamp capacitor value that allows the clamp capacitor to settle to the desired accuracy within a single line:

$$C_{CLAMP\ MAX} = \frac{t}{R}\,\frac{1}{\ln(\text{accuracy})}$$

$$= \frac{n}{R_{OUT}(\Omega)}\,\frac{t_{DARK}(s)}{\ln(\text{accuracy})}$$

Where n = the number of optical black pixels, t_{DARK} is the amount of time (per pixel) that the clamp is on, R_{OUT} is the output impedance of the CCD, and accuracy is the ratio of the worst-case initial capacitor voltage to the desired final capacitor voltage. For example, if a CCD has 18 black reference pixels, the output impedance of the CCD is 1500Ω, the LM9801 is configured to clamp for 300 ns, the worst case initial voltage across the capacitor is 10V, and the desired voltage after clamping is 0.1V (accuracy = 10/0.1 = 100), then:

$$C_{CLAMP\ MAX} = \frac{18}{1500\Omega}\,\frac{300\ ns}{\ln(100)}$$

$$= 514\ pF$$

The final value for C_{CLAMP} should be less than or equal to $C_{CLAMP\ MAX}$, but no less than $C_{CLAMP\ MIN}$. A value of 470 pF will work in this example.

In some cases, depending primarily on the choice of CCD, $C_{CLAMP\ MAX}$ may actually be *less* than the $C_{CLAMP\ MIN}$, meaning that the capacitor cannot be charged to its final voltage

Applications Information (Continued)

during the black pixels at the beginning of a line and hold its voltage without drooping for the duration of that line. This is usually not a problem because in most applications the CCD is clocked continuously as soon as power is applied. In this case, a larger capacitor can be used (guaranteeing that the $C_{CLAMP\ MIN}$ requirement is met), and the final clamp voltage is forced across the capacitor over multiple lines. This equation calculates how many lines are required before the capacitor settles to the desired accuracy:

$$\text{lines} = \left(\frac{R_{OUT}}{n}\frac{C_{CLAMP}}{t_{DARK}}\right) \ln\left(\frac{\text{Initial Voltage}}{\text{Final Voltage}}\right)$$

Using the values shown before and a clamp capacitor value of 0.01 µF, this works out to be:

$$\text{lines} = \left(\frac{1500\Omega}{18}\frac{0.01\ \mu F}{300\ \text{ns}}\right) \ln\left(\frac{10V}{0.1V}\right) = 12.8\ \text{lines}$$

At a 2.5MHz conversion rate, this is about 14 ms.

In this example a 0.01 µF capacitor takes 14 ms after power-up to charge to its final value, but its droop across all subsequent lines is now less than 2 mV (using the previous example's values). This wide margin is the reason a C_{CLAMP} value of 0.01 µF will work in most applications.

4.3 VGA

The LM9801 has a VGA (Variable Gain Amplifier) that can be used to increase the amplitude of the CCD signal prior to sampling, correction, and digitization. The gain of the VGA is 0 dB to 9 dB and is determined by the codes in the 4-bit VGA Gain register, as given by the equation:

$$\text{Gain}_{VGA}\ (\text{dB}) = \frac{\text{VGA code}}{16} 9.55$$

This gain may be changed at the line rate (not the pixel rate) by writing to the configuration register. You can write to the configuration register to change the gain at any time, but if you write during a line, the remaining pixels of that line may be corrupted. It is best to change the gain after all active pixels have been read out or while SYNC is low.

4.4 Correlated Double Sampler (CDS)

Figure 23 shows the output stage of a typical CCD and the resulting output waveform:

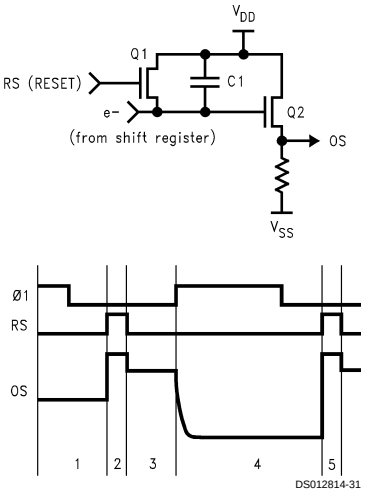


FIGURE 23. CDS

Capacitor C1 converts the electrons coming from the CCD's shift register to an analog voltage. The source follower output stage (Q2) buffers this voltage before it leaves the CCD. Q1 resets the voltage across capacitor C1 in between every pixel at intervals 2 and 5. When Q1 is on, the output signal (OS) is at its maximum. After Q1 turns off (period 3), the OS level represents the residual voltage across C1 ($V_{RESIDUAL}$). $V_{RESIDUAL}$ includes charge injection from Q1, thermal noise from the ON resistance of Q1, and other sources of error. When the shift register clock (ϕ1) makes a low to high transition (period 4), the electrons from the next pixel flow into C1. The charge across C1 now contains the voltage proportional to the number of electrons plus $V_{RESIDUAL}$, an error term. If OS is sampled at the end of period 3 and that voltage is subtracted from the OS at the end of period 4, the $V_{RESIDUAL}$ term is canceled and the noise on the signal is reduced. ($[V_{SIGNAL}+V_{RESIDUAL}] - V_{RESIDUAL} = V_{SIGNAL}$). This is the principal of Correlated Double Sampling.

The LM9801 implements CDS with two switched-capacitor S/H amplifiers. The S/Hs acquire a signal within a 50 ns window which can be placed anywhere in the pixel period with 25 ns precision. See *Figures 7, 8* for more detailed timing information.

4.5 CIS Mode

The LM9801 provides some support for CIS (Contact Image Sensor) devices by offering a sampling mode for capturing positive going signals, as opposed to the CCD's negative going signal.

Applications Information (Continued)

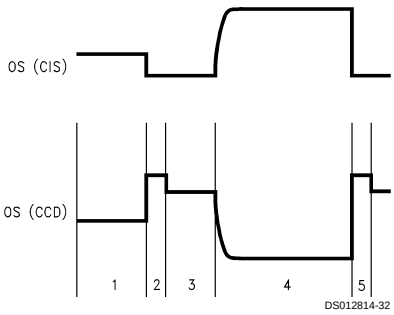


FIGURE 24. CIS vs CCD Output Signals

While CIS devices do not usually have a reference level with which to perform correlated double sampling, many have a very repeatable reset level which can be used as a black reference allowing the LM9801 to perform pseudo CDS on the signal. For more information on CIS applications, see Section 9.0. When the Signal Polarity bit is set to a zero, the LM9801 expects a positive going signal, typically from a CIS device. When the Signal Polarity bit is set to a one, the LM9801 expects a negative going signal, typically from a CCD sensor.

4.6 Offset DAC

The 4 bit plus sign Offset DAC is used to compensate for DC offsets due to the correlated double sampling stage. The offset can be corrected in 31 steps of 0.42 ADC LSB size between −6.3 and +6.3 LSBs. Note that the DAC comes betore the PGA, so any offset errors at this stage are multiplied by the gain of the PGA. The calibration procedure described in Section 5.0 demonstrates how to use the DAC to eliminate offset errors before scanning begins.

Note that this DAC is programmed during LM9801 calibration/configuration and is not meant to compensate for pixel-to-pixel CCD offset errors. CDS cancels the pixel-rate offset errors.

4.7 Programmable Gain Amplifier (PGA)

The PGA provides 8 bits of pixel-to-pixel gain correction over a 0 dB to 9 dB (x1 to x3) range. After the input signal is sampled and held by the CDS stage, it is amplified by the gain indicated by the data (“PGA Code”) on the CD0–CD7 databus using the formula:

$$\text{Gain}\left(\frac{V}{V}\right) = 1 + \frac{\text{PGA code}}{256}\,1.95$$

4.8 Offset Add Bit

In addition to the Offset DAC, there is a bit in the configuration register which, when set, adds a positive 2 LSB offset at the output of the PGA. This offset ensures that any offset between the output of the PGA and the ADC is positive, so that no dark level information is lost due to negative offsets. The calibration procedure described in Section 5.0 demonstrates how to set this bit.

4.9 ADC

The ADC converts the normalized analog output signal to an 8-bit digital code. The $\overline{EOC}$ output goes from high to low to indicate that a new conversion is ready. ADC data can be latched by external memory on the rising edge of $\overline{EOC}$. The $\overline{RD}$ input takes the ADC’s output buffer in and out of TRI-STATE. $\overline{RD}$ may be tied to $\overline{EOC}$ in many applications, putting the data on the bus only when EOC is low, and allowing other data on the bus (such as CD0–CD7 correction data) at other times. In this way the output data and correction coefficient data can share the same databus (see *Figure 12*).

5.0 CALIBRATION

Calibration of a CCD scanner is done to normalize the pixels of a linear CCD so that each pixel produces the same digital output code at the output of the scanner when presented with the same image light intensity. This intensity ranges from black (no light) to white (maximum light intensity). The CCD’s analog output may have large pixel-to-pixel DC offsets (corresponding to errors on black signals) and pixel-to-pixel variations in their output voltage given the same white image (corresponding to errors on brighter signals). If these offsets are subtracted from each pixel, and each pixel is given its own gain setting to correct for different efficiencies, then these errors can be eliminated.

Ideally the digital output code for any pixel would be zero for a black image, and some code near fullscale for an image with maximum brightness. For an 8-bit system like the LM9801, that code might be 250. This code will be called the Target Code.

The LM9801 eliminates these global and pixel-to-pixel offset and gain errors with its Correlated Double Sampling (CDS), Offset DACs, Variable Gain Amplifier, and pixel-rate Programmable Gain Amplifier. This section describes how to program the LM9801 and the coefficient RAM being used with it to eliminate these errors.

Calibration of a LM9801-based system requires 3 steps. The first, described in Section 5.1, *Offset Calibration*, takes a black image and normalizes the digital output code for each pixel to a code at or near 0.

The second step, Section 5.2, *Coarse Gain (VGA) Calibration*, finds the optimum gain setting that places the output voltage of all the pixels within the 9 dB adjustment range of the PGA.

The final step, described in Section 5.3, *PGA Correction Coefficients (Shading Calibration)*, describes how to calculate the gain required to normalize the output of each pixel to the desired output code (the Target code).

5.1 Offset Calibration

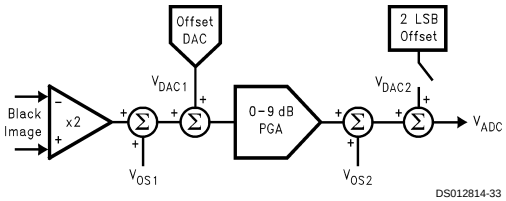


FIGURE 25. Offset Calibration

Applications Information (Continued)

This procedure corrects for static offsets generated by the CCD and the LM9801. Because the LM9801 uses CDS to eliminate the pixel-to-pixel offset errors of the CCD, no pixel-rate offset correction is required.

To use the Offset DAC and Offset Add bit for offset correction, the offset errors (V_{OS1} and V_{OS2}) must first be determined, as shown in *Figure 25*. This is done be measuring the voltage at the PGA output, using the ADC with a black image on the CCD (a black image can usually be created simply by turning off the scanner's illumination). If this voltage is known with a PGA gain of 1.00V/V (0 dB) and 2.95V/V (9 dB), then the offset errors (V_{OS1} and V_{OS2}) can be determined from the following two equations:

$V_{ADC1} = 1(V_{OS1} + V_{DAC1}) + V_{OS2} + V_{DAC2}$
(PGA gain = 1)

$V_{ADC2} = 2.95(V_{OS1} + V_{DAC1}) + V_{OS2} + V_{DAC2}$
(PGA gain = 2.95)

Solving for V_{OS1} and V_{OS2}:

$V_{OS1} = (V_{ADC2}–V_{ADC1})/1.95–V_{DAC1}$

$V_{OS2} = (2.95V_{ADC1}–V_{ADC2})/1.95–V_{DAC2}$

These equations were used to produce this procedure for cancelling the LM9801's offset errors. Please note that all voltages and measurements are in units of ADC LSBs to simplify calibration.

1. Set the VGA Gain to 1V/V (VGA code = 0 LSBs).
2. Set the Offset DAC (V_{DAC1}) to its maximum value (+6.3 LSBs) to ensure the total offset is positive and therefore measurable by the ADC.
3. Set the Offset Add bit (V_{DAC2}) to 0.
4. Set the PGA Gain to 1V/V (PGA code = 0).
5. Digitize a black line.
6. Calculate the average (in ADC LSBs) of all the valid pixels in the black line and store that number as V_{ADC1}.
7. Set the PGA Gain to 2.95V/V (PGA code = 255).
8. Digitize a black line.
9. Calculate the average (in ADC LSBs) of all the valid pixels in the black line and store that number as V_{ADC2}.
10. Calculate V_{OS1}:
    $V_{OS1} = (V_{ADC2}–V_{ADC1})/1.95–6.3$
11. Program the Offset DAC register using the formula:
    Offset DAC code = $-(V_{OS1})(15/6.3)$
    $= (6.3 + (V_{ADC1}–V_{ADC2})/1.95)(15/6.3)$
    $= 15 + 1.22(V_{ADC1}–V_{ADC2})$
    (**Note:** This calculation can be done as
    $15 + 39(V_{ADC1}–V_{ADC2})/32$
    for ease of programming in 8-bit microcontrollers)
12. If $3V_{ADC1} > V_{ADC2}$, then set the Offset Add bit to 0.
    If $3V_{ADC1} < V_{ADC2}$, set the Offset Add bit to 1.
13. The final value of the offset present at the ADC input can be used for the shading calibration calculations. Calculate the final value of the ADC input offset (V_{OFFSET}) using:

$V_{OFFSET} = (3V_{ADC1}–V_{ADC2})/2$
(if the Offset Add bit is 0), or

$V_{OFFSET} = (3V_{ADC1}–V_{ADC2})/2 + 2$
(if the Offset Add bit is 1)

5.2 Coarse Gain Calibration

The LM9801's PGA corrects for up to 9 dB of variation in the CCD output signal's white level intensity. That 9 dB range has to be centered inside the 9 dB window of correction as shown in *Figure 26*. The window's upper limit is determined by the Target code, and the lower limit by the Target code divided by 2.8 (this corresponds to the minimum gain range of the PGA). To allow proper calibration, the amplitude of all the pixels in the CCD should be inside this range when those pixels are scanning an image corresponding to the Target code. The placement of the pixels inside the 9 dB window can be controlled by any of three ways: changing the gain of the VGA, changing the integration time of the CCD, or changing the intensity of the light source.

In most designs, the output waveform of the CCD can be brought into the 9 dB correction range of the PGA by adjusting the gain of the VGA. This is the next step in system calibration.

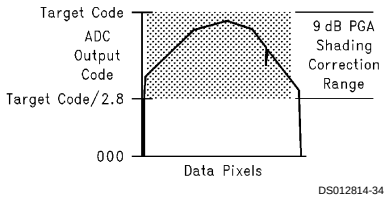


FIGURE 26. CCD Input Signal In Range

Figure 27 is a flowchart of one technique to find the optimum VGA gain setting during calibration. Calibration begins with a VGA gain setting of 1V/V and increments the VGA gain until one of the four possible results occur. Result 1 is the desired outcome, where the signal falls into the range shown in *Figure 26* and the VGA calibration has been successful.

Applications Information (Continued)

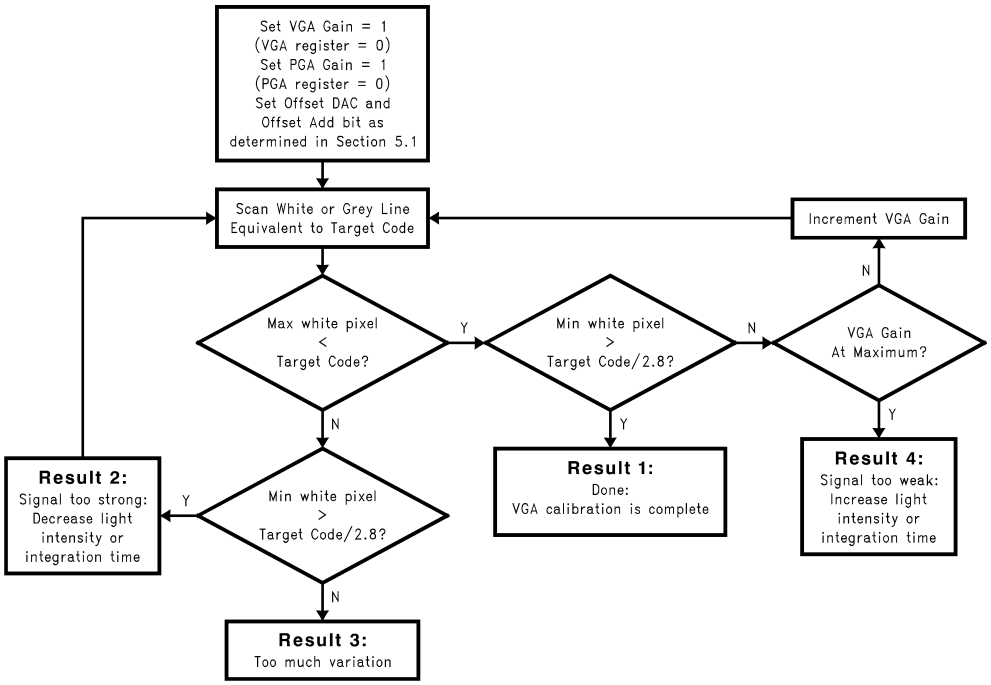


FIGURE 27. VGA Calibration Flowchart

There are several conditions that can cause the VGA gain calibration routine to fail. Result 2, "Signal is too strong: Decrease light intensity or integration time" is shown in *Figure 28*. This condition indicates that the amplitude of one or more of the white pixels coming from the CCD is greater than the maximum input voltage that the LM9801 is capable of accepting (about 1.2Vp-p). In this case the amplitude of the analog CCD output must be reduced before it enters the LM9801's OS input to prevent clipping. This can be done by reducing the intensity of the light source or shortening the integration time of the CCD.

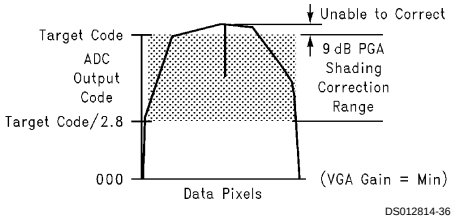


FIGURE 28. CCD Input Signal Too Strong

The second possible failure mode of the VGA calibration (Result 3) occurs if there is "Too much variation" in the amplitude of the pixels coming from the CCD *(Figure 29)*. The LM9801 can correct for up to a 2.8 to 1 variation in pixel amplitude. If the variation is greater than this than it must be reduced before it can perform shading correction on all the pixels. Typically this is done by using a better light source that has more uniform illumination, higher quality lenses, or other opto-mechanical techniques to reduce variation across all the active pixels.

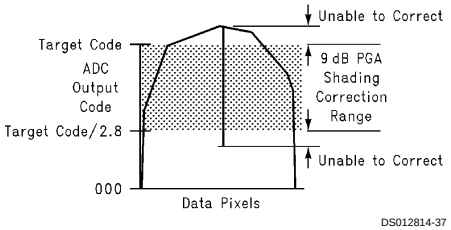


FIGURE 29. CCD Input Signal Range Too Wide

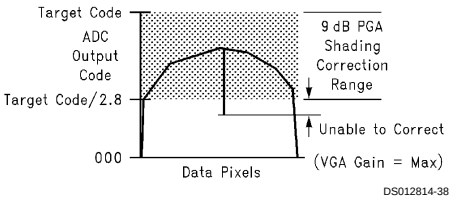


FIGURE 30. CCD Input Signal Too Weak

The final problem that can occur during VGA calibration (Result 4) is the "Signal too weak: increase light intensity or integration time" condition, shown in *Figure 30*. In this case,

Applications Information (Continued)

even with the VGA gain set to a maximum of 2.8, the amplitude of one or more pixels is less than the minimum required for shading correction. The solution is to increase the intensity of the light source or lengthen the integration time of the CCD to increase the CCD's output amplitude.

To ensure that a scanner system is manufacturable, the result of the VGA calibration must always be State 1. States 2, 3, and 4 must be eliminated either by ensuring that the total variation in light intensity (from all sources) from system to system to a maximum of 9 dB, or by being able to adjust the light source's intensity and/or the CCD's light integration time.

5.3 PGA Correction Coefficients (Shading Calibration)

Once the input signal has been centered inside the range the LM9801 can correct for, correction coefficients must be generated for each pixel to compensate for the gain error of that pixel.

1. Set Offset DAC and Add Bit as determined in Section 5.1.
2. Set the VGA gain to the value determined in Section 5.2.
3. Set the PGA gain to 0 dB.
4. Scan a reference line corresponding to all white or light grey and store it in memory.
5. Calculate the required gain correction coefficients for each pixel using the formula:

$$\text{Correction Coefficient}_n = \frac{256}{1.95}\left(\frac{\text{Target Code}}{\text{Uncorrected Code}_n} - 1\right)$$

Where **Uncorrected Code$_n$** is the ADC output code for pixel n with the PGA gain = 0 dB, **Target Code** is the number that corresponds to the desired output from the ADC with the given reference line input, and **Correction Coefficient$_n$** is the gain correction number that is sent to the CD0–CD7 correction databus to provide gain correction for pixel n when digitizing a line with the LM9801's PGA gain correction operating.

If it is difficult or undesirable to do the division, subtraction, and multiplication operations shown above for every pixel, then a lookup table can be generated in advance that will return the Correction Coefficient for any Uncorrected Code. This table can be stored in ROM or RAM and can speed up the calibration process. The disadvantage of this technique is that the Target Code must be fixed when the table is generated, so only one Target Code can be used (unless multiple tables are generated).

All the Correction Coefficients must be stored and sent to the LM9801 through the CD0–CD7 databus for every line scanned.

6.0 POWER SUPPLY CONSIDERATIONS

6.1 General

The LM9801 should be powered by a single +5V source (unless 3V-compatible digital I/O is required — see Section 6.2). The analog supplies (V_A) and the digital supplies (V_D and $V_{D(I/O)}$) are brought out individually to allow separate bypassing for each supply input. They should *not* be powered by two or more different supplies.

In systems with separate analog and digital +5V supplies, all the supply pins of the LM9801 should be powered by the analog +5V supply. Each supply input should be bypassed to its respective ground with a 0.1 µF capacitor located as close as possible to the supply input pin. A single 10 µF tantalum capacitor should be placed near the V_A supply pin to provide low frequency bypassing.

To minimize noise, keep the LM9801 and all analog components as far as possible from noise generators, such as switching power supplies and high frequency digital busses. If possible, isolate all the analog components and signals (OS, reference inputs and outputs, V_A, AGND) on an analog ground plane, separate from the digital ground plane. The two ground planes should be tied together at a single point, preferably the point where the power supply enters the PCB.

6.2 3V Compatible Digital I/O

If 3V digital I/O operation is desired, the $V_{D(I/O)}$ pin may be powered by a separate 3V ± 10% or 3.3V ± 10% supply. In this case, all the digital I/O pins (CD0–CD7, CCLK, MCLK, DD0–DD7, $\overline{EOC}$, $\overline{RD}$, SYNC, $\overline{CS}$, SCLK, SDO, and SDI) will be 3V compatible. The CCD clock signals (ϕ1, ϕ2, RS, and TR) remain 5V outputs, powered by V_D. In this case the $V_{D(I/O)}$ input should be bypassed to $DGND_{(I/O)}$ with a parallel combination of a 0.1 µF capacitor and a 10 µF tantalum capacitor.

6.3 Power Down Mode

Setting the Power Down bit to a "1" puts the device in a low power standby mode. The CCD outputs (ϕ1, ϕ2, RS, and TR) are pulled low and the analog sections are turned off to conserve power. The digital logic will continue to operate if MCLK continues and SYNC is held high, so for minimum power dissipation MCLK should be stopped when the LM9801 enters the Power Down mode. Recovery from Power Down typically takes 50 µs (the time required for the reference voltages to settle to 0.5 LSB accuracy).

7.0 COLOR

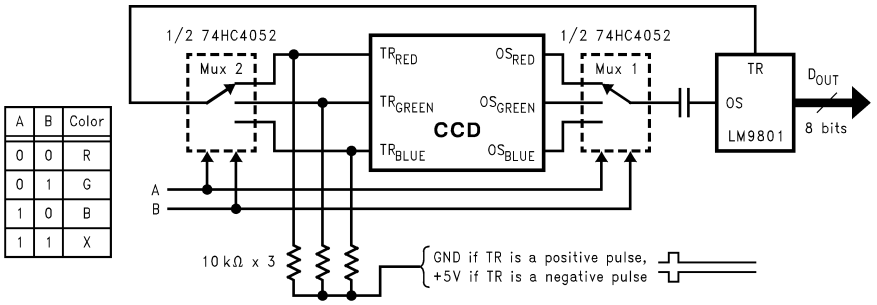
There are two primary ways to use the LM9801 in a color system with a triple output (RGB) CCD. The first is to use one LM9801 with an external multiplexer. This is the simplest solution. The second technique is to use one LM9801 per RGB color.

7.1 Parallel Output CCD, One LM9801

Figure 31 is an example of how to use a single LM9801 with a triple-output RGB CCD. In this case an entire line of red is digitized, followed by an entire line of green, then blue. This solution provides a 2.5 Mpixels/sec (for an effective 830k RGB pixels/sec after de-interleaving) pixel rate using a high performance triple output color CCD.

The Mux 1 multiplexer, located between the CCD's OS outputs and the LM9801's OS input, selects the color to be digitized according to the states of the A and B inputs (described below). The multiplexer's speed requirements are minimal because the mux switches at the line rate, not the pixel rate. Also, since the output of the mux goes into a high impedance, low-capacitance input, the ON resistance of the mux is not critical. The 74HC4052 is a good choice for this application.

Applications Information (Continued)



A	B	Color
0	0	R
0	1	G
1	0	B
1	1	X

FIGURE 31. Parallel Output CCD Application Circuit

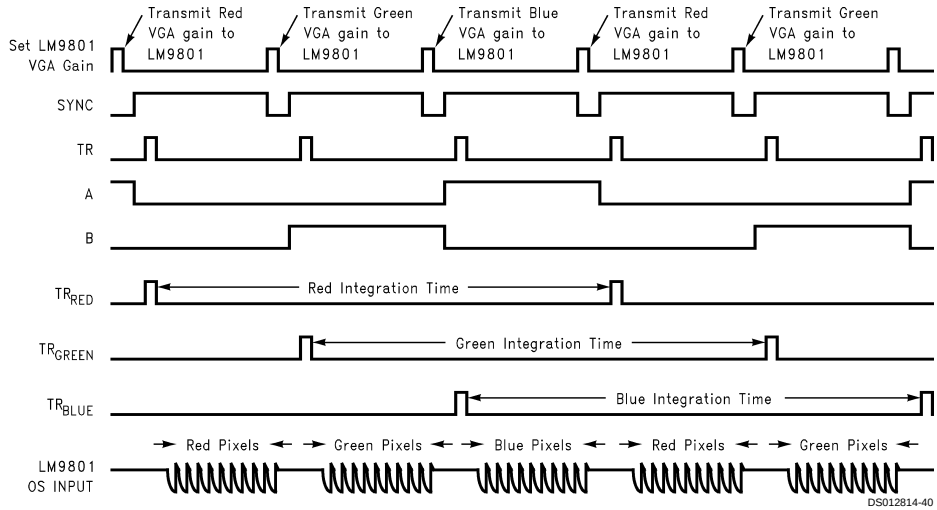


FIGURE 32. Parallel Output CCD Timing

To maximize the integration time for the Red, Green, and Blue photodiodes, the transfer (TR) pulses should be staggered as shown in *Figure 32*. This is done by a demultiplexer (Mux 2) between the TR output of the LM9801 and the transfer gate inputs of the CCD. If the CCD's transfer gate input capacitance is relatively low (see the CCD datasheet for this specification and the requirements for TR pulse rise and fall time), then the other half of the 74HC4052 may be used to switch the TR pulses as shown. If the TR gate input capacitance is so large that the minimum TR rise and fall times can not be met because of the 200Ω max on resistance of the 74HC4052's switches, then the 74HC4052 can not be used to multiplex the TR output and should be replaced with an active device such as the 74HC155 dual 2-to-4 demultiplexer.

Two signals (A and B) must be generated to choose which color is going to be digitized and receives the TR pulse. These signals can be as simple as the output of a two bit counter that counts from 0 to 2 (0, 1, 2, 0, 1, 2, etc.). This counter should be incremented after the end of the previous line and before the first transfer pulse of the next line. Also, since each color will need a different VGA gain, the appropriate VGA gain value for each color should be sent to the LM9801 during this time.

7.2 Parallel Output CCD, Three LM9801's

Figure 33 uses three LM9801s to achieve a 7.5 Mpixel/sec (2.5M RGB pixels/sec) pixel rate. The three LM9801s are synchronized by applying the same MCLK and SYNC signals to all three devices. One LM9801 provides the clock signals required for the CCD. Since the coefficient data for all three LM9801s will be latched simultaneously on the rising edge of CCLK, the correction coefficient bus must either be at least 24 bits wide (8 correction coefficient bits by 3 LM9801s) or run at a 7.5 MHz rate and be latched into a buffer between the correction coefficient databus and each LM9801. Similarly, the output data for all three LM9801s will be available simultaneously at the 3 output databusses. Since each LM9801 is dedicated to one color, the VGA gain does not change during line scan.

Applications Information (Continued)

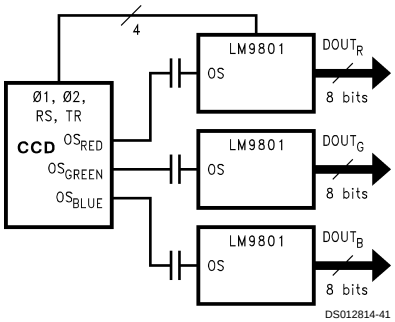


FIGURE 33. Parallel Output CCD, Three LM9801

8.0 A TYPICAL GREYSCALE APPLICATION

Figure 34 shows the interface between the LM9801 and a typical greyscale even/odd output CCD, the TCD1250. The interface for most other CCDs will be similar, the only difference being the values for the series resistors (if required).

The clamp capacitor value is determined as shown in Section 4.2. The resistor values are usually given in the CCD's datasheet. If the datasheet's requirement is given as a particular rise/fall time, the resistor can be chosen using the graph of **ϕ1, ϕ2, RS and TR Rise Times Through a Series Resistance vs Load Capacitance** graph in the **Typical Performance Characteristics** section. Given the required rise time and the input capacitance of the input being driven, the resistor value can be estimated from the graph.

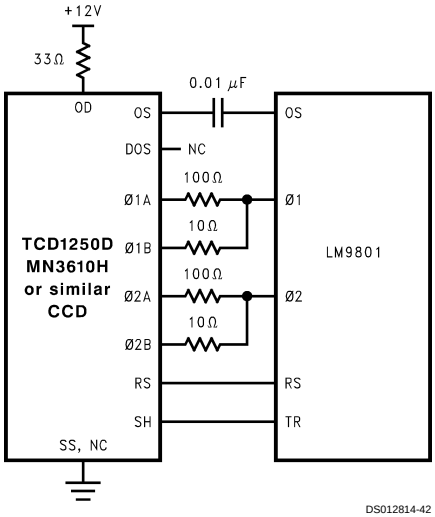


FIGURE 34. Greyscale CCD Interface Example

These are the Configuration Register parameters recommended for use as a starting point for most even/odd CCDs:

Mode = 1 (Even/Odd mode)*

RS Pulse Width = 0 (1 MCLK)

RS Pulse Polarity = 0*

RS Pulse Position = 10

Sample Reference Position = 14

Sample Signal Position = 8

ϕ1/ϕ2/RS/TR Enable = 1/1/1/1

TR Pulse Width = 0

TR-ϕ1 Guardband = 0

TR Polarity = 0*

Signal Polarity = 1

Dummy Pixels = 2*

Optical Black Pixels = 5*

(*Value given in CCD datasheet)

The Mode is set to Even/Odd, RS Pulse Width is set to its minimum value, and RS polarity is positive. The timing, shown in *Figure 35*, is determined by the RS, SR, and SS registers. The RS pulse position (RS) is set to 10, dividing the pixel period so that the *signal* portion is available for the first 5 MCLKs following a ϕ1 clock edge and the *black reference* portion appears during the last 2 MCLKs (following the 1 MCLK wide reset pulse). Sample Reference (SR) is set to 14, so it samples the black reference just before the next ϕ1 clock edge. Sample Signal (SS) is set to 8, so it samples the black reference just before the next reset pulse. These values can be adjusted to account for differences in CCDs, CCD data delays, settling time, etc., but this is often not necessary.

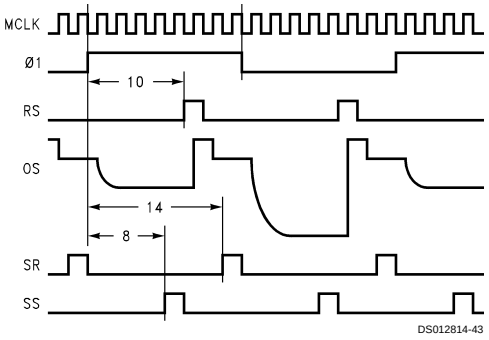


FIGURE 35. Typical Even/Odd Timing

All 4 digital outputs (ϕ1, ϕ2, RS, and TR) are enabled. The TR pulse width is set to the minimum, 20 MCLKs, as is the guardband between ϕ1 and TR. Either of these settings can be increased if necessary.

The TR polarity is positive, as is the RS polarity. Some CCDs may require one or both of these signals to be inverted, in which case the corresponding bit can be set to a "1". If there is an inverting buffer between the LM9801 and the CCD, these bits may be used to correct the output polarity at the CCD. Note that if ϕ1 and ϕ2 are inverted, then $\overline{\phi 2}$ should be used as ϕ1 at the CCD, and $\overline{\phi 1}$ should be used as ϕ2 at the CCD *(Figure 36)*.

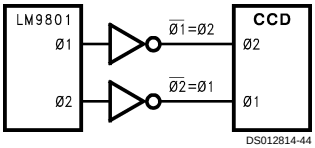


FIGURE 36. ϕ1 and ϕ2 After Inversion

Applications Information (Continued)

Since this is a CCD sensor, the Signal Polarity is set to a 1 (inverted) to match the CCD's output signal. The number of dummy pixels and optical black reference pixels are given in the CCD's datasheet. The dummy pixel register should be programmed with the number of dummy pixels in the CCD + 1 (for example, if the CCD has 16 dummy pixels then the register should contain 17). The optical black reference register should be programmed with the number of optical black pixels in the CCD.

The PGA gain coefficient register and PGA Gain Source bit are used during calibration (see Section 5.0). The Power Down bit should be set to 0 for normal operation. The Offset Add bit is also programmed during calibration.

The VGA and Offset DAC bits are programmed during calibration (Section 5.0). The Test Mode bits should always be set to "0".

9.0 TYPICAL CIS APPLICATION

Many CIS sensors (such as those made by Dyna Image Corporation) have only one clock input, a transfer signal, and an output signal that is referred to ground *(Figure 37)*. *Figure 38* shows the analog and digital circuitry required to connect a typical Dyna CIS to the LM9801.

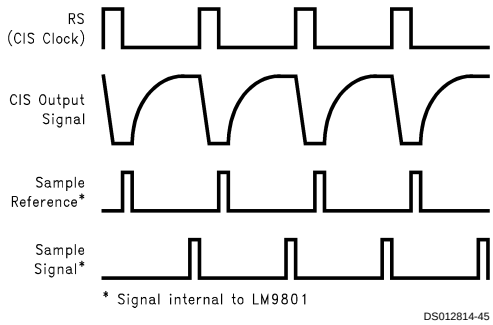


FIGURE 37. CIS Waveforms

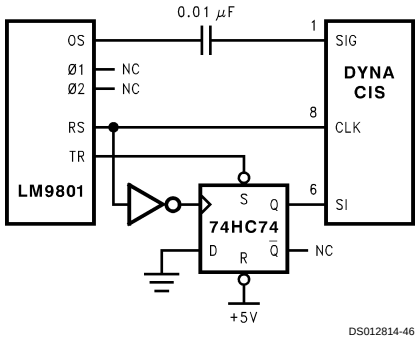


FIGURE 38. Minimum CIS Interface

Because the CIS requires only one clock with a duty cycle of less than 50%, the LM9801's RS output is used as the CIS's CLK source. ϕ1 and ϕ2 are not used. The 74HC74 D flip-flop is used to lengthen the transfer pulse (SI, or "Shift In" on the CIS) so that it overlaps the first RS pulse and meets the timing requirement of the CIS (see *Figure 39*).

The final "trick" required to interface a CIS to the LM9801 is the generation of optical black pixels for the LM9801 to clamp to at the beginning of a line. Unlike CCDs, CIS devices do not have a sequence of optical black pixels at the beginning of a line — the first pixel out of a CIS is valid image data. There are several ways to create black pixels for the LM9801 to clamp to.

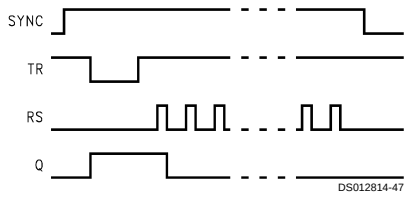


FIGURE 39. CIS Interface Digital Timing

The simplest solution is to physically place a light shield (black plastic, tape or metal) over the first 10 or so pixels. This reduces the voltage output of the CIS to nearly 0V, which is adequate for the LM9801 to clamp to. This has the side effect of slightly reducing the number of active pixels available for image capture.

A second option is to artifically generate "black" pixels by holding the CLOCK input high for 10 or so RS pulses *(Figure 40)*. This forces the output voltage to zero for the time that the CLOCK input is high, and only one active image pixel is lost. The BLACK signal could be generated by the ASIC/external logic that generates a pulse on the first rising edge of RS after the TR pulse.

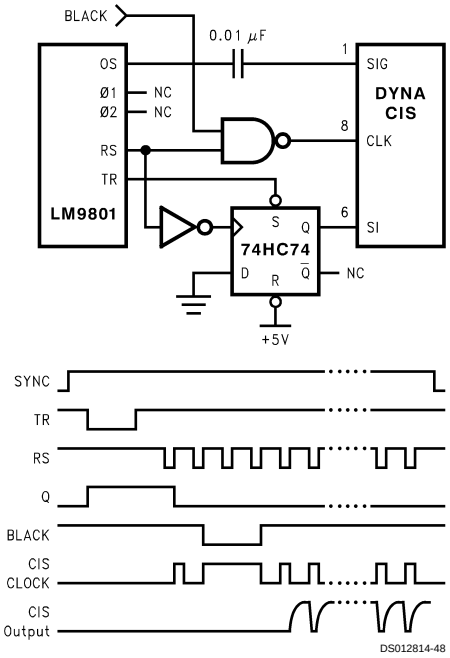


FIGURE 40. Generating Artificial Black Pixels

Applications Information (Continued)

Suggested timing for CIS devices is:

Mode = 0 (Standard Mode)*
RS Pulse Width = 0 (2 MCLKs)
RS Pulse Polarity = 0 (or 1 if circuit of *Figure 40* is used)*
RS Pulse Position = 0
Sample Reference Position = 2
Sample Signal Position = 14
ϕ1/ϕ2/RS/TR Enable = 0/0/1/1
TR Pulse Width = 0
TR-ϕ1 Guardband = 0
TR Polarity = 1*
Signal Polarity = 0
Dummy Pixels = 2
Optical Black Pixels = 10
(*Value given in CCD datasheet)

As CIS sensors approach pixel rates of 1 MHz and above (corresponding to MCLK frequencies of 8 MHz and above), the voltage during the reset level becomes less stable, making it difficult to perform CDS on the output *(Figure 41)*. The solution is to create the ground reference externally, shorting the LM9801's input to ground for half of the time using the ϕ1 clock, as shown in *Figure 42*.

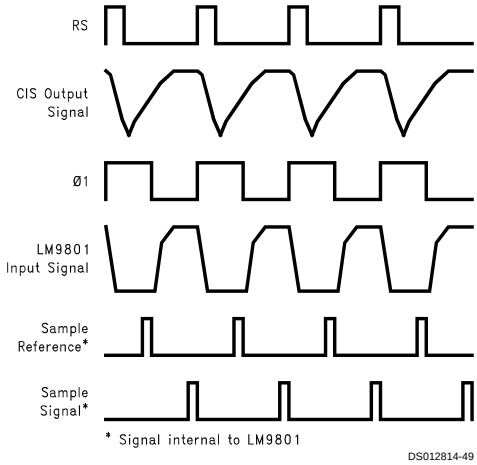


FIGURE 41. High Speed CIS Waveforms

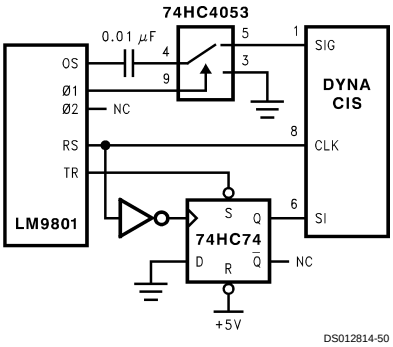


FIGURE 42. High Speed CIS Interface

10.0 HINTS AND COMMON SYSTEM DESIGN PROBLEMS

10.1 Reading and Writing to the Configuration Register

The Configuration Register sends and receives data LSB (Least Significant Byte) first. Some microcontrollers send out data MSB (Most Significant Byte) first. The order of the bits must be reversed to when using these microcontrollers.

Note: Unlike the LM9800, the SYNC pin does not have to be held high to send or receive data to or from the Configuration Register.

10.2 Setting the Dummy and Optical Black Pixel Registers

The minimum value in the Dummy Pixels register is 2 (a value of 0 or 1 will cause errors in the EOC and CCLK timing). Note that the value in this register should be equal to 1 plus the actual number of dummy pixels in the CCD. For example, if the CCD being used with the LM9801 has 12 dummy pixels, this register should be set to 13. The minimum number in the Optical Black Pixels register is 1.

10.3 Stretching the TR-ϕ1 Guardband

Some CCDs (Sony's ILX514, ILX518, and ILX524, for example) require a TR to ϕ1 guardband greater than the 100 ns (2 MCLKs) provided by the LM9801. The circuit shown in *Figure 43* produces a 1 µs ϕROG (transfer) pulse with a guardband between the end of the ϕROG pulse and the next edge of ϕ1. This is done by setting the LM9801's TR pulse width register to 2 µs and using the 74HC4538 to generate a 1 µs pulse inside that TR period to send to the CCD.

Applications Information (Continued)

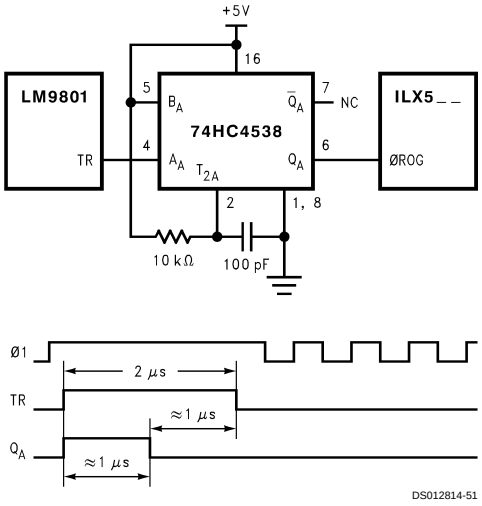


FIGURE 43. Stretching the TR-ϕ1 Guardband

Figure 44 shows a different technique for increasing the TR-ϕ1 guardband and/or increasing the length of the TR pulse by stopping the MCLK during the TR period. When TR initially goes high, the first one-shot (U1A) triggers, effectively disabling the LM9801's MCLK for ≈ 2 µs, thereby lengthening the TR pulse width by ≈ 2 µs over the value programmed in the configuration register. On the falling edge of TR, the second one-shot (U1B) fires, disabling the LM9801's MCLK for ≈ 1 µs and increasing the TR-ϕ1 guardband by that amount.

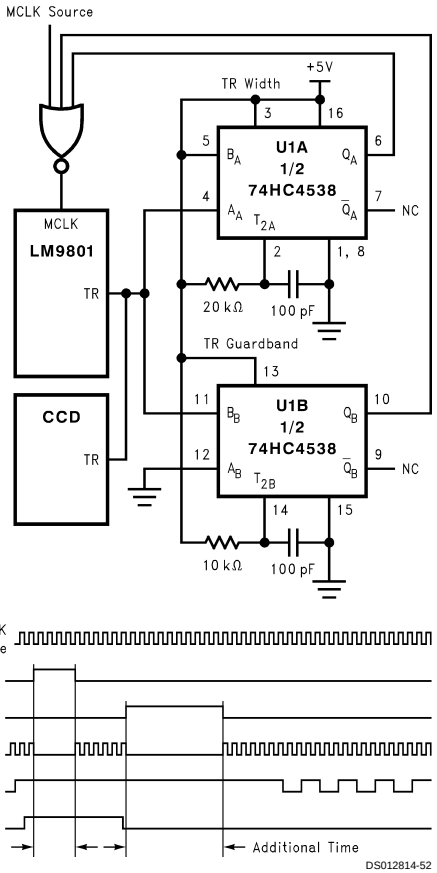
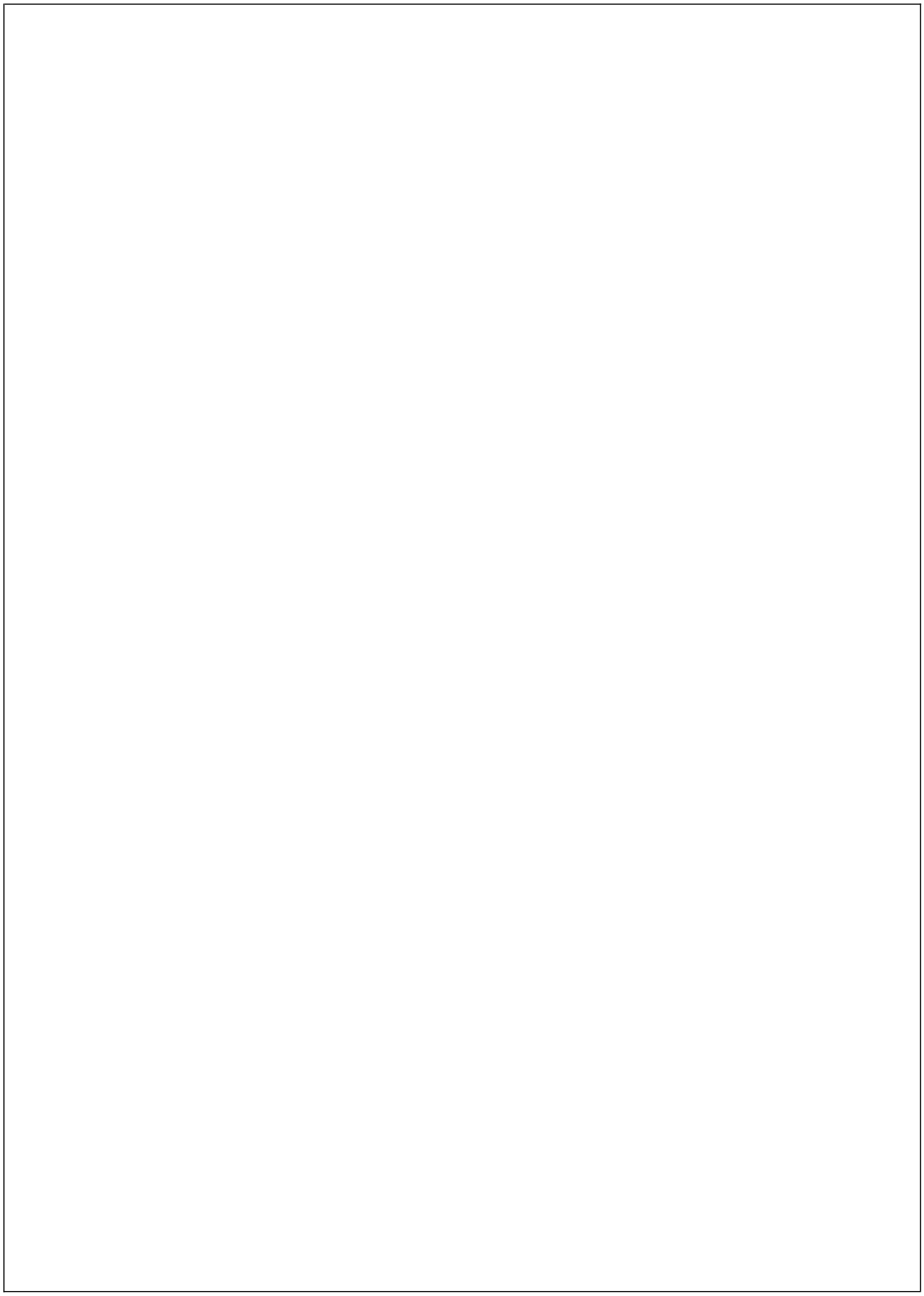
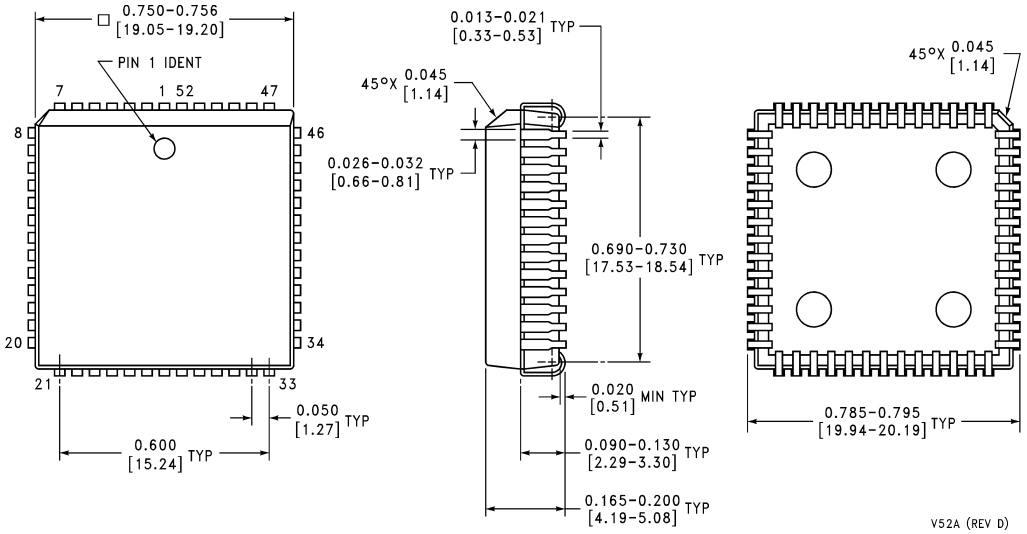


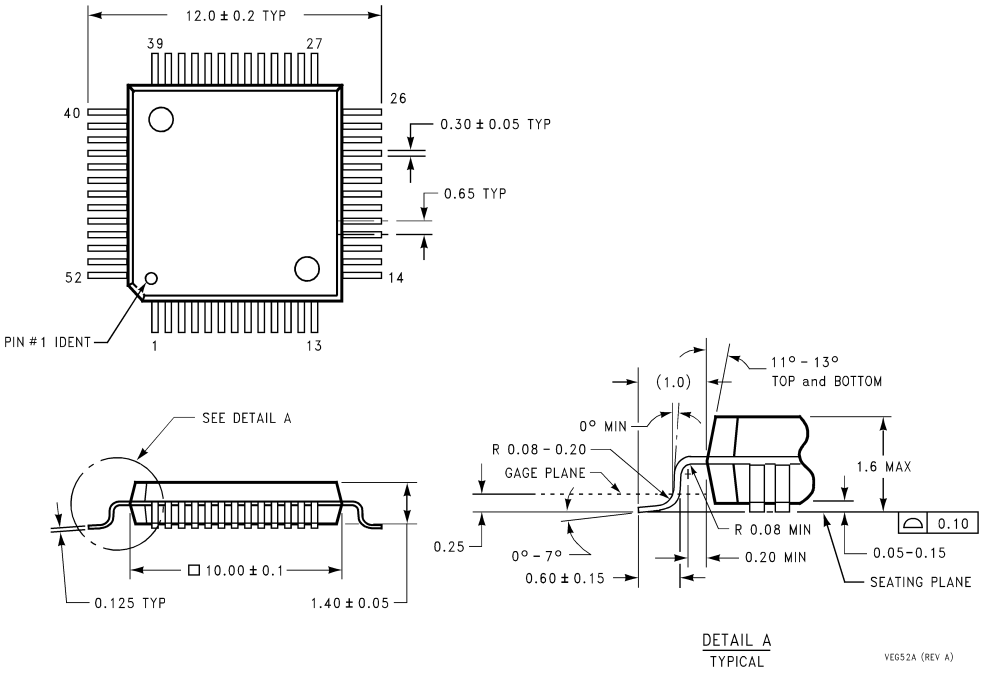
FIGURE 44. Stretching TR and the TR-ϕ1 Guardband



Physical Dimensions inches (millimeters) unless otherwise noted



52-Pin Plastic Leaded Chip Carrier (PLCC)
Order Number LM9801CCV
NS Package Number V52A



Dimensions are in millimeters

52-Pin Thin Quad Flatpak
Order Number LM9801CCVF
NS Package Number VEG52A

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