National Semiconductor

February 2005

LM4925 Boomer® Audio Power Amplifier Series
2 Cell, Single Ended Output, 40mW Stereo Headphone Audio Amplifier

General Description

The unity gain stable LM4925 is both a mono differential output (for BTL operation) audio amplifier and a Single Ended (SE) stereo headphone amplifier. Operating on a single 3V supply, the mono-BTL mode delivers 410mW into an 8Ω load at 1% THD+N. In Single Ended stereo headphone mode, the amplifier delivers 40mW per channel into a 16Ω load at 1% THD+N.

With the LM4925 packaged in the MM and LLP packages, the customer benefits include low profile and small size. This package minimizes PCB area and maximizes output power.

The LM4925 features circuitry that reduces output transients ("clicks" and "pops") during device turn-on and turn-off, an externally controlled, low-power consumption, active-low shutdown mode, and thermal shutdown. Boomer audio power amplifiers are designed specifically to use few external components and provide high quality output power in a surface mount package.

Key Specifications

- Mono-BTL Output Power
- (R_L = 8Ω, V_{DD} = 3.0V, THD+N = 1%) 410mW (typ)
- Single Ended Output Power Per Channel
- (R_L = 16Ω, V_{DD} = 3.0V, THD+N = 1%) 40mW (typ)
- Micropower shutdown current 0.1µA (typ)
- Supply voltage operating range 1.5V < V_{DD} < 3.6V
- PSRR 100Hz, V_{DD} = 3V, BTL 70dB (typ)

Features

- BTL mode for mono speaker
- 2-cell 1.5V to 3.6V battery operation
- Single ended headphone operation with output coupling capacitors
- Unity-gain stable
- "Click and pop" suppression circuitry for both Shutdown and Mute
- Active low micro-power shutdown
- Active-low mute mode
- Thermal shutdown protection circuitry

Applications

- Portable two-cell audio products
- Portable two-cell electronic devices

Typical Application

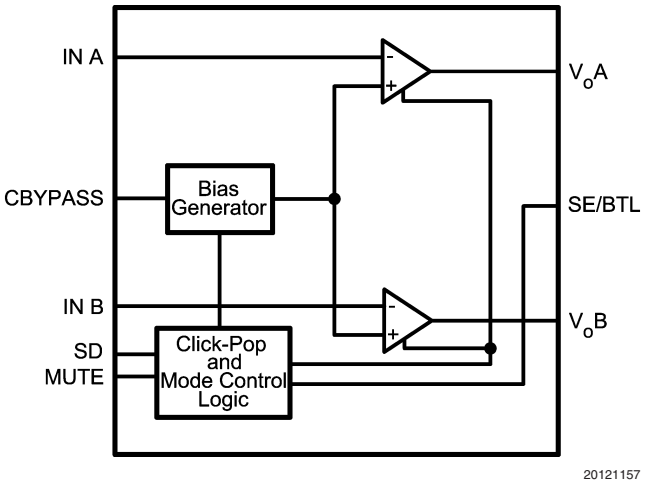
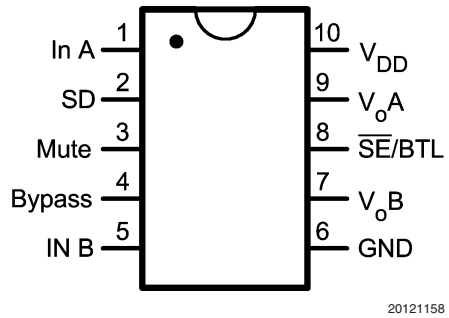


FIGURE 1. Block Diagram

Boomer® is a registered trademark of National Semiconductor Corporation.

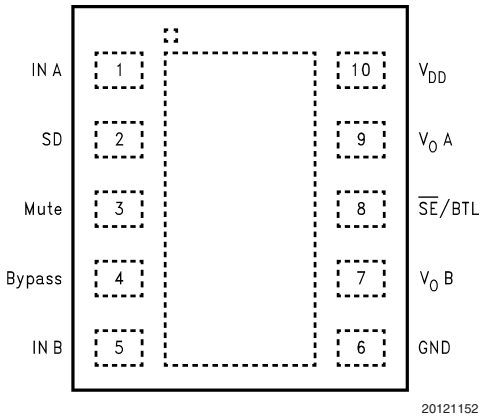
Connection Diagrams

MSOP Package



Top View
Order Number LM4925MM
See NS Package Number MUB10A for MSOP

LD Package



Top View
Order Number LM4925SD
See NS Package Number SDA10A

Typical Connections

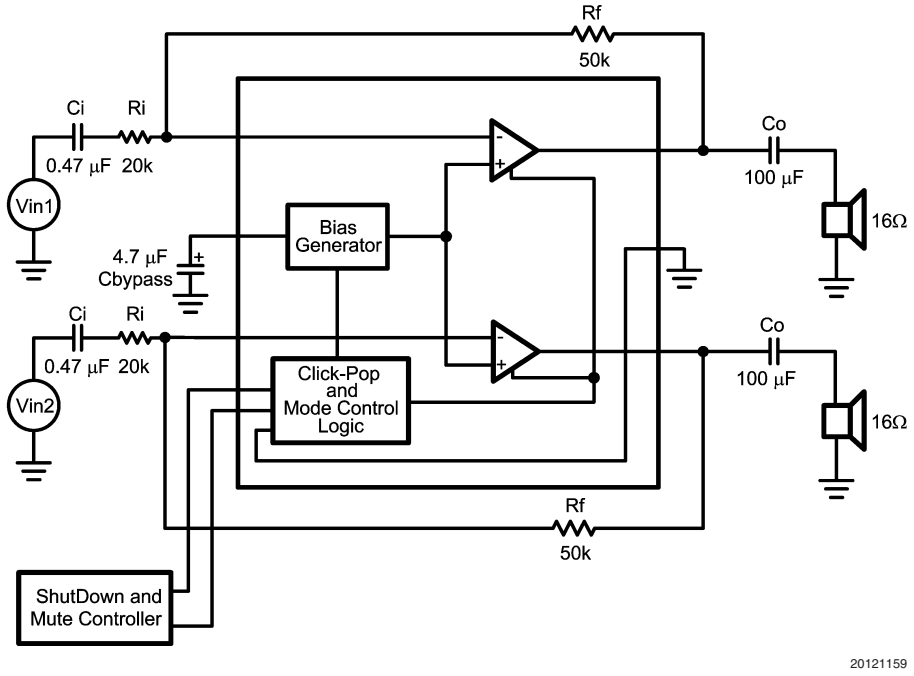


FIGURE 2. Typical Capacitive Couple (SE) Output Configuration Circuit

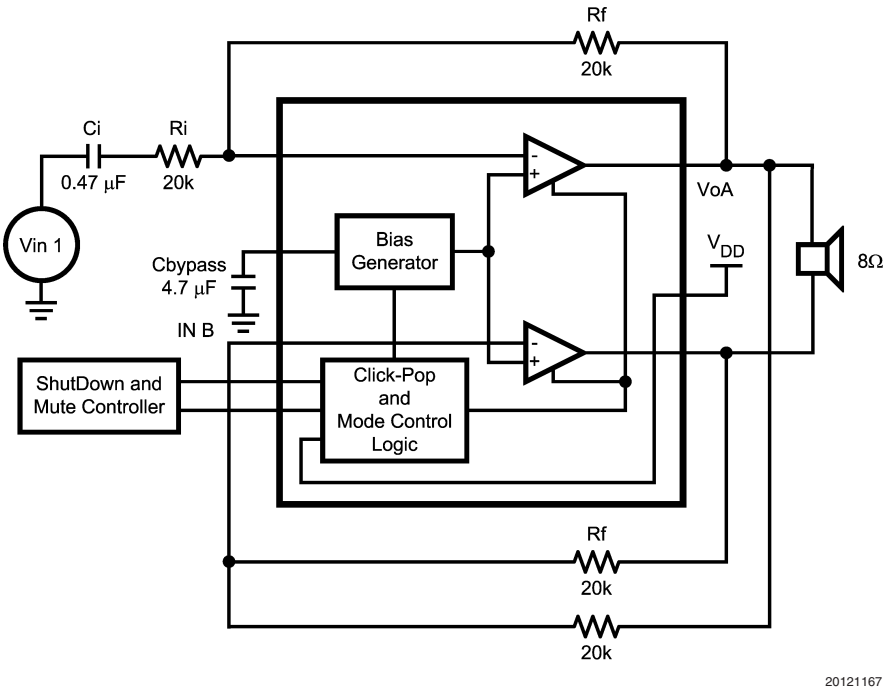


FIGURE 3. Typical BTL Speaker Configuration Circuit

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	3.8V
Storage Temperature	−65˚C to +150˚C
Input Voltage	−0.3V to V_{DD} +0.3V
Power Dissipation (Note 2)	Internally limited
ESD Susceptibility(Note 3)	2000V
ESD Susceptibility (Note 4)	200V
Junction Temperature	150˚C
Solder Information	
Small Outline Package Vapor Phase (60sec)	215˚C
Infrared (15 sec)	220˚C

See AN-450 “Surface Mounting and their Effects on Product Reliablilty” for other methods of soldering surface mount devices.

Thermal Resistance	
θ_{JA} (typ) MUB10A	175˚C/W
θ_{JA} (typ) LDA10A	73˚C/W

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40˚C \le T_A \le +85˚C$
Supply Voltage	$1.5V \le V_{DD} \le 3.6V$

Electrical Characteristics V_{DD} = 3.0V (Notes 1, 5)

The following specifications apply for the circuit shown in Figure 2 for Single Ended Outputs (A_V = 2.5V) and Figure 3 for BTL Outputs ($A_{V\text{-}BTL}$ = 2), unless otherwise specified. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4925		Units (Limits)
			Typical (Note 6)	Limit (Note 7)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A, R_L = ∞ (Note 8)	1.0	1.6	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = GND	0.1	1	µA (max)
V_{OS}	Output Offset Voltage		2	10	mV (max)
P_O	Output Power (Note 9)	R_L = 8Ω, BTL, Fig. 3, THD+N = 1%, f = 1kHz	410	350	mW (min)
		R_L = 16Ω, Fig. 2, SE per Channel, THD+N = 1%, f = 1kHz	40	30	mW (min)
THD+N	Total Harmonic Distortion + Noise	R_L = 8Ω, BTL, P_O = 300mW, Fig. 3, f = 1kHz	0.1	0.5	% (max)
		R_L = 16Ω, SE, P_O = 20mW per channel, Fig.2, f = 1kHz	0.05		
V_{NO}	Output Voltage Noise	20Hz to 20kHz, A-weighted, Input Referred, Single Ended Output, Fig. 2	10		μV_{RMS}
Crosstalk		R_L = 16Ω, Fig. 2	58		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200m$V_{P\text{-}P}$ sine wave C_{BYPASS} = 4.7µF, R_L = 8Ω f = 100Hz, BTL, Fig. 3	70		dB
		V_{RIPPLE} = 200m$V_{P\text{-}P}$ sine wave C_{BYPASS} = 4.7µF, R_L = 16Ω f = 100Hz, SE, Fig. 2	68		dB
V_{IH}	Control Logic High	$1.5V \le V_{DD} \le 3.6V$		$0.7V_{DD}$	V (min)
V_{IL}	Control Logic Low	$1.5V \le V_{DD} \le 3.6V$		$0.3V_{DD}$	V (max)
Mute Attenuation		$1V_{PP}$ Reference, R_i = 20k, R_f = 50k		70	dB (min)

Electrical Characteristics V_{DD} = 1.8V (Notes 1, 5)

The following specifications apply for the circuit shown in Figure 2 for Single Ended Outputs (A_V = 2.5V) and Figure 3 for BTL Outputs (A_{V-BTL} = 2), unless otherwise specified. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4925		Units (Limits)
			Typical (Note 6)	Limit (Note 7)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A, R_L = ∞ (Note 8)	0.9	1.6	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = GND	0.05	1	µA (max)
V_{OS}	Output Offset Voltage		2	10	mV (max)
P_O	Output Power (Note 9)	R_L = 8Ω, BTL, Fig. 3, THD+N = 1%, f = 1kHz	120	90	mW (min)
		R_L = 16Ω, Fig. 2, SE per Channel, THD+N = 1%, f = 1kHz	10	7	mW (min)
THD+N	Total Harmonic Distortion + Noise	R_L = 8Ω, BTL, P_O = 50mW, Fig. 3, f = 1kHz	0.15	0.5	% (max)
		R_L = 16Ω, SE, P_O = 5mW per channel, Fig.2, f = 1kHz	0.1		
V_{NO}	Output Voltage Noise	20Hz to 20kHz, A-weighted, Input Referred, Single Ended Output, Fig. 2	10		μV_{RMS}
Crosstalk		R_L = 16Ω, Fig. 2	58		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{P-P} sine wave C_{BYPASS} = 4.7µF, R_L = 8Ω f = 100Hz, BTL, Fig. 3	70		dB
		V_{RIPPLE} = 200mV_{P-P} sine wave C_{BYPASS} = 4.7µF, R_L = 16Ω f = 100Hz, SE, Fig. 2	68		dB
V_{IH}	Control Logic High	1.5V ≤ V_{DD} ≤ 3.6V		$0.7V_{DD}$	V (min)
V_{IL}	Control Logic Low	1.5V ≤ V_{DD} ≤ 3.6V		$0.3V_{DD}$	V (max)
Mute Attenuation		$1V_{PP}$ Reference, R_i = 20k, R_f = 50k		70	dB (min)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 2: The maximum power dissipation is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A and must be derated at elevated temperatures. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$. For the LM4925, T_{JMAX} = 150˚C. For the θ_{JA}s, please see the Application Information section or the Absolute Maximum Ratings section.

Note 3: Human body model, 100pF discharged through a 1.5kΩ resistor.

Note 4: Machine model, 220pF–240pF discharged through all pins.

Note 5: All voltages are measured with respect to the ground (GND) pins unless otherwise specified.

Note 6: Typicals are measured at 25˚C and represent the parametric norm.

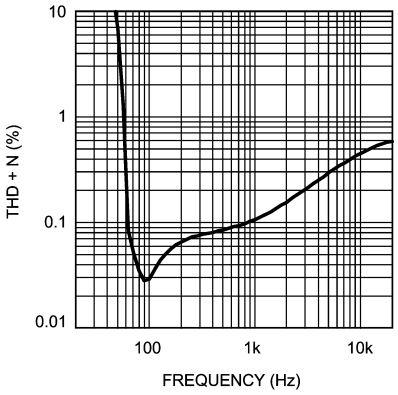
Note 7: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Note 8: The quiescent power supply current depends on the offset voltage when a practical load is connected to the amplifier.

Note 9: Output power is measured at the device terminals.

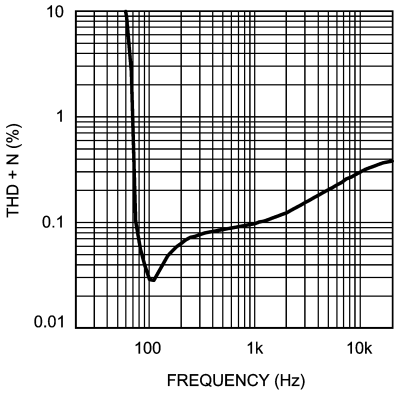
Typical Performance Characteristics

THD+N vs Frequency
V_{DD} = 1.8V, SE, R_L = 16Ω
P_O = 5mW per channel



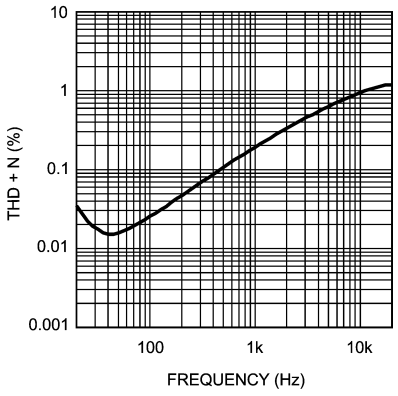
20121108

THD+N vs Frequency
V_{DD} = 3V, SE, R_L = 16Ω
P_O = 20mW per channel



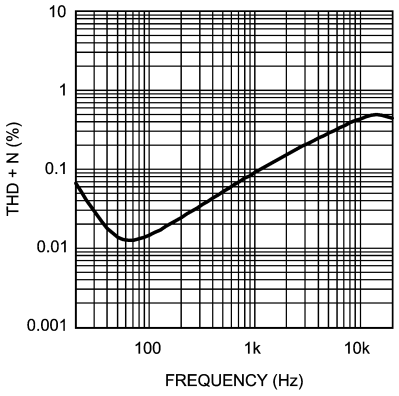
20121110

THD+N vs Frequency
V_{DD} = 1.8V, BTL, R_L = 8Ω
P_O = 50mW



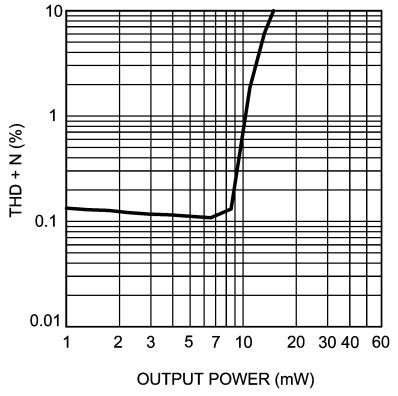
20121107

THD+N vs Frequency
V_{DD} = 3V, BTL, R_L = 8Ω
P_O = 300mW



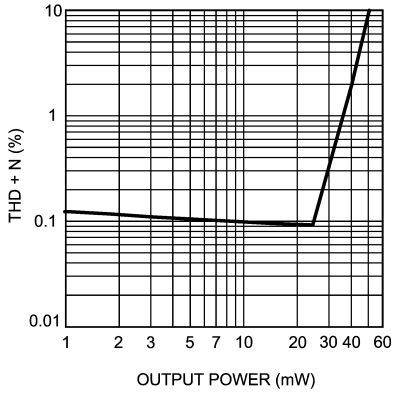
20121109

THD+N vs Output Power
V_{DD} = 1.8V, SE, R_L = 16Ω
f = 1kHz, Both channels



20121112

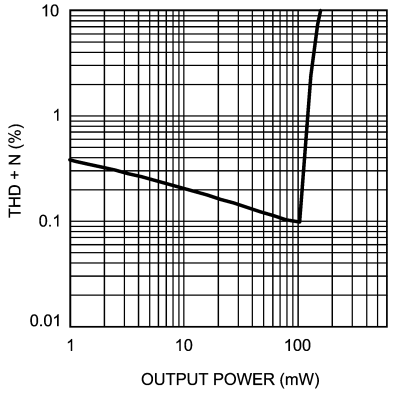
THD+N vs Output Power
V_{DD} = 3V, SE, R_L = 16Ω
f = 1kHz, Both channels



20121114

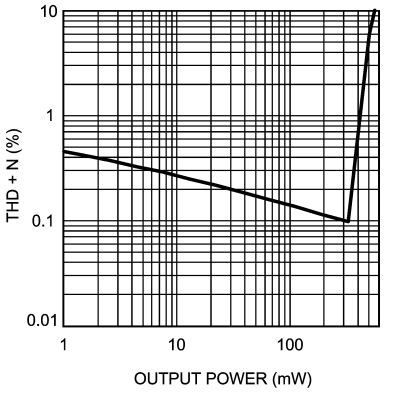
Typical Performance Characteristics (Continued)

THD+N vs Output Power
V_{DD} = 1.8V, BTL, R_L = 8Ω
f = 1kHz



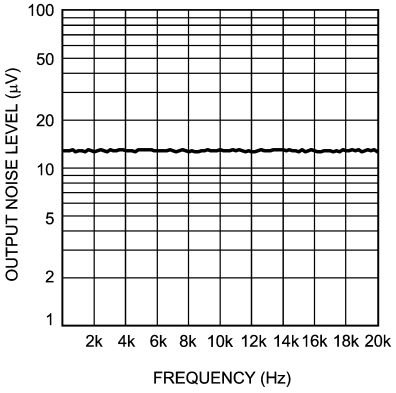
20121111

THD+N vs Output Power
V_{DD} = 3V, BTL, R_L = 8Ω
f = 1kHz



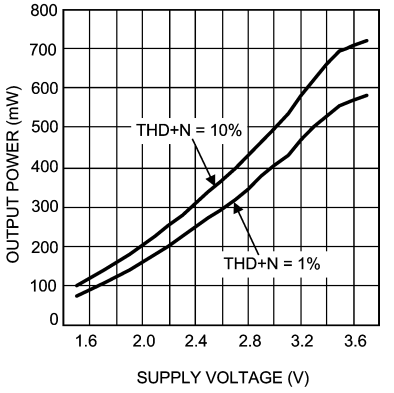
20121133

Output Noise vs Frequency



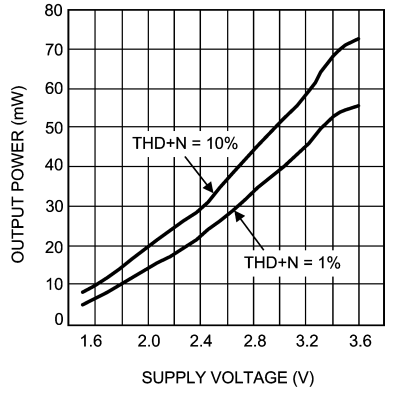
20121106

Output Power vs Supply Voltage
R_L = 8Ω, BTL, f = 1kHz



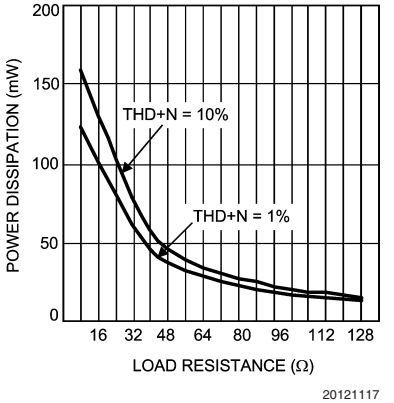
20121115

Output Power vs Supply Voltage
R_L = 16Ω, SE, f = 1kHz



20121116

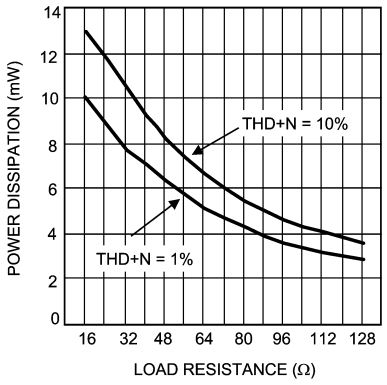
Output Power vs Load Resistance
V_{DD} = 1.8V, BTL, f = 1kHz



20121117

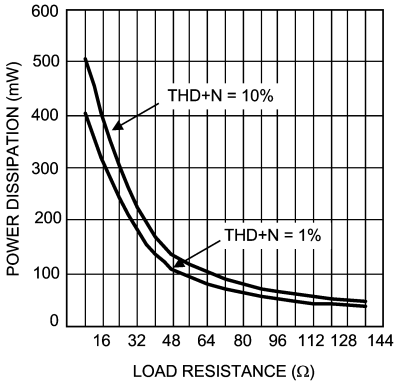
Typical Performance Characteristics (Continued)

Output Power vs Load Resistance
V_{DD} = 1.8V, SE, f = 1kHz



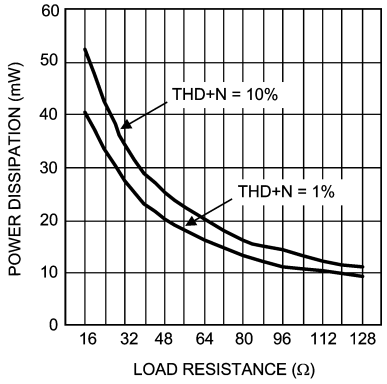
20121134

Output Power vs Load Resistance
V_{DD} = 3V, BTL, f = 1kHz



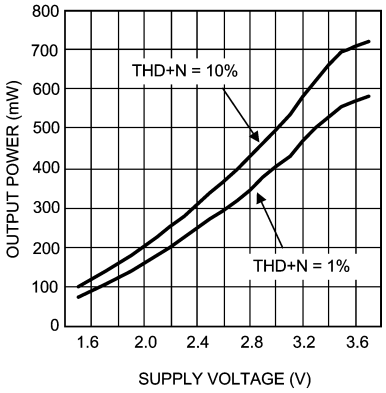
20121119

Output Power vs Load Resistance
V_{DD} = 3V, SE, f = 1kHz



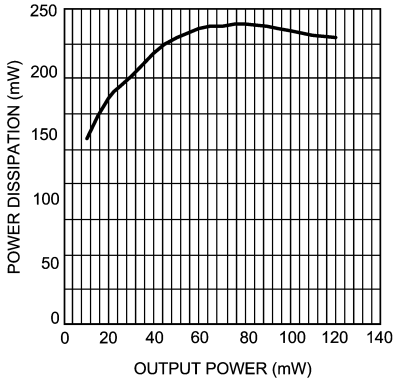
20121120

Output Power vs Supply Voltage
R_L = 8Ω, BTL, f = 1kHz



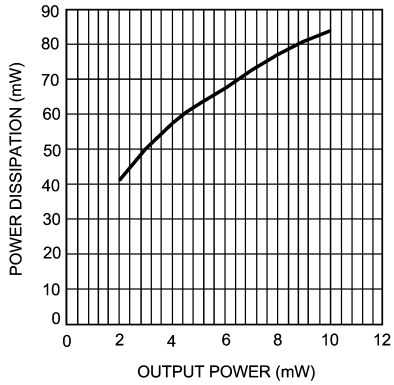
20121121

Power Dissipation vs Output Power
V_{DD} = 1.8V, R_L = 8Ω, BTL, f = 1kHz



20121123

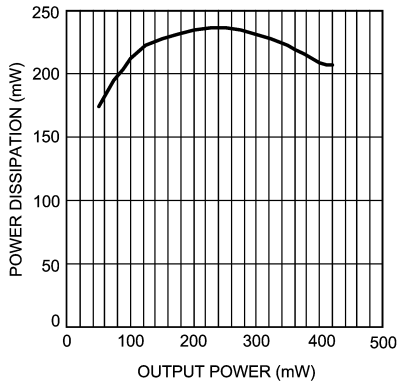
Power Dissipation vs Output Power
V_{DD} = 1.8V, R_L = 16Ω, SE, f = 1kHz



20121124

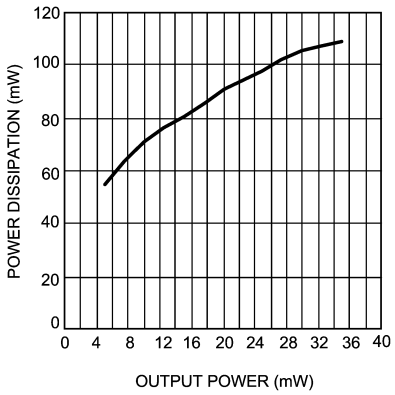
Typical Performance Characteristics (Continued)

Power Dissipation vs Output Power
V_{DD} = 3V, R_L = 8Ω, BTL, f = 1kHz



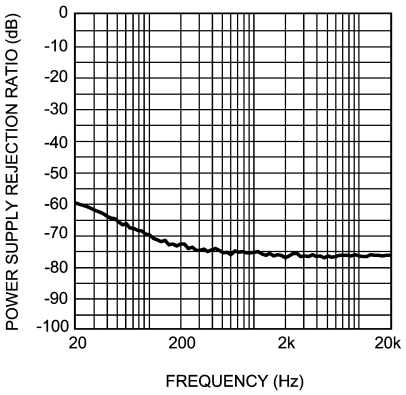
20121125

Power Dissipation vs Output Power
V_{DD} = 3V, R_L = 16Ω, SE, f = 1kHz



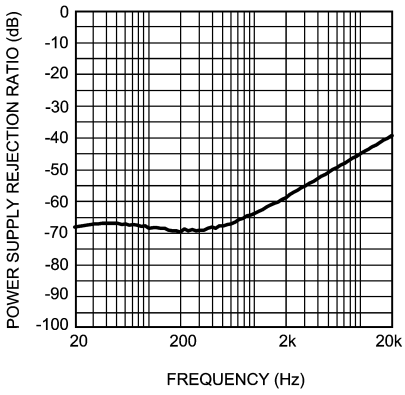
20121126

Power Supply Rejection vs Frequency
V_{DD} = 1.8V, R_L = 8Ω, BTL
V_{RIPPLE} = 200mVp-p, A_{V-BTL} = 2V/V



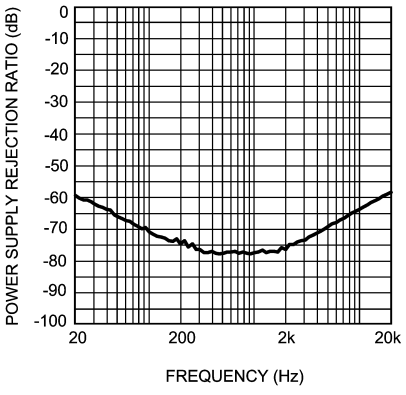
20121129

Power Supply Rejection vs Frequency
V_{DD} = 1.8V, R_L = 16Ω, SE
V_{RIPPLE} = 200mVp-p, A_V = 2.5V/V



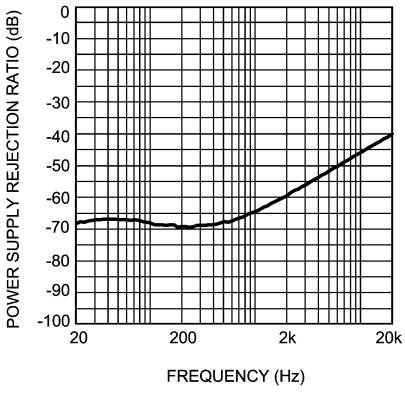
20121130

Power Supply Rejection vs Frequency
V_{DD} = 3V, R_L = 8Ω, BTL
V_{RIPPLE} = 200mVp-p, A_{V-BTL} = 2V/V



20121131

Power Supply Rejection vs Frequency
V_{DD} = 3V, R_L = 16Ω, SE
V_{RIPPLE} = 200mVp-p, A_V = 2.5V/V



20121132

Application Information

BRIDGE (BTL) CONFIGURATION EXPLANATION

The LM4925 is a stereo audio power amplifier capable of operating in bridged (BTL) mode. As shown in Figure 3, the LM4925 has two internal operational amplifiers. The first amplifier's gain is externally configurable, while the second amplifier should be externally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of Rf to Ri while the second amplifier's gain is fixed by the two external 20kΩ resistors. Figure 3 shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but out of phase by 180˚. Consequently, the differential gain for the IC is

$$A_{VD} = 2 * (R_f / R_i)$$

By driving the load differentially through outputs VoA and VoB, an amplifier configuration commonly referred to as "bridged mode" is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of the load is connected to ground. A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping, please refer to the Audio Power Amplifier Design section.

A bridge configuration, such as the one used in LM4925, also creates a second advantage over single-ended amplifiers. Since the differential outputs, VoA and VoB, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration.

MODE SELECT DETAIL

The LM4925 can be configured for either single ended (see Figure 2) or BTL mode (see Figure 3). When the $\overline{SE}$/BTL pin has a logic high (V_{DD}) applied to it, the LM4925 is in BTL mode. If a logic low (GND) is applied to $\overline{SE}$/BTL, the LM4925 operates in single-ended mode. The slew rate of V_{DD} must be greater than 2.5V/ms to ensure reliable Power on reset (POR). The circuit shown in Figure 4 presents an applications solution to the problem of using different supply voltages with different turn-on times in a system with the LM4925. This circuit shows the LM4925 with a 25-50kΩ. Pull-up resistor connected from the shutdown pin to V_{DD}. The shutdown pin of the LM4925 is also being driven by an open drain output of an external microcontroller on a separate supply. This circuit ensures that shutdown is disabled when powering up the LM4925 by either allowing shutdown to be high before the LM4925 powers on (the microcontroller powers up first) or allows shutdown to ramp up with V_{DD} (the LM4925 powers up first). This will ensure the LM4925 powers up properly and enters the correct mode of operation (BTL or SE). Please note that the $\overline{SE}$/BTL pin should be tied to GND for single-ended (SE) mode, and to Vdd for BTL mode.

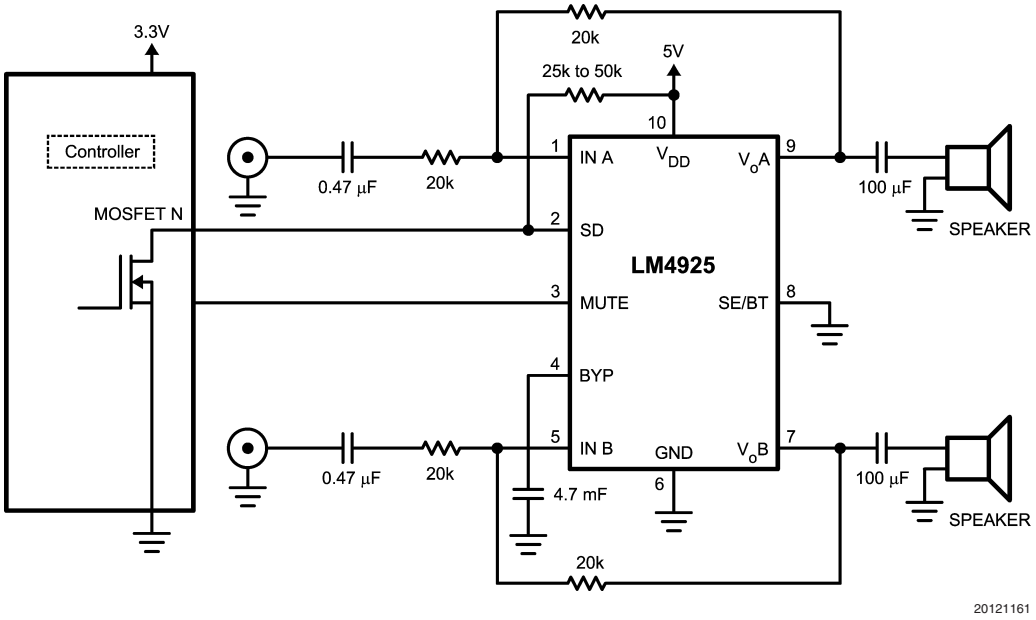


FIGURE 4. Recommended Circuit for Different Supply Turn-On Timing

Application Information (Continued)

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged (BTL) or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Since the LM4925 has two operational amplifiers in one package, the maximum internal power dissipation in BTL mode is 4 times that of a single-ended amplifier. The maximum power dissipation for a given application can be derived from the power dissipation graphs or from Equation 1.

$$P_{DMAX} = 4 * (V_{DD})^2 / (2\pi^2 R_L) \quad (1)$$

When operating in single ended mode, Equation 2 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2 / (2\pi^2 R_L) \quad (2)$$

Since the LM4925 has two operational amplifiers in one package, the maximum internal power dissipation point is twice that of the number that results from Equation 2.

The maximum power dissipation point obtained from either Equations 1, 2 must not be greater than the power dissipation that results from Equation 3:

$$P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA} \quad (3)$$

For package MUB10A, θ_{JA} = 175˚C/W. T_{JMAX} = 150˚C for the LM4925. Depending on the ambient temperature, T_A, of the system surroundings, Equation 3 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 1 or 2 is greater than that of Equation 3, then either the supply voltage must be decreased, the load impedance increased or T_A reduced. For the typical application of a 3.0V power supply, with an 16Ω load, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 129˚C provided that device operation is around the maximum power dissipation point. Thus, for typical applications, power dissipation is not an issue. Power dissipation is a function of output power and thus, if typical operation is not around the maximum power dissipation point, the ambient temperature may be increased accordingly. Refer to the Typical Performance Characteristics curves for power dissipation information for lower output powers.

POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is important for low noise performance and high power supply rejection. The capacitor location on the power supply pins should be as close to the device as possible. Typical applications employ a battery (or 3.0V regulator) with 10µF tantalum or electrolytic capacitor and a ceramic bypass capacitor that aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LM4925. A bypass capacitor value in the range of 0.1µF to 4.7µF is recommended.

MICRO POWER SHUTDOWN

The voltage applied to the SHUTDOWN pin controls the LM4925's shutdown function. Activate micro-power shutdown by applying a logic-low voltage to the SHUTDOWN pin. When active, the LM4925's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. A voltage that is higher than ground may increase the shutdown current. There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When using a switch, connect an external 100kΩ pull-up resistor between the SHUTDOWN pin and V_{DD}. Connect the switch between the SHUTDOWN pin and ground. Select normal amplifier operation by opening the switch. Closing the switch connects the SHUTDOWN pin to ground, activating micro-power shutdown. The switch and resistor guarantee that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or microcontroller, use a digital output to apply the control voltage to the SHUTDOWN pin. Driving the SHUTDOWN pin with active circuitry eliminates the pull-up resistor. Shutdown enable/disable times are controlled by a combination of C_{bypass} and V_{DD}. Larger values of C_{bypass} results in longer turn on/off times from Shutdown. Longer shutdown times also improve the LM4925's resistance to click and pop upon entering or returning from shutdown. For a 3.0V supply and C_{bypass} = 4.7µF, the LM4925 requires about 2 seconds to enter or return from shutdown. This longer shutdown time enables the LM4925 to have virtually zero pop and click transients upon entering or release from shutdown. Smaller values of C_{bypass} will decrease turn-on time, but at the cost of increased pop and click and reduced PSRR. When the LM4925 is in shutdown, the outputs become very low impedance (less than 5Ω to GND).

MUTE

The LM4925 also features a mute function that enables extremely fast turn-on/turn-off with a minimum of output pop and click. The mute function leaves the outputs at their bias level, thus resulting in higher power consumption than shutdown mode, but also provides much faster turn on/off times. Providing a logic low signal on the MUTE pin enables mute mode. Threshold voltages and activation techniques match those given for the shutdown function as well.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the LM4925 is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality. The LM4925 is unity-gain stable that gives the designer maximum system flexibility. The LM4925 should be used in low gain configurations to minimize THD+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1Vrms are available from sources such as audio codecs. Very large values should not be used for the gain-setting resistors. Values for Ri and Rf should be less than 1MΩ. Please refer to the section, Audio Power Amplifier Design, for a more complete explanation of proper gain selection. Besides gain, one of the major considerations is the closed-loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in Figures 2 and 3. The input coupling capacitor, Ci, forms a first order high pass

Application Information (Continued)

filter that limits low frequency response. This value should be chosen based on needed frequency response and turn-on time.

SELECTION OF INPUT CAPACITOR SIZE

Amplifying the lowest audio frequencies requires a high value input coupling capacitor, Ci. A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the headphones used in portable systems have little ability to reproduce signals below 60Hz. Applications using headphones with this limited frequency response reap little improvement by using a high value input capacitor. In addition to system cost and size, turn on time is affected by the size of the input coupling capacitor Ci. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage. This charge comes from the output via the feedback. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on time can be minimized. A small value of Ci (in the range of 0.1µF to 0.47µF), is recommended.

AUDIO POWER AMPLIFIER DESIGN

A 25mW/32Ω Audio Amplifier

Given:	
Power Output	10mWrms
Load Impedance	16Ω
Input Level	0.4Vrms
Input Impedance	20kΩ

A designer must first choose a mode of operation (SE or BTL) and determine the minimum supply rail to obtain the specified output power. By extrapolating from the Output Power vs. Supply Voltage graphs in the Typical Performance Characteristics section, the supply rail can be easily found. 3.0V is a standard voltage in most applications, it is chosen for the supply rail. Extra supply voltage creates headroom that allows the LM4925to reproduce peak in excess of 10mW without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the Power Dissipation section. Once the power dissipation equations have been addressed, the required gain can be determined from Equation 2.

$$A_V \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (4)$$

From Equation 4, the minimum AV is 1; use $A_V = 1$. Since the desired input impedance is 20k, and with a A_V gain of 1, a ratio of 1:1 results from Equation 1 for R_f to R. The values are chosen with $R_i = 20k$ and $R_f = 20k$. The final design step is to address the bandwidth requirements which must be stated as a pair of -3dB frequency points. Five times away from a -3dB point is 0.17dB down from passband response which is better than the required ± 0.25dB specified.

$f_L = 100Hz/5 = 20Hz$

$f_H = 20kHz * 5 = 100kHz$

As stated in the **External Components** section, R_i in conjunction with C_i creates a

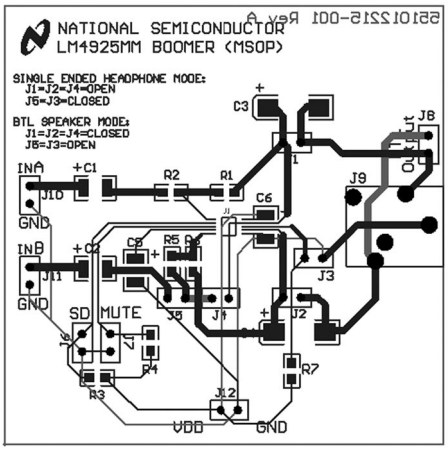
$C_i \geq 1 / (2\pi * 20k\Omega * 20Hz) = 0.397\mu F$; use 0.39µF.

The high frequency pole is determined by the product of the desired frequency pole, fH, and the differential gain, A_V. With an $AV_V = 1$ and $f_H = 100kHz$, the resulting GBWP = 100kHz which is much smaller than the LM4925GBWP of 3MHz. This example displays that if a designer has a need to design an amplifier with higher differential gain, the LM4925can still be used without running into bandwidth limitations.

Application Information (Continued)

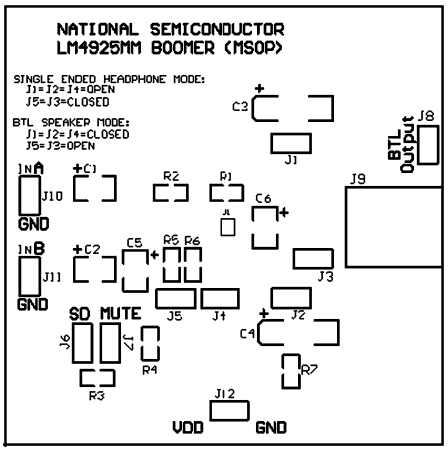
LM4925 BOARD ARTWORK

Composite View



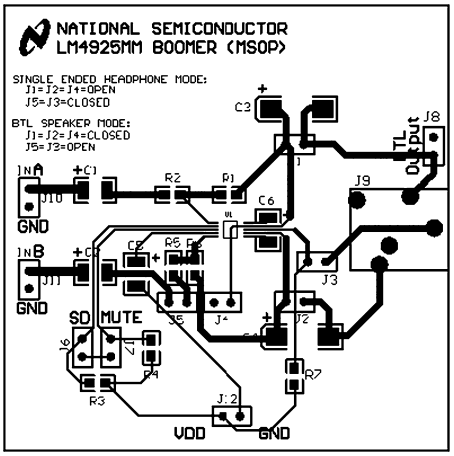
20121164

Silk Screen



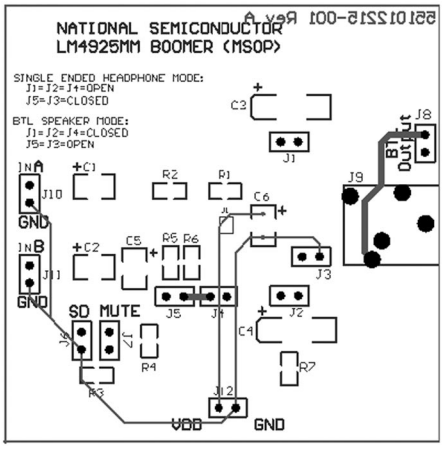
20121165

Top Layer



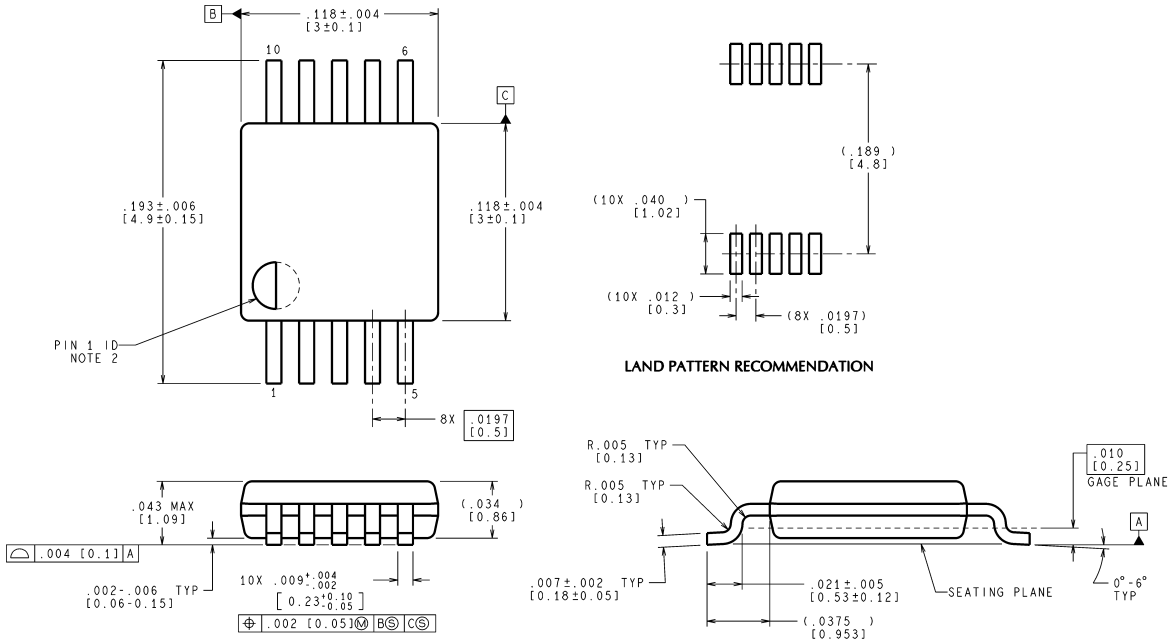
20121166

Bottom Layer



20121163

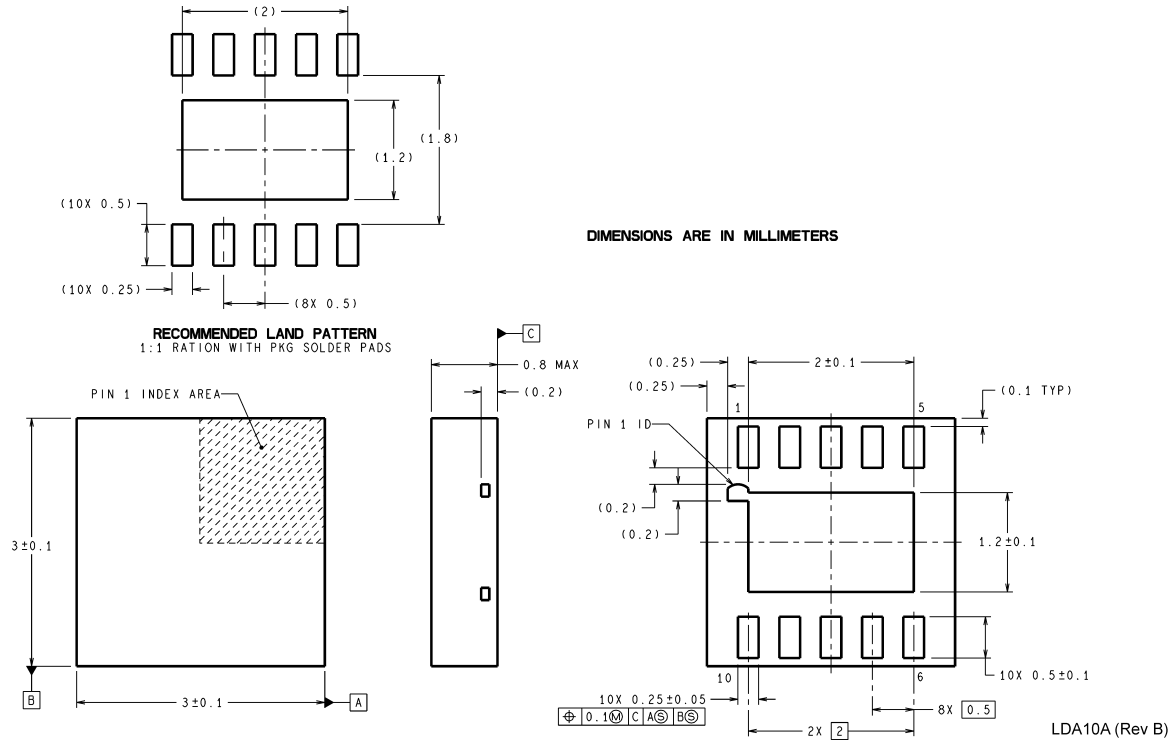
Physical Dimensions inches (millimeters) unless otherwise noted



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

MUB10A (Rev B)

MSOP Package
Order Number LM4925MM
NS Package Number MUB10A



DIMENSIONS ARE IN MILLIMETERS

LDA10A (Rev B)

LD Package
Order Number LM4925LD
NS Package Number LDA10A

Notes

National Semiconductor
Americas Customer
Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

www.national.com

National Semiconductor
Europe Customer Support Center
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer
Support Center
Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560