January 1999

National Semiconductor

LM3641
Lithium-Ion Battery Pack Protection Circuit

General Description

The LM3641 Lithium Protection Integrated Circuit resides inside a 3.6V Lithium-Ion battery pack consisting of a single cell or multiple parallel cells. The IC controls the ON/OFF state of a pair of low threshold N-channel power MOSFETs placed in series with the battery cell(s). The purpose of this MOSFET pair is to protect the cell(s) from inadvertent electrical over-stress. The IC compares the cell voltage against internally programmed minimum and maximum limits. Transient voltage faults of approximately 1.25 seconds are tolerated.

The IC also monitors the bi-directional current flow in the battery pack by measuring the voltage across a robust 4 mΩ current sensing resistor internal to the protection IC package. The IC turns OFF the MOSFET pair whenever any fault limit is exceeded. Momentary current surges <4 ms are tolerated.

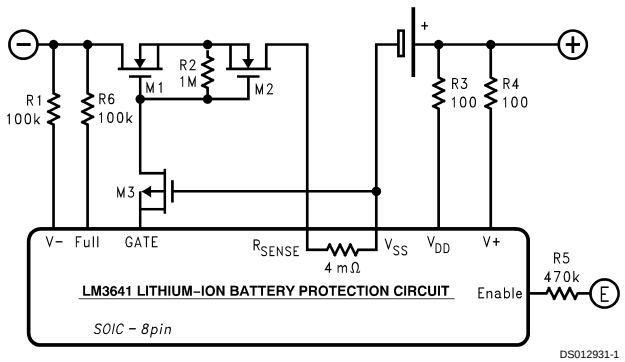
The Enable pin allows external ON/OFF control of the MOSFET pair and resets the IC after the MOSFET pair is turned OFF and the pack is safe to operate again.

The limits for overcharge and overdischarge voltage, as well as independent limits for each direction of overcurrent are factory adjusted employing EEPROM.

Features

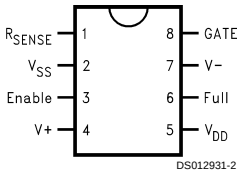
- Automatic battery disconnect when the cell is over-charged or over-discharged.
- Maximum cell voltage for MOSFET conduction is factory programmable between 4.0V and 4.4V with a ±25 mV tolerance (0˚C to +60˚C).
- Minimum cell voltage for MOSFET conduction = $0.57 \bullet V_{MAX}$ ±3.5% (0˚C to +60˚C).
- Internal 4 mΩ current sense resistor provides ±0.5A maximum accuracy for detection of overcurrent faults. The maximum charge and discharge current is factory programmable between 1A and 5A. A single overcurrent fault event opens and protects the MOSFET pair.
- Automatic detection of safe pack conditions for recovery (MOSFET pair ON) from a fault condition (over/under discharged or overcurrent).
- Average current drain = 1.2 µA typical.
- Optional Enable pack terminal can be used to prevent accidental short circuit of pack and for maximizing the shelf life of the pack (IC powers down when the pack is not in use).
- Over-current events cause connection of an internal 50 kΩ "FET-Bypass" resistance across OFF MOSFET pair. Loads >3–7 MΩ are required for return to conduction mode.
- Over-charged states cause connection of a 5 kΩ "Cell-Bypass" resistor to ensure that the cell is not allowed to be overcharged by leakage paths.

Typical Application



Connection Diagram and Ordering Information

Top View
8-Lead SOIC (M08A)



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Actual Size

DS012931-3

Order Number LM3641M
See NS Package Number M08A
This device is factory programmable. Contact your local NSC sales office for ordering information.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Maximum Input Supply Voltage (V_{DD})	−0.3V to 5.5V
V+ or GATE or Full Pin Voltage	−0.3V to V_{DD} + 0.3V
Enable or V− Pin Current	±200 µA
Power Dissipation (Note 2)	Internally limited
ESD Susceptibility Human Body Model (Note 3)	2 kV
Lead Temperature (Soldering, 10s)	260˚C

Operating Range (Note 1)

Ambient Temperature Range	0˚C to +60˚C
Junction Temperature Range	−40˚C to +125˚C

LM3641 Electrical Characteristics

Specifications with standard type face for T_J = 25˚C, and those with **bold type** apply over **full Operating Temperature Range**. Unless otherwise specified, V_{SS} = 0V, V_{DD} = 3.6V, V_{ENABLE} = V_{DD}.

Symbol	Parameter	Conditions	Typical (Note 4)	Limit (Note 5)	Units
V_{MAX}	Overcharge Protection Accuracy	0˚C to +60˚C	A.S.(Note 6)	±25	V mV(max)
V_{MAX-85}	Overcharge Protection Accuracy	Temp = 85˚C	$<V_{MAX}$ @ 25˚C		
$V_{MAX-RANGE}$	Overcharge Protection Program Range		4.2	4.0 4.4	V V(max) V(min)
V_{SAFE}	Max Cell Voltage Overshoot (referred to V_{MAX})		V_{MAX} + 100 mV		V
V_{MIN}	Overdischarge Protection Accuracy		0.57•V_{MAX}	**+0.04 • V_{MAX}** **−0.04 • V_{MAX}**	V V(max) V(min)
$V_{GATE-FETS-ON}$	Gate Pin High	1 MΩ Load	V_{DD} −50 mV		V
$I_{GATE-FETS-ON}$	Gate Pin FET Turn-on Impedence		2		kΩ
$I_{GATE-FETS-OFF}$	Gate Pin OFF Current	V_{Gate} = 0V	10		nA
$I_{MAX-CHG}$	Overcurrent Protection Accuracy — Charging		A.S.(Note 6)	+0.5 −0.5	A A(max) A(min)
$I_{MAX-DIS}$	Overcurrent Protection Accuracy — Disharging		A.S.(Note 6)	+0.5 −0.5	A A(max) A(min)
I_{SUPPLY}	Supply Current (V_{DD}, V+, control pins) (Note 7)	normal mode V_{DD} = 3.6V excludes I_{R2}	120 1	 4	µApeak µA rms µA rms(max)
$I_{ENABLE\ PIN}$	Enable Pin Current (sink)	V_{ENABLE} = V_{DD}	400		nA
I_{V+}	Cell Sense Pin Current (sink)	V_{DD} = 3.6V	40		nA rms
t_{SAMPLE}	Cell Voltage Sampling Period — Normal and Overdischarge Modes	V+ < V_{MAX}	1	**0.75** **1.5**	s s(min) s(max)
$t_{SAMPLE-OVERCHARGED}$	Cell Voltage Sampling Period — Overcharged	V+ > V_{MAX}	0.25	**0.19** **0.28**	s s(min) s(max)
N_{SAMPLE}	Number of consecutive samples for overcharge or overdischarge prior to disconnect		4		

LM3641
Electrical Characteristics (Continued)

Specifications with standard type face for T_J = 25˚C, and those with **bold type** apply over **full Operating Temperature Range**. Unless otherwise specified, V_{SS} = 0V, V_{DD} = 3.6V, V_{ENABLE} = V_{DD}.

Symbol	Parameter	Conditions	Typical (Note 4)	Limit (Note 5)	Units
$t_{OVERCHARGE}$	Overcharge Transient Rejection Time (Note 8)		1.6		s
				0.57	s(min)
				2.64	s(max)
$t_{OVERDISCHARGE}$	Overdischarge Transient Rejection Time (Note 8)		4		s
				3	s(min)
				6	s(max)
$t_{OVERCURRENT}$	Overcurrent Transient Rejection Time		6		ms
DC	Duty Cycle of Pulse Charging	$V_{MAX} < V_{CELL} < V_{SAFE}$	87.5		%
		$V_{CELL} > V_{SAFE}$	50		%
$t_{ENABLE-DELAY}$	Delay from Rising/Falling Enable pin to FETs ON/OFF (Note 9)	L → H	5		ms
		H → L	3		
$V_{RECOVERY}$	MOSFET Threshold Voltage		±36		mV
$V_{MIN-CHARGE}$	Minimum Cell Voltage that can be charged, $V_{GATE} \approx V_{DD}$ (Note 10)		0		V
$V_{FULL-HIGH}$	Maximum High Output Voltage of Full Pin	$V+ > V_{MAX}$ $I_{FULL} < 4$ µA	V_{DD} − 1.2V		
$I_{FULL-OFF}$	Source/Sink Current of Full Pin in TRI-STATE®	$V+ < V_{MAX}$ V_{FULL} = 0V	10		nA
$I_{R-SENSE}$	Maximum R_{SENSE} Current	Duration < 6 ms	60		A
R_{SENSE}	R_{SENSE} Range		4		mΩ

Note 1: Absolute Maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum allowable power dissipation is calculated by using $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$, where T_{JMAX} = 150˚C, T_A is the ambient temperature, and θ_{JA} = 160˚C/W.

Note 3: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

Note 4: Typical numbers are at 25˚C and represent the most likely parametric norm.

Note 5: Limits are 100% production tested at 25˚C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's Averaging Outgoing Quality Level (AOQL).

Note 6: Application Specific. This analog parameter's value is programmed during National's production testing of the device. Please contact your local NSC sales office to specify the V_{MAX}, $I_{MAX-CHG}$ and $I_{MAX-DIS}$ values when ordering this device. V_{MAX} can be programmed between 4.0V and 4.4V. $I_{MAX-CHG}$ can be programmed between 1A and 5A. $I_{MAX-DIS}$ can be programmed between 1A and 5A.

Note 7: I_{SUPPLY} includes V_{DD} pin peak currents that occur at each t_{sample} period. The I_{DD} peak current duration is approximately 2.2 ms and the I_{VDD} peak current is approximately 120 µA.

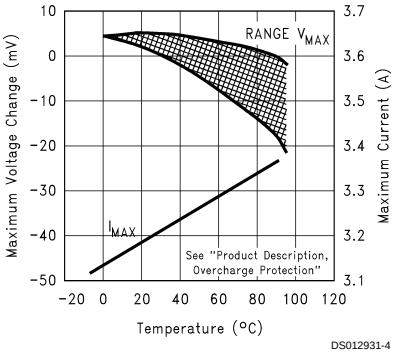
Note 8: Computed from 4 sample periods of the worst case values of t_{SAMPLE} and $t_{SAMPLE-OVERCHARGED}$.

Note 9: High pulses < 3 ms (typ) will be typically ignored and low pulses < 5 ms (typ) will be typically ignored.

Note 10: $V_{MIN-CHARGE}$ will be limited by the threshold of M3.

Typical Performance Characteristics

Maximum Current and Normalized Maximum Voltage vs. Temperature



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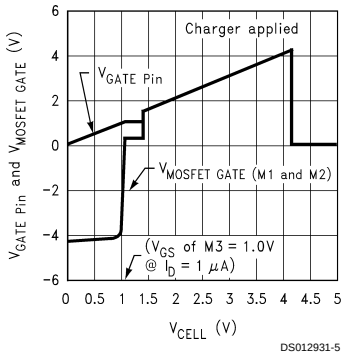
GATE Pin and MOSFET GATE Voltage vs CELL Voltage



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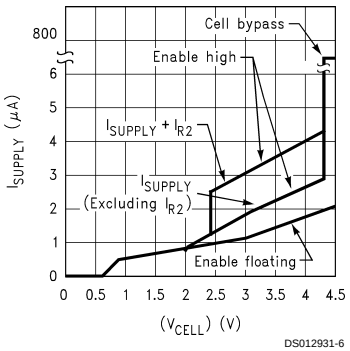
Supply Current



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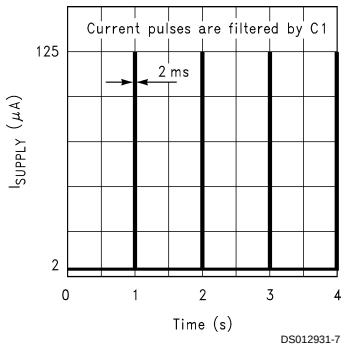
Supply Current vs Time



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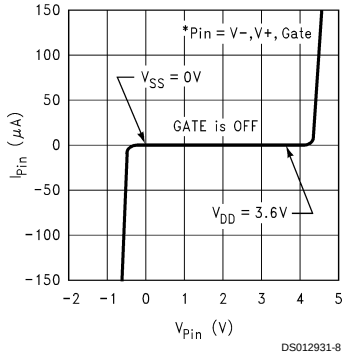
Pin* Current vs Pin* Voltage



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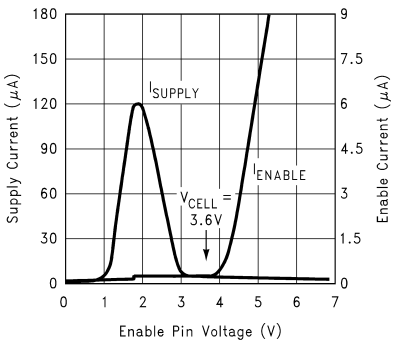
Supply and Enable Current vs Enable Voltage



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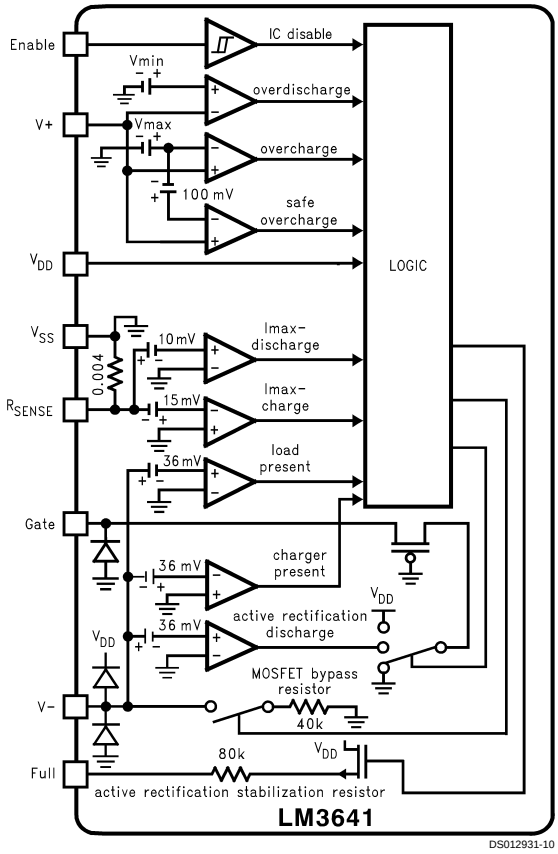
Block Diagram



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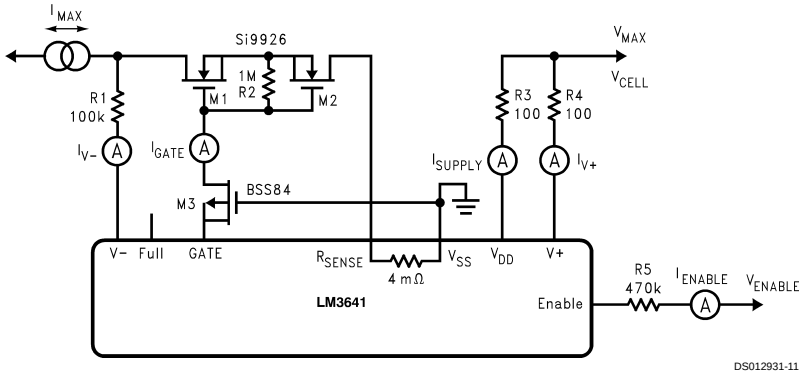
Test Circuit



DS012931-11

Product Description

Normal charging of Li-Ion packs requires Constant Voltage Constant Current (CVCC) chargers that terminate charging at a voltage value just below the maximum protection voltage (V_{MAX}). Only in the event of an invalid charger or an out of compliance charger operation should the protection IC terminate charging.

OVERCHARGE PROTECTION

The IC protects the cell(s) against overcharge. Normally, the cell voltage is sampled once a second. Four consecutive samples of $V_{CELL} > V_{MAX}$ result in the MOSFET pair turning OFF. The transient response for overvoltage requires one sample at the t_{SAMPLE} period (1s typical) and three $t_{SAMPLE-OVERVOLTAGE}$ periods (0.25s typical). The first overcharge event is asynchronous to the 1 second sampling so the delay between the actual instance of overcharge and the first sample can result anywhere in the range of zero to t_{SAMPLE}. The requirement for 4 consecutive samples of $V_{CELL} > V_{MAX}$ filters noise from the cell due to transient currents. Should the cell voltage exceed V_{MAX} by more than 100 mV (V_{SAFE}), the MOSFETs will turn off on the first sample reading. This provides an extra measure of safety. The return to conduction mode requires that a load be applied to the pack or $V_{CELL} < V_{MAX} - 20$ mV. Also a L→H signal on the Enable pin will reset the GATE high, but if $V_{CELL} > V_{MAX}$, the GATE will go low again after 1.75 seconds. Whenever an overcharge disconnect has occurred, a cell bypass resistor (≈5 kΩ) is switched across the V_{DD} and V_{SS} pins and the Full pin pulls to near V_{DD}. The cell bypass resistor ensures that the cell is discharged even though some component of R1's current will still flow in the cell, if a charger is applied. The cell bypass resistor is removed when $V_{CELL} < V_{MAX}$ again.

ACTIVE RECTIFICATION

Overcharged cells can be discharged by the application of a load to the pack. Active Rectification is the biasing of the power MOSFETs GATE so that the $V_{DS} = V_{RECOVERY}$ for discharge currents. The MOSFETs turn OFF for charge currents. The Active Rectification amplifier assures uninterrupted conduction for discharge currents only. The Full pin's output impedance is ≈80 kΩ when active high ($V_{CELL} > V_{MAX}$) and TRI-STATE when inactive ($V_{CELL} < V_{MAX}$). The Full pin can optionally supply a small FET current necessary to stabilize the Active Rectification loop by maintaining at least $(V_{DD}-1V)/R6+80k)\bullet I_D$ in the MOSFET. The Full pin's overcharge signal could be used in applications where the charger is logically disabled by the protection circuit, a change time-out circuit is initiated or whenever an overcharge signal is otherwise desired. The Full signal will go low (TRI-STATE with an external resistor pulldown) and cell bypass turns off if a cell decays to $V_{CELL} < V_{MAX}$.

OVERDISCHARGE PROTECTION

The cell(s) are also protected against overdischarge. Four consecutive 1 Hz samples of $V_{CELL} < V_{MIN}$ result in the MOSFET pair turning OFF. Cells that have discharged below V_{MIN} due to long periods of self-discharge can still be charged. Return to conduction mode for overdischarged packs automatically occurs if a charger is applied to the pack. Also a L→H signal on the Enable pin will reset the GATE high, however if $V_{CELL} < V_{MIN}$, the GATE will turn OFF again in 4 seconds.

OVERCURRENT PROTECTION

The battery current is monitored continuously by measuring the voltage across the internal sense resistor. If the terminal current exceeds $I_{MAX-CHG}$ (programmable) in the charge mode for longer than $t_{OVERCURRENT}$, the MOSFET pair disconnects. Similarly, if the terminal current exceeds $I_{MAX-DIS}$ (programmable) in the discharge mode for longer than $t_{OVERCURRENT}$, the MOSFET pair disconnects. Recovery to conduction mode requires either 1) a momentary detachment of the pack so the Enable pin can be cycled low, then high or 2) a direct low to high signal to the Enable pin controlled from logic.

ENABLE PIN

The pack can be protected from accidental short circuits should the Enable pin be made available as a third battery pack terminal. This third pack terminal is tied to the pack's positive terminal through a connection on either a valid charger or load. Shorting the high impedance Enable pin to the pack's positive terminal enables all functions of the protection circuit. The Enable pin disables the MOSFET pair whenever this pin is floating, such as when the battery pack is detached from a valid load or charger. Floating the Enable pin also forces the protection circuit into FET's OFF mode to maximize the shelf life of the battery pack. When the Enable pin is used to recover from overcharge, overdischarge or overcurrent events, the voltage measurement system memory is cleared of previous results. If the MOSFET bypass resistor is active, and the Enable goes low, the bypass resistor turns OFF. A series resistor of 470 kΩ to 1 MΩ between the Enablel terminal of the pack and the Enable pin of the IC, protects the IC from ESD events at the pack's terminals.

SLEEPMODE

Sleepmode is a reduced current state that occurs when the Enable pin is floating or low. The FETs are turned OFF. Sleepmode minimizes the artificial self-discharge of the pack when the pack is not in use.

INVALID CHARGER

Assume a charger that exceeds the V_{MAX} rating of the IC is applied to the pack. The power MOSFETs will eventually turn OFF due to overcharge if $I_{CHARGER} < I_{MAX-CHG}$, or turn OFF due to overcurrent if the invalid charger's current exceeds $I_{MAX-CHG}$. If the charger was applied to the pack with the polarity reversed, then the MOSFETs would eventually turn OFF due to either overdischarge or overcurrent depending on the magnitude of the charger's available current. In either case, the voltage on the V− pin will be driven by the open circuit voltage of the charger. The V− pin is clamped by internal diodes to V_{DD} and V_{SS} and the pin's current limited by R1 (see the typical curve "Pin Current vs. Pin Voltage") with R1 = 100k, the pin current will not exceed the maximum recommended value of ±200 µA for a ±20V invalid charger. Higher invalid charger voltages can be tolerated when using higher values for R1. Proper LCCE operation is not limited, even by values for R1 in excess of 1 MΩ.

Product Description (Continued)

NORMAL TERMINATION OF CHARGING

As you can see in *Figure 1*, the cell voltage must exceed V_{MAX} for 4 consecutive samples before the MOSFET pair is turned OFF (1). Once V_{MAX} is exceeded, the sampling rate increases to 4 Hz. The sampling rate will return to 1 Hz only after 4 consecutive samples result in $V_{CELL} < V_{MAX}$. After the MOSFET pair is OFF (2), the voltage across the cell(s) relax and the cell voltage will drop below V_{MAX}. On the next sample, (3), the MOSFET pair will turn ON. As long as the charger is applied and the MOSFET pair turn ON, the cell voltage will exceed V_{MAX} again. The cycle of 4 samples ON a 1 samples OFF will continue until the cell voltage equals V_{MAX} after the MOSFET pair is OFF, (4). This example exaggerates the rate of these events. The actual operation would result in many ON/OFF cycles at a decreasing duty cycle prior to complete termination of charge. The cell bypass resistor will discharge the cell enough to turn on the GATE over a period of minutes.

NORMAL TERMINATION OF DISCHARGING

The cell voltage must go below V_{MIN} for 4 consecutive samples before the MOSFET pair is turned OFF (1), which is shown in *Figure 2*. Once the MOSFET pair is OFF and the current is interrupted, the voltage across the cell(s) will increase and the cell voltage could exceed V_{MIN} (2). The MOSFET pair remain off until a charger is applied to the pack (3). The presence of a charger turns the MOSFET pair ON. Deeply discharged cells will be charged, although for some narrow bands of V_{CELL}, the GATE may occasionally pulse OFF momentarily.

TERMINATION OF ILLEGALLY HIGH CHARGING

Should a high charge current be applied to the pack near the end of charge, the cell voltage could exceed V_{SAFE}, which is approximately 100 mV greater than V_{MAX} (1), see *Figure 3*. On the first detection of a cell voltage in excess of $V_{SAFE-OVERCHARGE}$, the MOSFET pair will be turned OFF (2). The sample rate increases to 4 Hz after the first detection of $V_{CELL} > V_{MAX}$. It is desirable under these circumstances for the MOSFET pair to turn ON for only the shortest allowed time period, which is 0.25 seconds. Each sample exceeding V_{SAFE} causes the MOSFET pair to turn OFF (3). Should the cell voltage not drop below V_{MAX} after the MOSFET pair turn OFF, the MOSFET pair remain OFF (4). This example exaggerates the rate of these events. The actual operation would result in many ON/OFF cycles at a decreasing duty cycle prior to complete termination of charge.

LOAD APPLIED IN OVERCHARGED STATE

If a load is momentarily applied while the cell is in overcharged state, then the MOSFET pair is momentarily turned ON, see *Figure 4*. The MOSFET pair will stay ON only as long as the load is applied. The MOSFET pair will stay ON after the load is removed only if the cell voltage remains below V_{MAX} for 4 consecutive samples. Possible events are shown as examples of operation:

(1) A momentary load is applied to an overcharged cell, the MOSFET pair stay ON only as long as the load is applied. The gate drive is limited so that the MOSFET pair ON voltage will match a bias voltage generated internal to the IC, $V_{RECOVERY}$. This bias voltage is the minimum MOSFET ON voltage that allows for the detection of a load. This mode of operation is *Active Rectification*. Note that the MOSFET pair do not turn ON for the momentary application of a charger.

(2) A load is applied for less than 4 samples. The MOSFET pair is ON for the load period, but turn OFF after the load is removed. Only after the 4th sample of $V_{CELL} < V_{MAX}$ will the MOSFET pair turn ON, this time will full drive potential.

(3) Assume the application of a charger. Conduction is allowed because the FETs are ON, but the MOSFET pair will stay ON only for 4 consecutive overcharge samples. See the diagram for the “Normal Termination of Charging”.

(4) The MOSFET pair will turn OFF after the 4 consecutive overcharge samples.

(5) A load is applied and after $V_{CELL} < V_{MAX}$ for 4 consecutive samples, the MOSFET pair turn ON full. As long as V_{CELL} stays below V_{MAX}, the MOSFET pair will stay ON.

Should a load be applied that exceeds the overcurrent-discharge current limit while the IC is in active rectification mode, the MOSFET pair will turn OFF. Recovery requires that either the IC detects a load greater than 3–7 MΩ or that the cell voltage remains under V_{MAX} for 4 samples. If the load that caused overcurrent remains after the cell voltage drops under V_{MAX} for 4 samples, then the MOSFET pair will turn ON once more and normal overcurrent mode is entered.

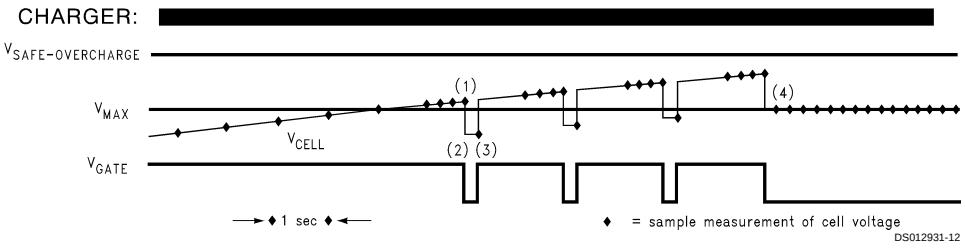


FIGURE 1. Normal Termination of Charging

Product Description (Continued)

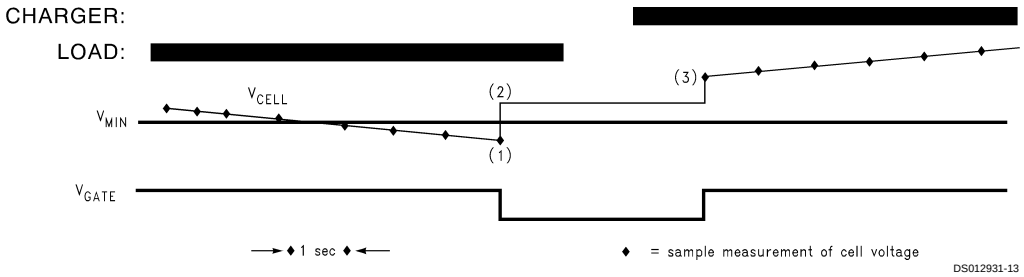


FIGURE 2. Normal Termination of Discharging

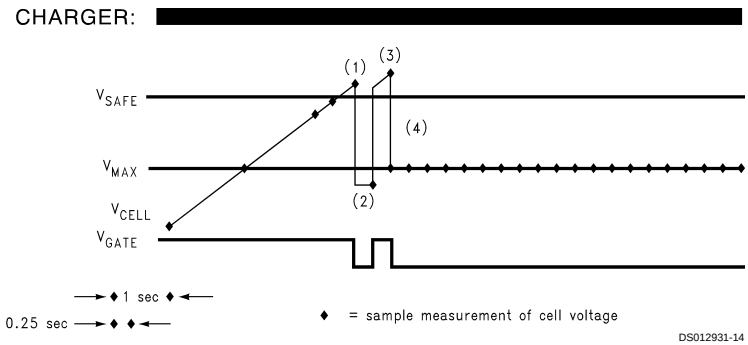


FIGURE 3. Termination of Illegally High Charging

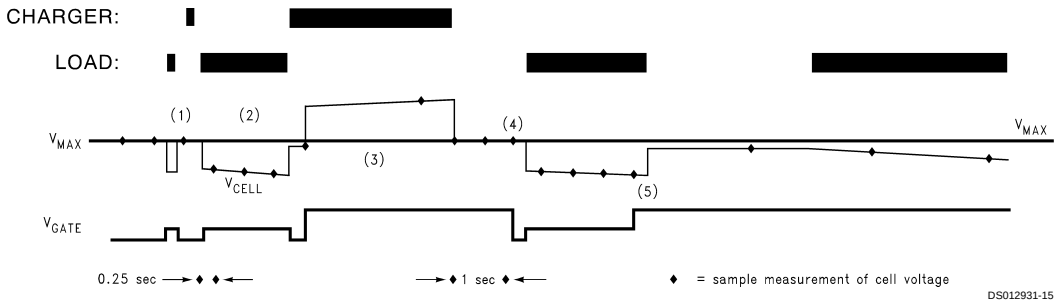


FIGURE 4. Load Applied in Overcharged State

Fail Safe Features

The safety provided by the LM3641 goes beyond the normal operation of the IC. The design of the IC includes many aspects that continue to assure protection of the cells even when malfunctions occur.

- A rugged internal sense resistor offers precise overcurrent response (magnitude and time) which allows smaller volume power MOSFETs to be used. If the internal resistor's sense circuitry's input open circuit (very unlikely), the MOSFET pair will turn OFF. The IC will fail safe.
- If any pin becomes detached from the PCB, either the MOSFETs will turn OFF or the part will continue to protect the Cell.
- The maximum cell voltage limit is trimmed by EEPROM and offers optimal accuracy. Each EEPROM cell has redundant EEPROM transistors for additional reliability. The EEPROM register also contains a parity check bit. In the rare event that an EEPROM bit would change state, the power MOSFETs will be turned OFF rather than allow the IC to operate out of specification.
- The external MOSFETs are specified to provide adequate illegal charger withstand capability. Because of M3, the IC is designed to never be exposed to more than the actual cell voltage. Therefore the IC's maximum rated supply voltage does not limit the magnitude of illegal charger voltages that can be protected by the IC. M3's Vt also guarantees that shorted cells can not be charged.

Fail Safe Features (Continued)

- In the event of an extremely high charge current, the cell voltage could exceed the maximum supply rating of the IC. The IC is protected by internal voltage clamps and the external 100Ω resistors R3 and R4.
- The external MOSFET pair turn-off resistor R2 aids in fail safe operation in the rare event that the IC fails. Dual independently controlled series switches internal to the IC must both turn on to allow the MOSFET pair to conduct. If either control signal is in error, the external resistor R2 will ensure that the MOSFET pair turn OFF.
- The LM3641 is 100% tested for all aspects of operation. The digital design-for-test methodology allows the circuitry to be tested at a greatly accelerated rate while maintaining near perfect fault coverage.
- The cell bypass resistor prevents leakage current from continuing to charge overcharged cells.

PCB Safety Considerations

- The power MOSFET turn-OFF resistor R2 is critical for proper turn-OFF of the MOSFETs during a fault condition. Precaution is necessary so that this resistor or its contacts to the FET terminals is not interrupted by defects during and after the PCB assembly. The most robust design is to replicate this resistor and its connections (see *Figure 6*).
- The IC bypass capacitor, C1, maintains stable operation of the IC's analog functions. This component's presence can be assured with a redundant capacitor (see *Figure 6*).

Pin Description

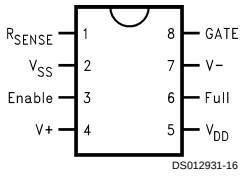


FIGURE 5. Connection Diagram

R_{sense}	Terminal of the internal current sensing resistor.
V_{SS}	Negative IC supply and sense pin for the cell's negative terminal.
Enable	Enable/Disable for MOSFET drive and power-down mode. Also used to recover from fault conditions.
V+	Sense pin for the cell's positive terminal.
V_{DD}	Positive IC supply.
Full	High impedance pull-up signal indicating that the overcharge transition has occurred.
V−	Pin used to monitor the negative terminal potential of the battery pack.
GATE	Gate drive for the external MOSFET pair. This pin is switched to V_{DD} in the ON condition and is high impedance for the OFF condition.

Glossary of Terms

Conduction	Battery pack mode of operation when the MOSFET pair is ON.
Disconnect	Battery pack mode of operation where the MOSFET pair is OFF.
Charging	State of current conduction *into* positive terminal of battery pack from a current limited voltage source that does not exceed the maximum voltage rating of the MOSFET pair.
Discharging	State of current conduction *out of* the positive terminal of battery pack into a load.
IC Enabled	The state when the Enable pin potential is set to the V+ potential. The IC operates with full functionality.
IC Disabled	The IC state when the Enable pin is floating or pulled low, such as in a detached pack. The Enable pin will be pulled to V_{SS} with an internal current source, $I_{ENABLE\ PIN}$. The IC will go into power-down and the MOSFET pair is turned OFF to protect the pack from accidental short circuits, invalid chargers or invalid loads.
Recovery	The ability to safely return to conduction mode after a fault condition has caused the MOSFET pair to turn OFF. Recovery is accomplished with a low to high signal on the Enable pin for overcharge, overdischarge and overcurrent. Recovery from overdischarge is automatic with the application of a charger. Recovery from overcharge is automatic with the application of a load. Recovery from overcurrent is automatic when the impedance at the terminal pack exceeds 4–7 MΩ.
$t_{FET-TURN-OFF}$	The turn-off time of the MOSFET pair. This parameter is dependent on the external components used, however the typical time is 1–4 ms.
Power-down	A reduced power state resulting from a floating Enable. The MOSFET pair is always OFF.
Cell-Bypass resistor	A resistor that is connected across the cell(s) whenever overcharge conditions are detected. If the MOSFET pair is OFF and a charger applied, then some of the current in the V− pin would flow through the cell. This resistor ensures that the cell is discharged and not charged during such an event. This resistor also compensates for the possibility of leaking OFF MOSFET pair overcharging the cell(s).
MOSFET Bypass resistor	A resistor that is connected across the MOSFETs after overcurrent fault. When the pack impedance 3–7 MΩ, the MOSFET bypass resistor reduces the MOSFET voltage to less than $V_{RECOVERY}$ and the MOSFET turns ON. If the MOSFET bypass resistor is active, and the Enable goes low, the bypass resistor turns OFF.
LCCE	Return to conduction mode for overdischarged packs does not require a low to high edge on the Enable pin. The application of a charger will turn on the FETs.

Glossary of Terms (Continued)

This is also defined as the *Low Cell Charge Enable (LCCE)*. This way, deeply discharged packs can be charged even if the cell voltage is too low to enable the logic to operate. See also, the M3 section in the "Component Selection".

Glossary of Specification Parameters

V_{MAX} The maximum steady state cell voltage for disconnect mode.

$V_{SAFE-OVER-CHARGE}$ The maximum cell voltage overshoot for conduction mode, referred to V_{MAX}.

V_{MIN} The minimum steady state cell voltage for conduction mode.

$V_{MIN-CELL-CHARGE}$ The minimum cell voltage for which conduction mode for charging is guaranteed. Cell voltages below this value will not be charged, that is the MOSFET pair will remain OFF. This feature ensures that very deeply discharged cells will be chargeable.

$V_{GATE-FETS-ON}$ The maximum pull-up voltage of the GATE pin in conduction mode.

$I_{GATE-FETS-ON}$ The pull-up current available from the GATE pin in transition to the conduction mode. This current collapses to zero at GATE = V_{DD}.

$I_{GATE-FETS-OFF}$ The leakage current of the GATE pin in disconnect mode.

$V_{RECOVERY}$ The voltage across the MOSFET pair that is used to detect if a charger or a load is connected to the battery pack. This voltage is the difference between the V− and V_{SS} pins. The voltage between these pins is forced to equal $V_{RECOVERY}$ after a load has been applied to an overcharged pack in order to discharge the pack without the MOSFET cycling ON/OFF.

$I_{MAX-CHG}$ The maximum magnitude terminal current allowed during charge mode.

$I_{MAX-DIS}$ The maximum magnitude terminal current allowed during discharge mode.

I_{SUPPLY} The IC supply excluding the current needed to supply the MOSFET turn-on current. The MOSFET turn-on current is calculated by $V_{CELL}/R2 \cong 4\ \mu A$. The IC supply current flows between the V_{DD} and V_{SS} pins. Additional current can flow from the V_{DD} and V_{SS} pins to the V− pin when the MOSFET pair is OFF and a charger is applied to the pack. This current is limited by the V− pin's external resistor, R1.

$I_{ENABLE\ PIN}$ The internal pulldown current for the Enable pin; terminated at V_{SS}.

t_{SAMPLE} The time period between cell voltage measurements.

$t_{SAMPLE-4X}$ The time period between cell voltage measurements after 1 overcharge measurement and before 4 normal cell voltage measurements.

$t_{OVERCURRENT}$ The time period for which the battery current must be greater than the maximum current limit prior to turning the MOSFET pair OFF.

$t_{FET-TURN-ON}$ Turn-on time (MOSFET pair $V_{GS} > V_t$) with 1 MΩ and 2 nF load at the GATE pin.

$t_{ENABLE-RECOVERY}$ The delay time after the Enable pin is reconnected to V+ before the MOSFET pair is allowed to turn-on. This prevents switching "chatter" of the MOSFET pair during insertion to a charger or load.

Component Selection

M1 & M2

The **power N-MOSFETs** must be able to isolate the cell from invalid charge voltages, when the MOSFETs are OFF. The breakdown voltage from drain to source determines the maximum charger or reversed charger voltage tolerated. Invalid chargers that exceed this breakdown voltage will allow unlimited charge currents and therefore it is recommended to provide secondary protection with passive thermal and/or current fuses.

The maximum gate to source DC voltage is the cell voltage. The V_{GS} may peak momentarily during the MOSFETs turn ON from an OFF condition with a charger applied. This causes the charger voltage to appear across the gate to source voltage. So, choose MOSFETs than can withstand this voltage.

The LM3641 has limited gate pin drive current and therefore, the maximum V_{GS} rating of the MOSFETs must be higher than the illegal charger voltage. The selection of the MOSFETs' ON impedance is a pack power efficiency consideration.

The MOSFETs maximum DC current operation should exceed the maximum rating of the LM3641's overcurrent protection. Junction thermal conditions of the MOSFETs are of prime importance in designing a reliable system. For example, a dual MOSFET can have an I_{MAX} rating of 5A. This rating however is valid when either one of the MOSFETs is ON. If both MOSFETs are ON, the rating for I_{MAX} is less than 2.5A, because you have twice the R_{DSON}, so twice the power dissipation. Two single MOSFETs might give you a better solution.

The peak currents encountered during short circuit are of prime consideration in specifying the MOSFETs. The peak current of parallel connected cells will be greater. Different cell chemistries give different peak currents. The ON resis-

Component Selection (Continued)

tance of the MOSFETs ultimately determines the peak current in short circuit and therefore is a useful parameter for determining if the MOSFETs are compatible for the application. The proper pack design dictates that the MOSFETs are capable of withstanding repeated short circuit events over the life of the pack without developing opens or shorts between the drain and source.

M3

This P-MOSFET is necessary for isolating the IC from invalid chargers. Its drain to source voltage breakdown should exceed that of M1 and M2. The on conductance and g_m can be very poor and serve the purpose of driving the power MOSFETs M1 and M2 as the steady state drive is only $V_{CELL}/R2$. The operating $V_{GSmax} \leq V_{CELL}$. The V_t of M3 has significance in that it determines what minimum value of cell voltage is allowed for charging. When the cell voltage is lower than the V_{GSM3} required to conduct $V_{CELL}/R2$, M1 and M2 can not be turned ON and the pack is unchargeable. This is useful for preventing the charging of shorted cells, while reviving packs that have become deeply discharged during extended storage.

R's and C's

For the **resistors and capacitors** used in the application circuit, *Table 1* will give the acceptable value range and the effected parameters. The function of each of these components is described in the "Application Circuit" section.

TABLE 1. Component Acceptable Value Range and Effected Parameters

Component	Acceptable Value Range	Parameters Effected
R1	100 kΩ–1 MΩ	Tolerated magnitude of invalid charger
R2	1 MΩ	I_{SUPPLY} vs. MOSFET turnoff delay
R3, R4	50Ω–500Ω	Current limit in extreme over voltage condition vs. IR drop of I_{SUPPLY}
R5	100 kΩ–1 MΩ	Current limit in pack ESD event vs. IR drop of I_{ENABLE}
R6	100 kΩ–1 MΩ	I_{OL} vs. V_{OH} of Full signal
C1	0.01 µF–0.1 µF	Depends on frequency of noise loading the pack
C2	0.01 µF–0.1 µF	Depends on impedance spectrum of Cells
C3	0.01 µF–0.1 µF	Depends on MOSFET/Cell behavior during pack short circuit
C4	220 pF–1 nF	Equally effective during pack short circuit

Application Circuit

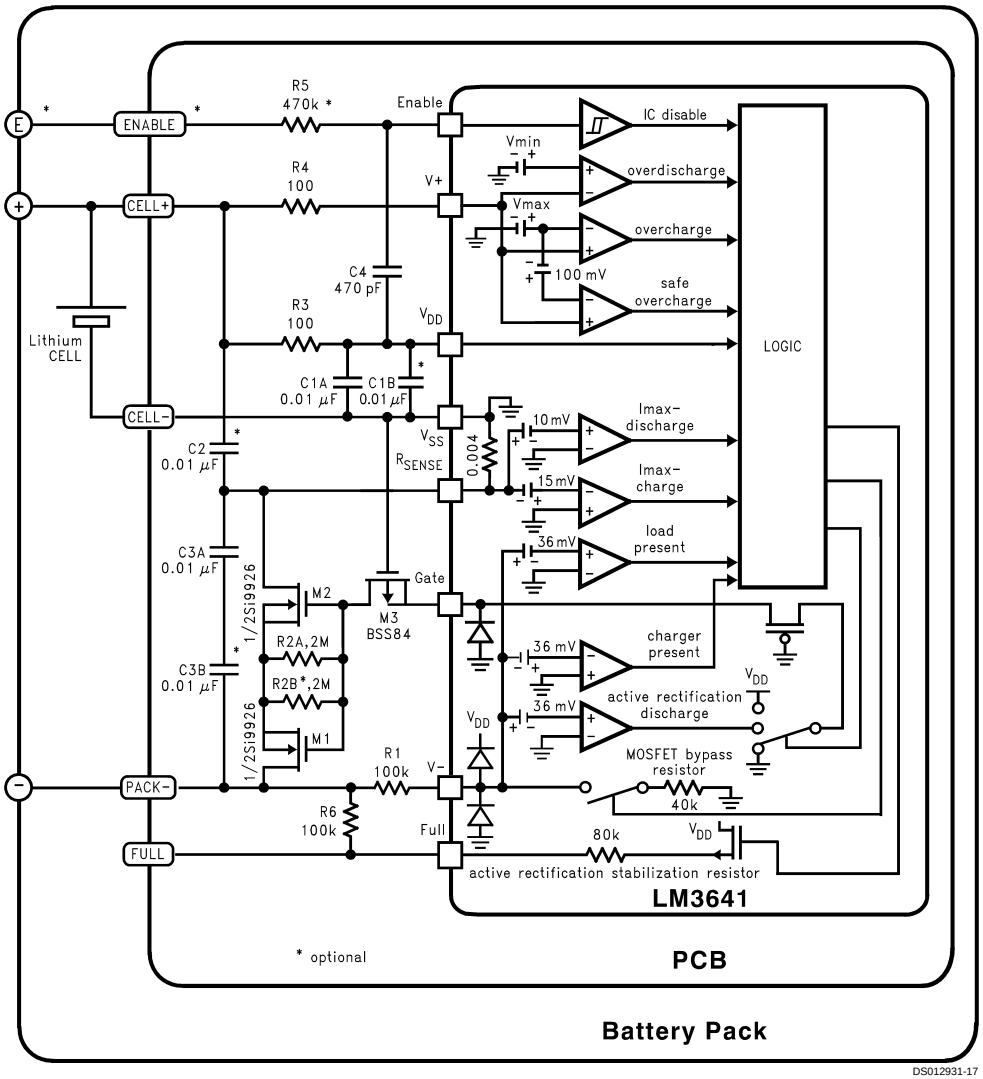


FIGURE 6. Application Circuit

The pack current flows through the series path of the cell, the sense resistor and the power MOSFETs, M1 and M2. M3 isolates the IC against high compliance voltage chargers when the power MOSFETs are OFF. The V− pin detects the polarity of voltage across the power MOSFETs. R1 limits the current into the V− pin when a charger is applied and the MOSFETs are OFF. R3 and R4 limit the current into the IC in the event of extreme charge current. They also prevent the cell to be shorted when the V_{DD} or V+ pin becomes shorted, either internally or externally. R5 provides ESD protection of the IC from the pack terminal “E”. C1 bypasses transient Cell currents so that the IC supply current is not interrupted. The bypass of V_{DD} is critical for stable operation, therefore it is advised that 2 parallel bypass capacitors C1A and C1B be used for redundancy. C2 is necessary to prevent the power MOSFETs from oscillating when the pack is short circuited. C3 suppresses possible oscillation of the MOSFETs during pack short circuit. C3 can be duplicated for extra safety. The same can be said for R2, which is used for proper turn OFF of the MOSFETs during a fault condition. C4 isolates the Enable pin from false reset signals during a pack short circuit event. Series C2 and C3 also provide high frequency bypass of the Cells which exhibit large impedance increase beyond 10–100 kHz. R6 has to be added to pull up the Full pin. The Enable section is optional. R5 and C4 are only needed if the 3rd terminal of the pack is used for the Enable function (see Product Description, “Enable Pin” section). If not used, short the Enable pin to the V_{DD} pin.

State Diagram

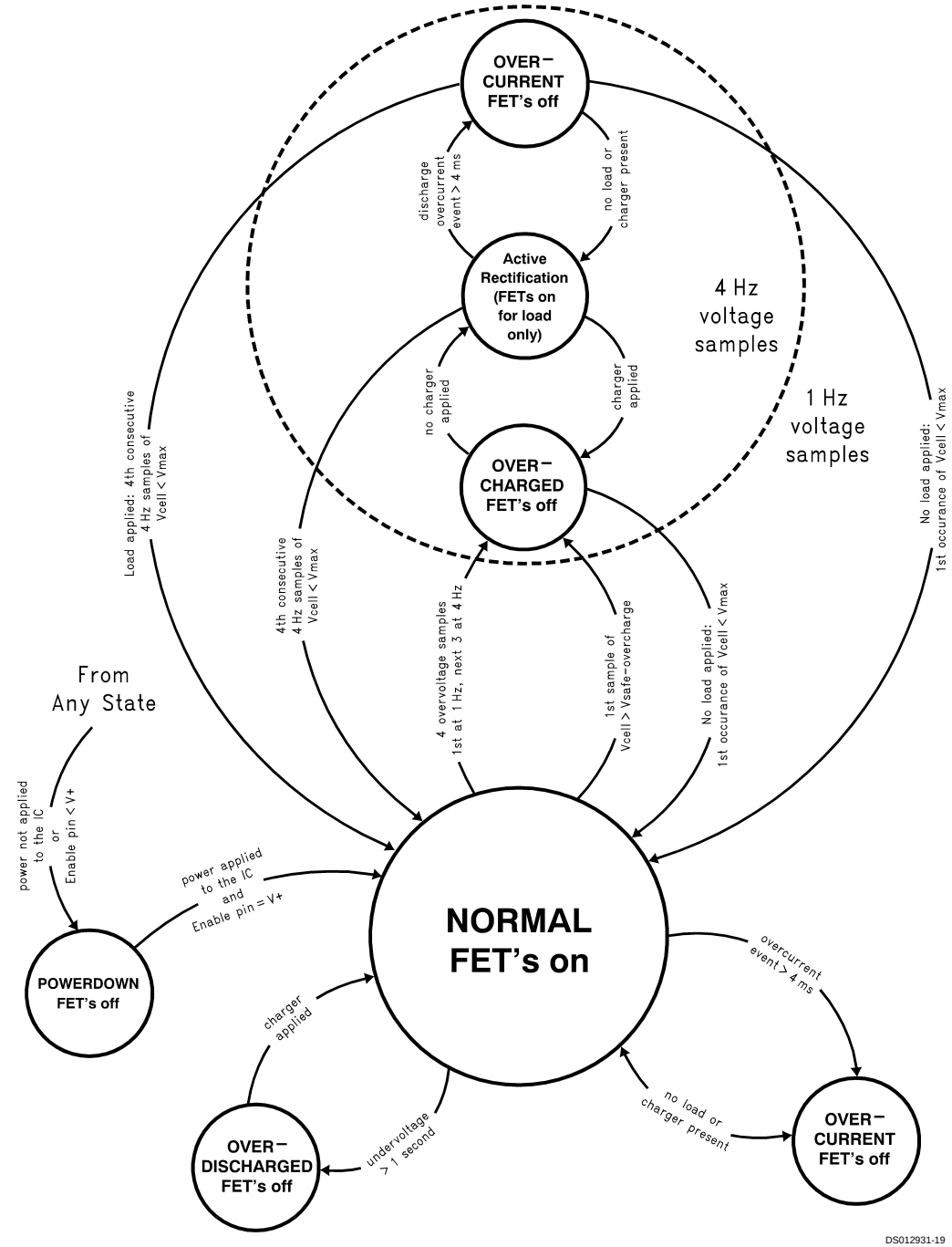
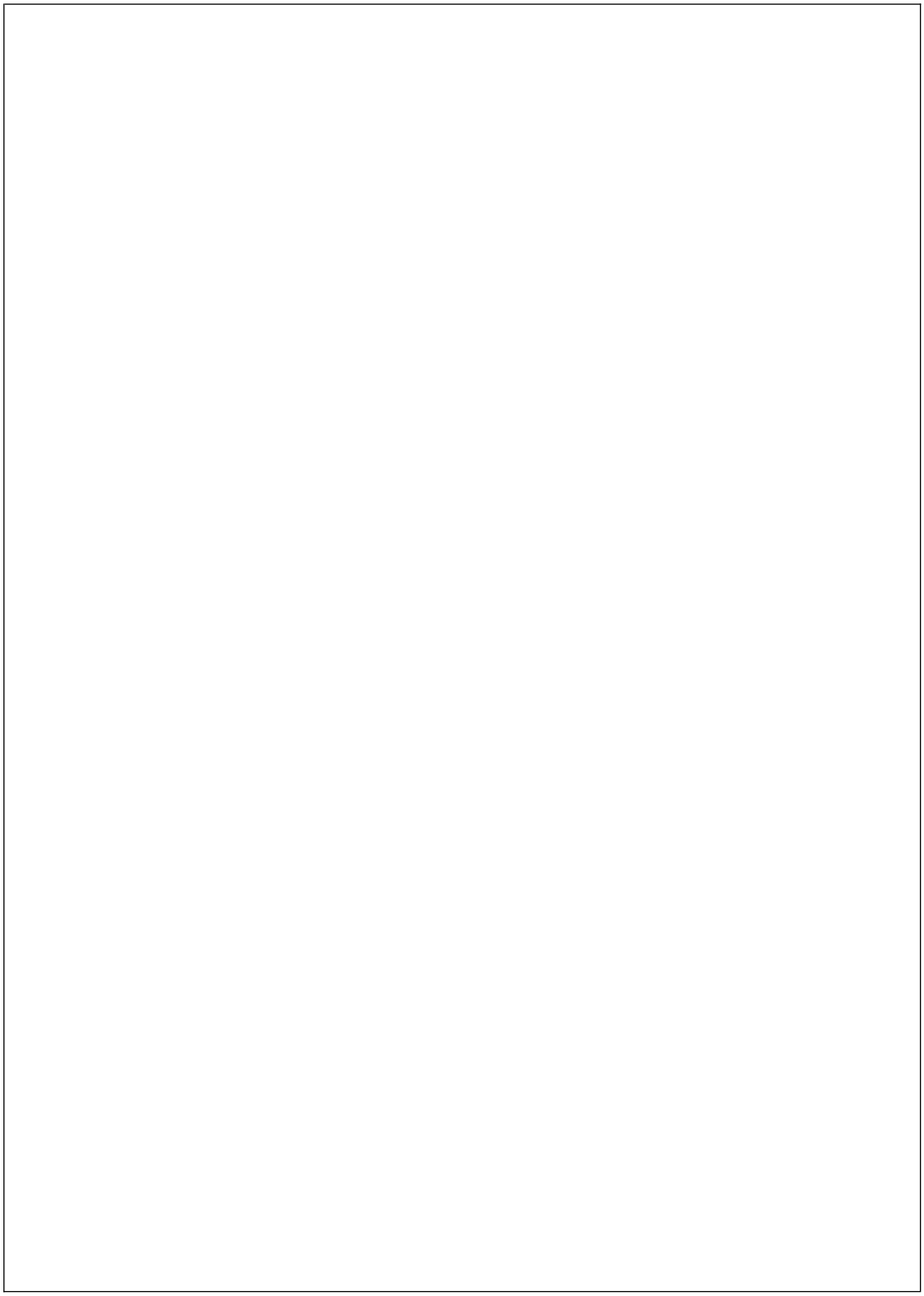
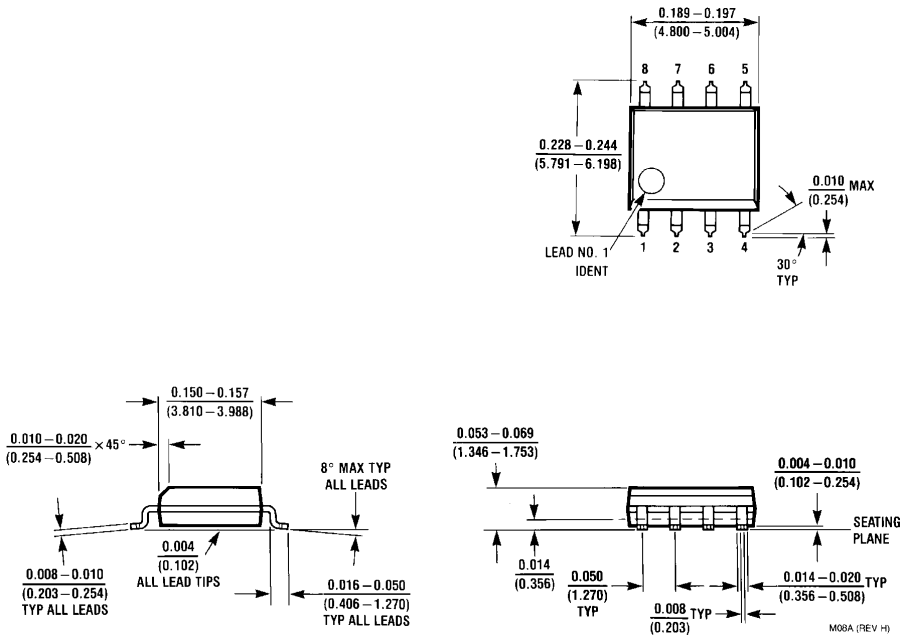


FIGURE 7. State Diagram for LM3641 Operation



Physical Dimensions inches (millimeters) unless otherwise noted



8-Lead SOIC (M08A)
Order Number LM3641M
NS Package Number M08A
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