National Semiconductor

March 2005

LM2903EP
Low Power Low Offset Voltage Dual Comparators

General Description

The LM2903EP consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. This comparator also has a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM2903EP was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM2903EP will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

ENHANCED PLASTIC

- Extended Temperature Performance of −40˚C to +85˚C
- Baseline Control - Single Fab & Assembly Site
- Process Change Notification (PCN)
- Qualification & Reliability Data
- Solder (PbSn) Lead Finish is standard
- Enhanced Diminishing Manufacturing Sources (DMS) Support

Advantages

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near ground
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Wide supply
  - — Voltage range: 2.0V to 36V
  - — Single or dual supplies: ±1.0V to ±18V
- Very low supply current drain (0.4 mA) — independent of supply voltage
- Low input biasing current: 25 nA
- Low input offset current: ±5 nA
- Maximum offset voltage: ±3 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage,: 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Applications

- Selected Military Applications
- Selected Avionics Applications

Ordering Information

PART NUMBER	VID PART NUMBER	NS PACKAGE NUMBER (Note 3)
LM2903MEP	V62/04745-01	M08A
(Notes 1, 2)	TBD	TBD

Note 1: For the following (Enhanced Plastic) version, check for availability: - LM2903MXEP, LM2903NEP, LM2903ITLEP, LM2903ITLXEP. Parts listed with an "X" are provided in Tape & Reel and parts without an "X" are in Rails.

Note 2: FOR ADDITIONAL ORDERING AND PRODUCT INFORMATION, PLEASE VISIT THE ENHANCED PLASTIC WEB SITE AT: www.national.com/mil

Note 3: Refer to package details under Physical Dimensions

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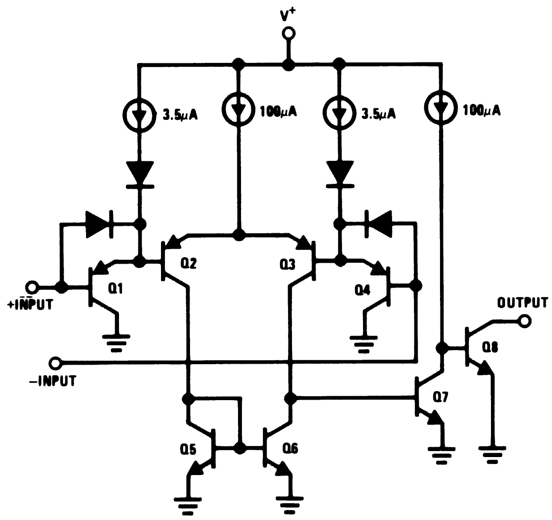
Schematic and Connection Diagrams



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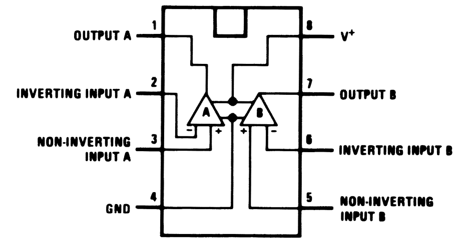
Dual-In-Line/SOIC Package



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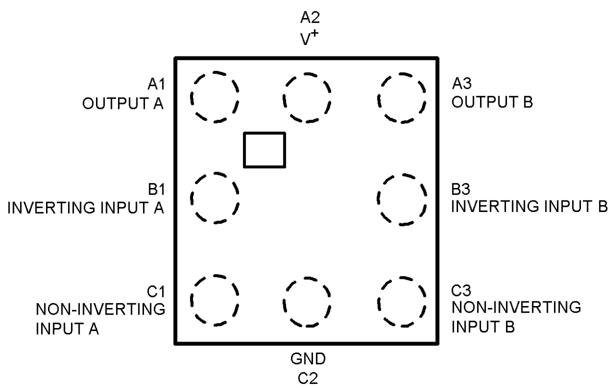
micro SMD



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Top View

Absolute Maximum Ratings (Note 14)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V^+	36V
Differential Input Voltage (Note 12)	36V
Input Voltage	−0.3V to +36V
Input Current (V_{IN}<−0.3V) (Note 7)	50 mA
Power Dissipation (Note 4)	
Molded DIP	780 mW
Small Outline Package	510 mW
Output Short-Circuit to Ground (Note 6)	Continuous
Operating Temperature Range	−40˚C to +85˚C
Storage Temperature Range	−65˚C to +150˚C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260˚C
Small Outline Package	215˚C
Vapor Phase (60 seconds)	
Infrared (15 seconds)	220˚C
ESD rating (1.5 kΩ in series with 100 pF)	1300V

Electrical Characteristics (Note 5)

(V^+=5V, T_A = 25˚C, unless otherwise stated)

Parameter	Conditions	LM2903			Units
		Min	Typ	Max	
Input Offset Voltage	(Note 13)		2.0	7.0	mV
Input Bias Current	I_{IN}(+) or I_{IN}(−) with Output In Linear Range, V_{CM} = 0V (Note 9)		25	250	nA
Input Offset Current	I_{IN}(+)−I_{IN}(−) V_{CM} = 0V		5.0	50	nA
Input Common Mode Voltage Range	V+ = 30V (Note 10)	0		V+−1.5	V
Supply Current	R_L=∞, V^+=5V		0.4	1.0	mA
	R_L=∞, V^+=36V		1	2.5	mA
Voltage Gain	R_L≥15 kΩ, V^+=15V V_O = 1V to 11V	25	100		V/mV
Large Signal Response Time	V_{IN}=TTL Logic Swing, V_{REF}=1.4V V_{RL}=5V, R_L=5.1 kΩ		300		ns
Response Time	V_{RL}=5V, R_L=5.1 kΩ (Note 11)		1.5		µs
Output Sink Current	V_{IN}(−)=1V, V_{IN}(+)=0, V_O≤1.5V	6.0	16		mA
Saturation Voltage	V_{IN}(−)=1V, V_{IN}(+)=0, I_{SINK}≤4 mA		250	400	mV
Output Leakage Current	V_{IN}(−)=0, V_{IN}(+)=1V, V_O=5V		0.1		nA

Electrical Characteristics (Notes 4, 5)

(V+ = 5V)

Parameter	Conditions	LM2903			Units
		Min	Typ	Max	
Input Offset Voltage	(Note 13)		9	15	mV
Input Offset Current	$I_{IN(+)}$−$I_{IN(-)}$, V_{CM}=0V		50	200	nA
Input Bias Current	I_{IN}(+) or I_{IN}(−) with Output in Linear Range, V_{CM}=0V (Note 9)		200	500	nA
Input Common Mode Voltage Range	V^+=30V (Note 10)	0		V^+−2.0	V
Saturation Voltage	V_{IN}(−)=1V, V_{IN}(+)=0, I_{SINK}≤4 mA		400	700	mV
Output Leakage Current	V_{IN}(−)=0, $V_{IN(+)}$=1V, V_O=30V			1.0	µA
Differential Input Voltage	Keep All V_{IN}'s≥0V (or V^-, if Used), (Note 12)			36	V

Electrical Characteristics (Notes 4, 5) (Continued)

Note 4: For operating at high temperatures, the LM2903EP must be derated based on a 125˚C maximum junction temperature and a thermal resistance of 170˚C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small (P_D≤100 mW), provided that the output transistors are allowed to saturate.

Note 5: "Testing and other quality control techniques are used to the extent deemed necessary to ensure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific PARAMETRIC testing, product performance is assured by characterization and/or design."

Note 6: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 7: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V.

Note 8: These specifications are limited to −40˚C≤T_A≤+85˚C.

Note 9: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 10: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+−1.5V at 25˚C, but either or both inputs can go to 36V without damage, independent of the magnitude of V^+.

Note 11: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

Note 12: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3V (or 0.3V below the magnitude of the negative power supply, if used).

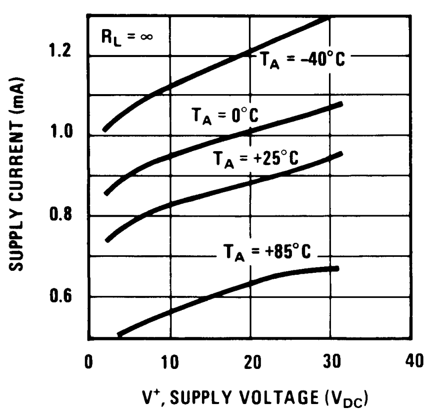
Note 13: At output switch point, V_O≃1.4V, R_S=0Ω with V^+ from 5V to 30V; and over the full input common-mode range (0V to V^+−1.5V), at 25˚C.

Note 14: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 15: The LM193 within this data sheet's graphics is referenced because of it's a similarity to the LM2903, however is not offered in this data sheet.

Typical Performance Characteristics

Supply Current



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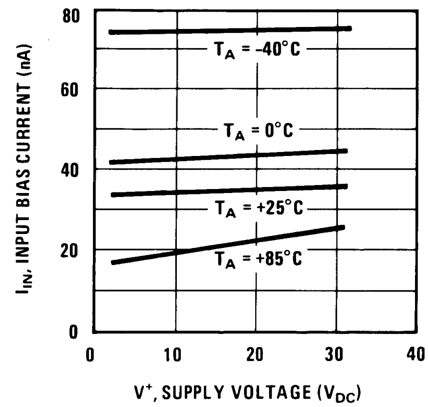
Input Current



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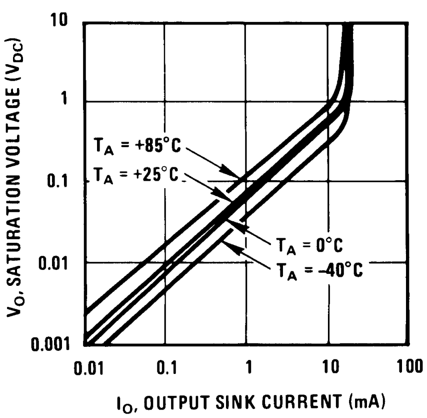
Output Saturation Voltage



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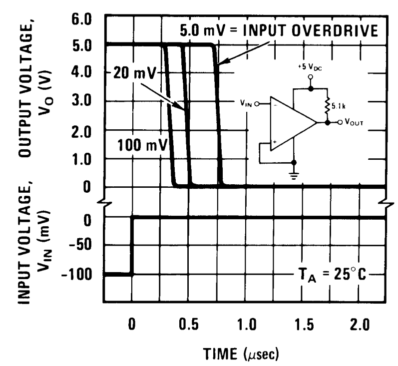
Response Time for Various Input Overdrives — Negative Transition



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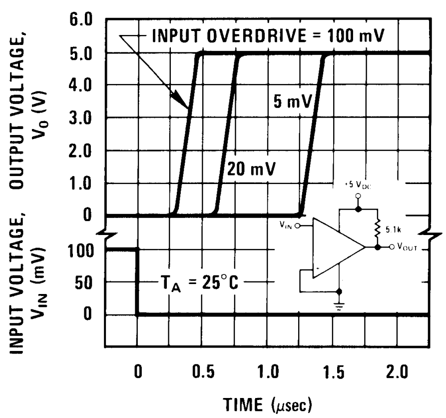
Response Time for Various Input Overdrives — Positive Transition



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Application Hints

The LM2903EP is a high gain, wide bandwidth device which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator change states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to < 10 kΩ reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All input pins of any unused comparators should be tied to the negative supply.

The bias network of the LM2903EP establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2.0 V_{DC} to 30 V_{DC}.

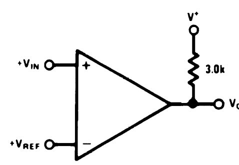
It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device (Note 12). Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25˚C). An input clamp diode can be used as shown in the applications section.

The output of the LM2903EP is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM2903EP package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω r_{SAT} of the output transistor. The low offset voltage of the output transistor (1.0mV) allows the output to clamp essentially to ground level for small load currents.

Typical Applications (V^+=5.0 V_{DC}) (Note 15)

Basic Comparator



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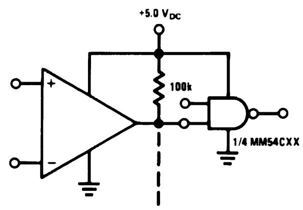
Driving CMOS



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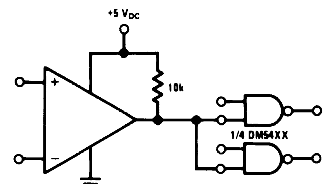
Driving TTL



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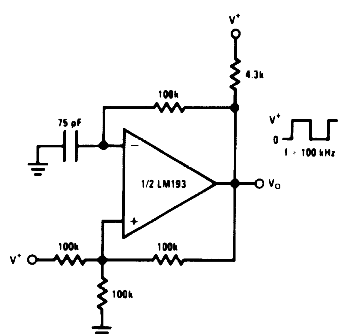
Squarewave Oscillator



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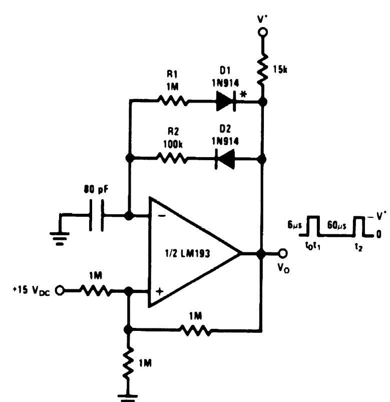
Pulse Generator



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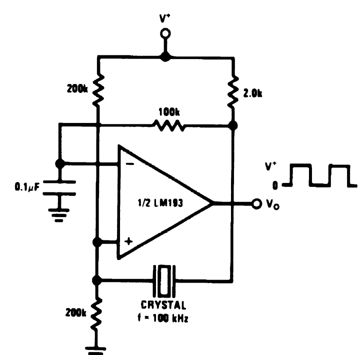
* For large ratios of R1/R2, D1 can be omitted.

Crystal Controlled Oscillator



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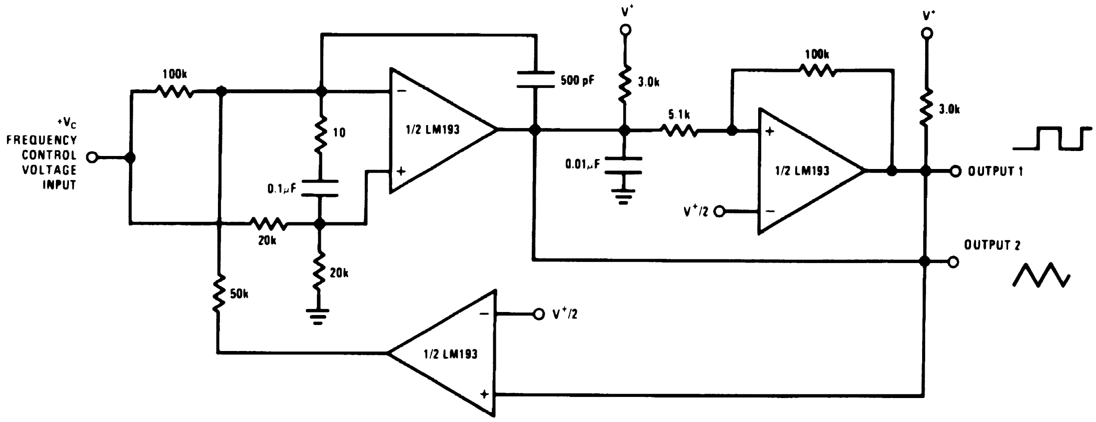
Typical Applications (V^+=5.0 V_{DC}) (Note 15) (Continued)

Two-Decade High Frequency VCO



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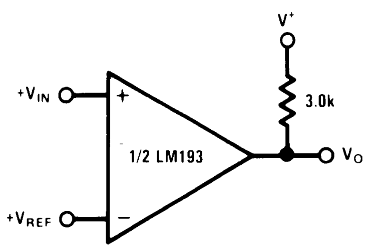
$V^* = +30\ V_{DC}$

$+250\ mV_{DC} \le V_C \le +50\ V_{DC}$

$700Hz \le f_o \le 100kHz$

Basic Comparator



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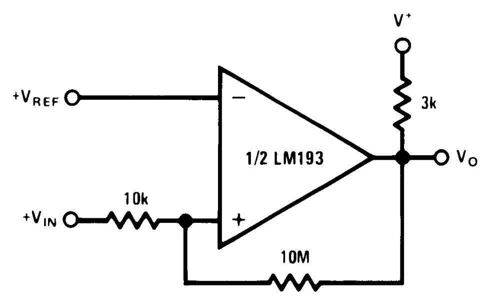
Non-Inverting Comparator with Hysteresis



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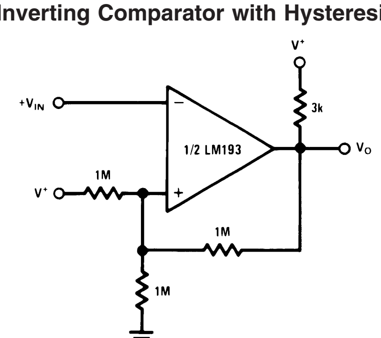
Inverting Comparator with Hysteresis



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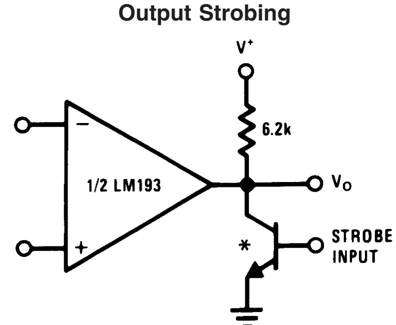
Output Strobing



* OR LOGIC GATE WITHOUT PULL-UP RESISTOR

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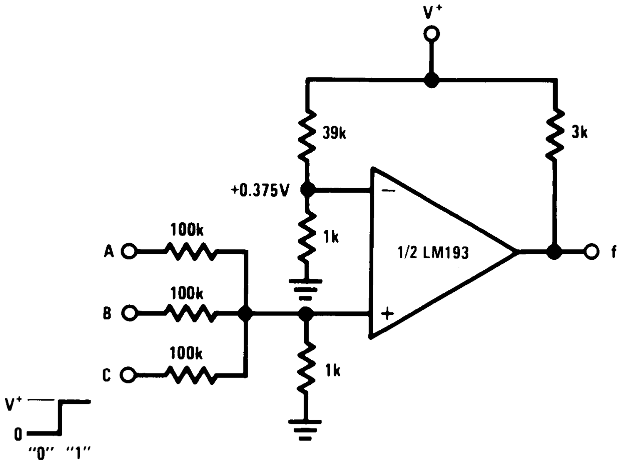
Typical Applications (V+=5.0 V_{DC}) (Note 15) (Continued)

AND Gate



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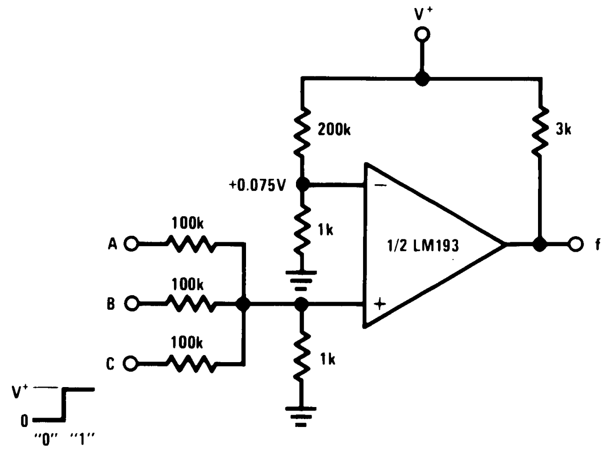
OR Gate



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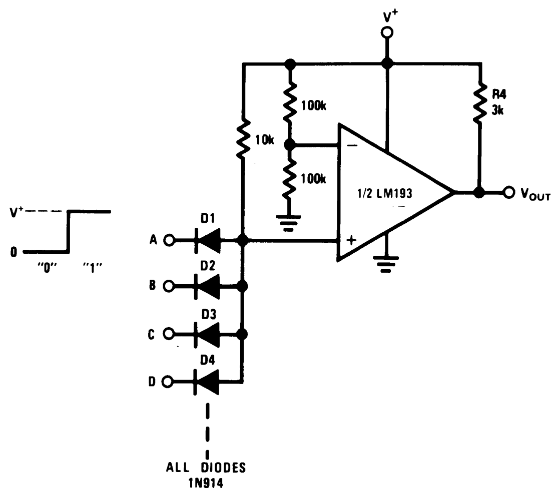
Large Fan-in AND Gate



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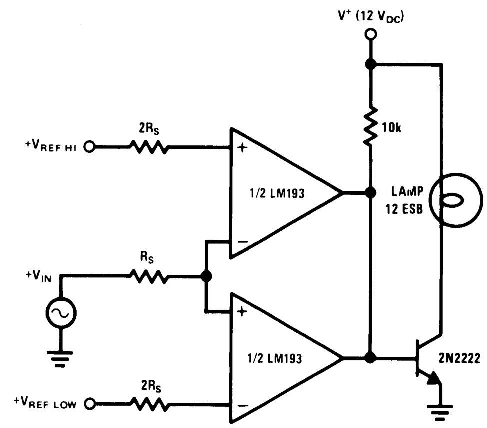
Limit Comparator



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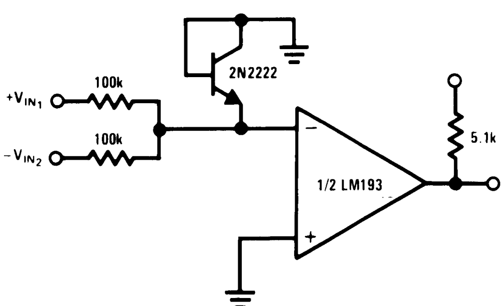
Comparing Input Voltages of Opposite Polarity



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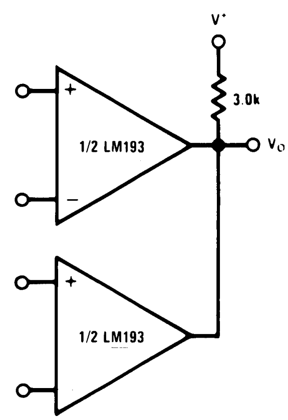
ORing the Outputs



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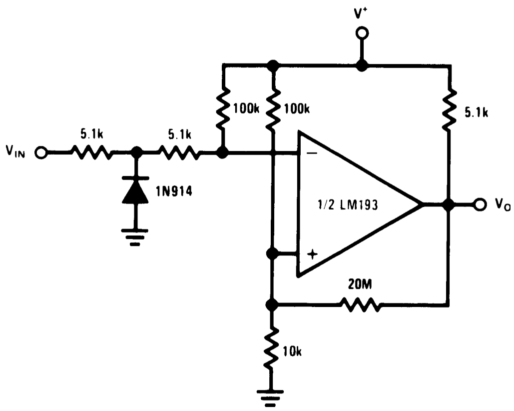
Typical Applications (V^{+}=5.0 V_{DC}) (Note 15) (Continued)

Zero Crossing Detector (Single Power Supply)



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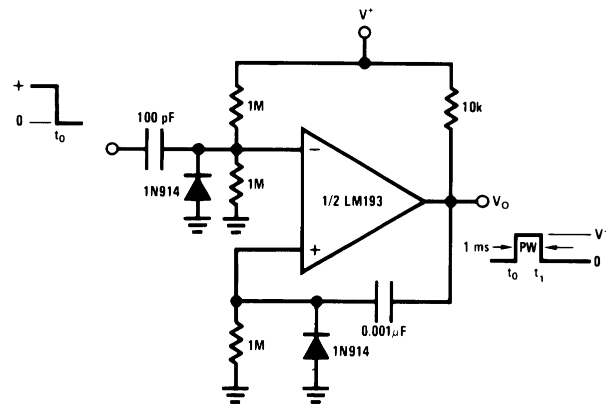
One-Shot Multivibrator



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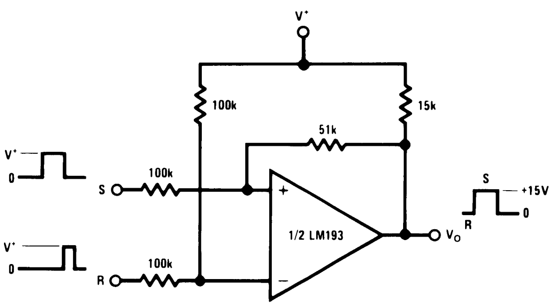
Bi-Stable Multivibrator



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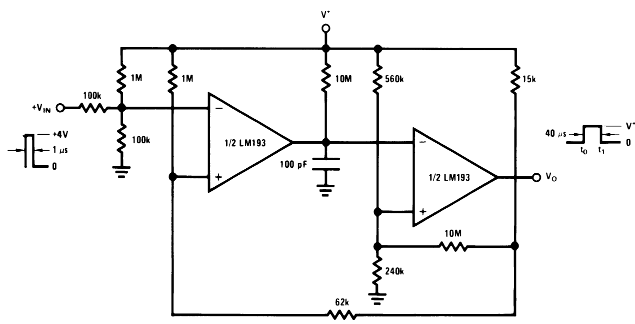
One-Shot Multivibrator with Input Lock Out



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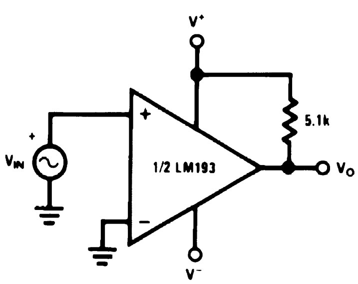
Zero Crossing Detector



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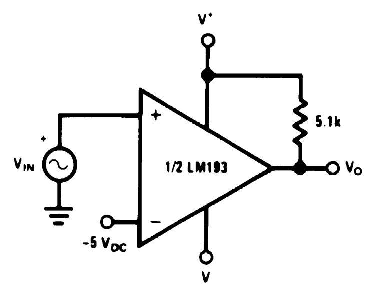
Comparator With a Negative Reference



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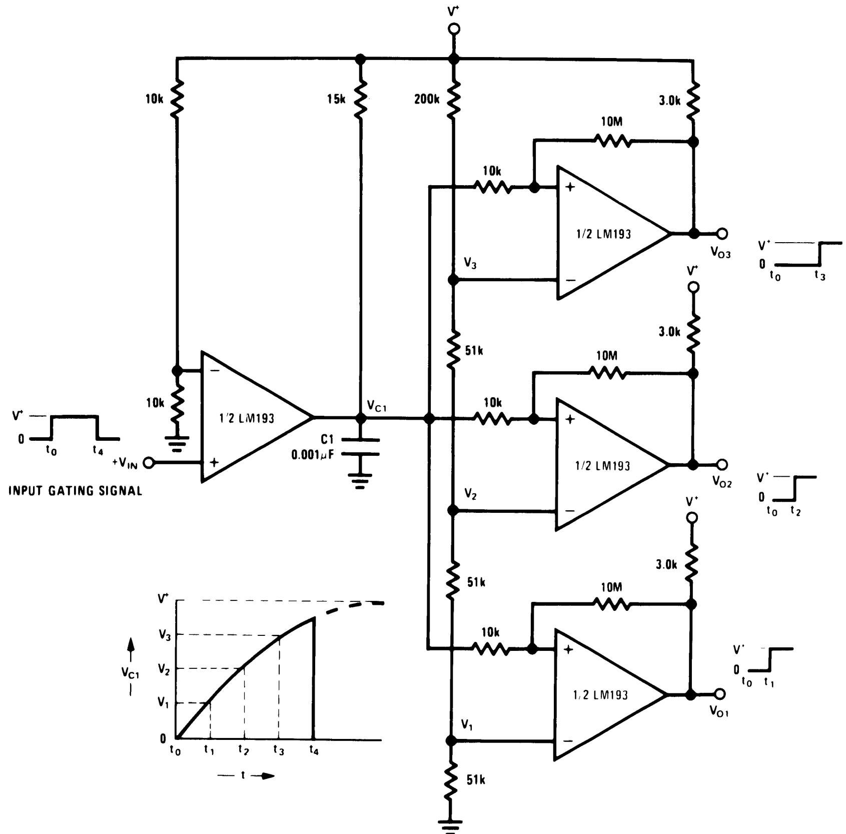
Typical Applications (V+=5.0 V_{DC}) (Note 15) (Continued)

Time Delay Generator



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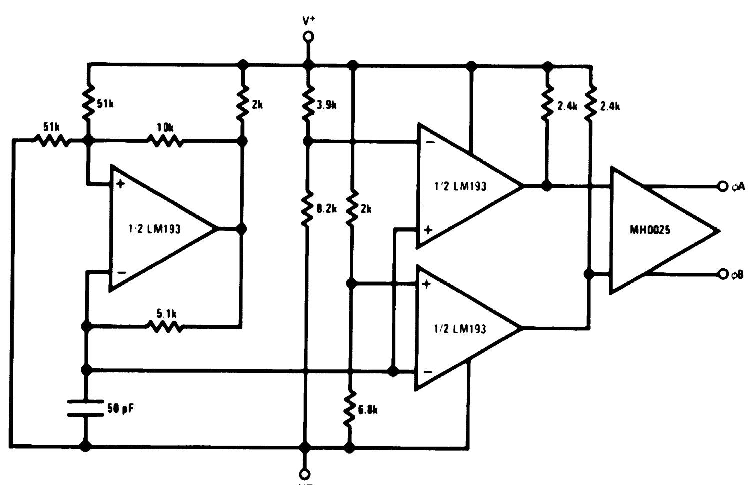
Split-Supply Applications (V+=+15 V_{DC} and V−=−15 V_{DC})

MOS Clock Driver



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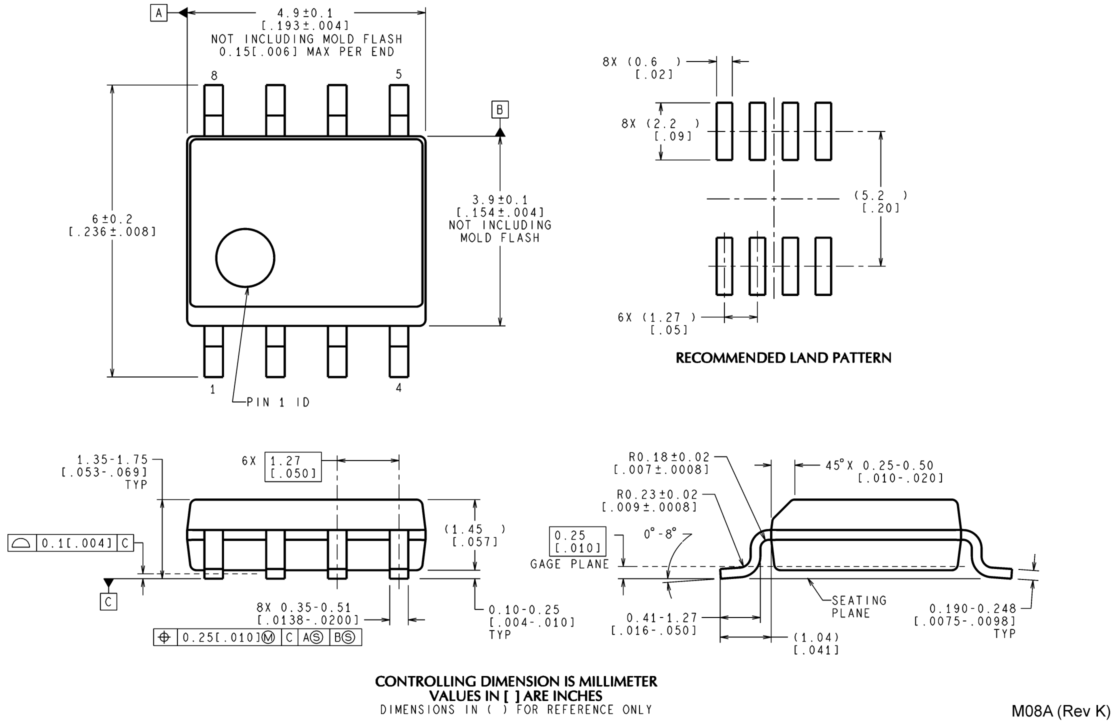
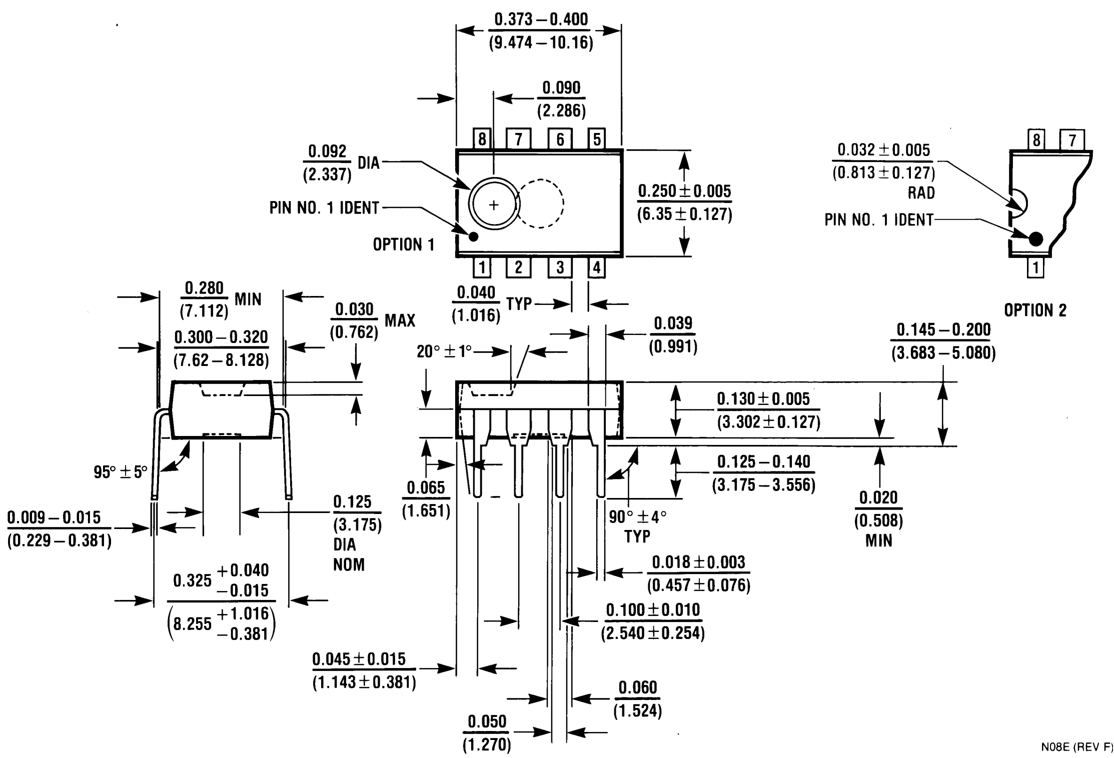
Physical Dimensions inches (millimeters) unless otherwise noted

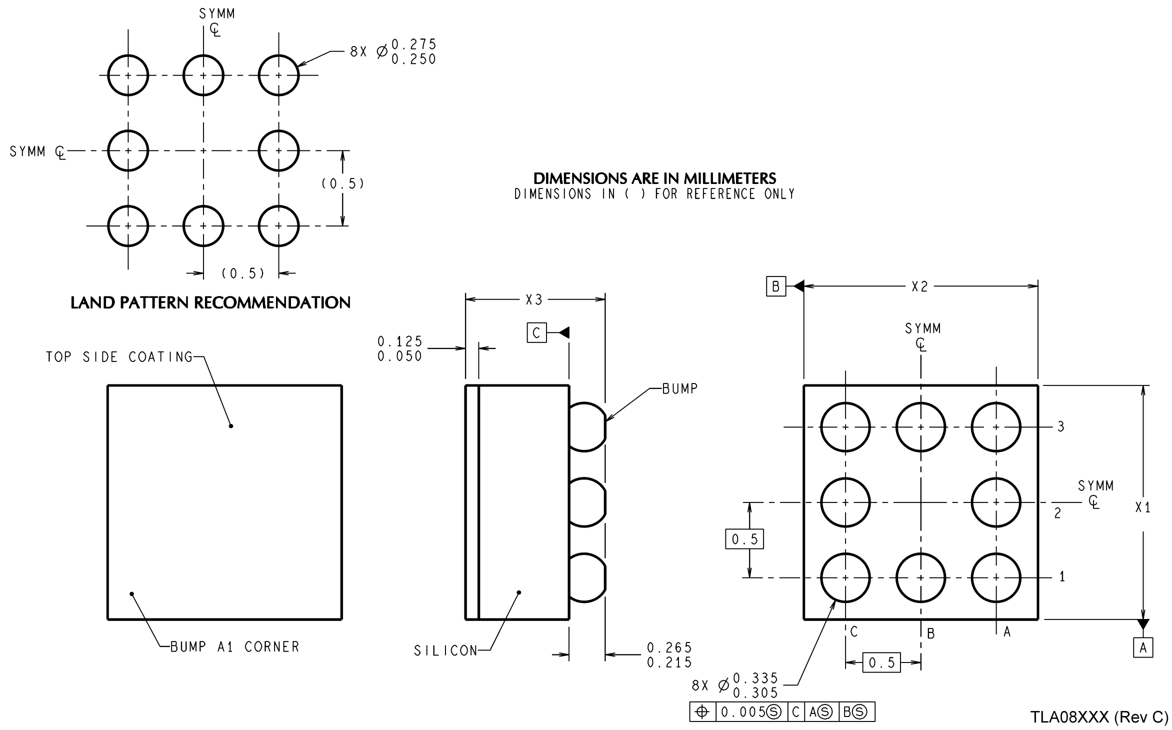


SOIC Package
NS Package Number M08A



Molded Dual-In-Line Package (N)
NS Package N08E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



8–Bump (12 mil) micro SMD Package
NS Package TLA08AAA
X_1 = 1,514mm X_2 = 1.514mm X_3 = 0.600mm

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