November 2000

National Semiconductor

LM2725/LM2726
High Speed Synchronous MOSFET Drivers

General Description

The LM2725/LM2726 is a family of dual MOSFET drivers that can drive both the top MOSFET and bottom MOSFET in a push-pull structure simultaneously. It takes a logic level PWM input and splits it into two complimentary signals with a typical 20ns dead time in between. The built-in shoot-through protection circuitry prevents the top and bottom FETs from turning on simultaneously. With a bias voltage of 5V, the peak sourcing and sinking current for each driver of the LM2725 is about 1.2A and that of the LM2726 is about 3A. In an SO-8 package, each driver is able to handle 50mA average current. Input UVLO (Under-Voltage-Lock-Out) ensures that all the driver outputs stay low until the supply rail exceeds the power-on threshold during system power on, or after the supply rail drops below power-on threshold by a specified hysteresis during system power down. The cross-conduction protection circuitry detects both the driver outputs and will not turn on a driver until the other driver output is low. The top gate bias voltage needed by the top MOSFET can be obtained through an external bootstrap structure. Minimum pulse width is as low as 55ns.

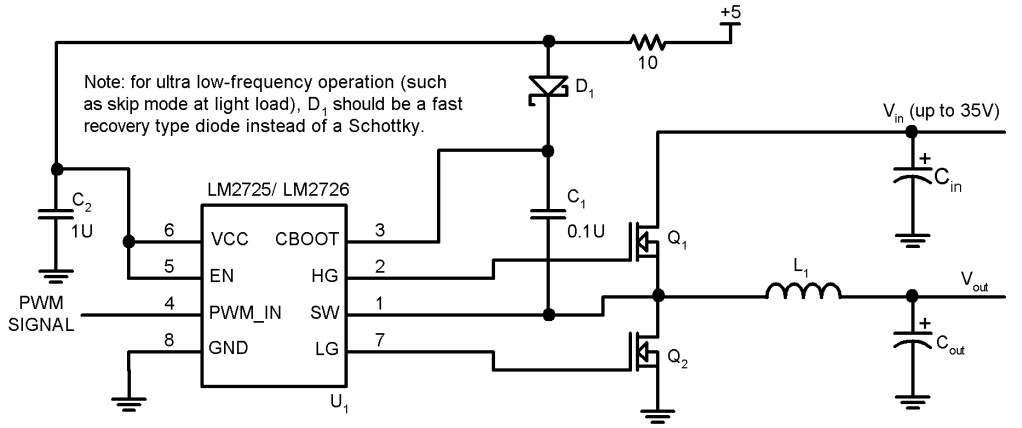
Features

- High peak output current
- Adaptive shoot-through protection
- 36V SW pin absolute maximum voltage
- Input Under-Voltage-Lock-Out
- Typical 20ns internal delay
- Plastic 8-pin SO package

Applications

- High Current DC/DC Power Supplies
- High Input Voltage Switching Regulators
- Microprocessors

Typical Application



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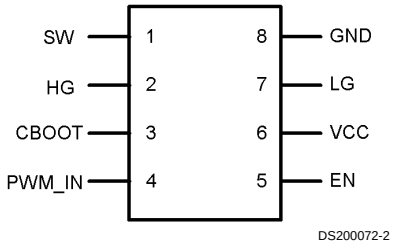
Connection Diagram

8-Lead Small Outline Package



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Top View

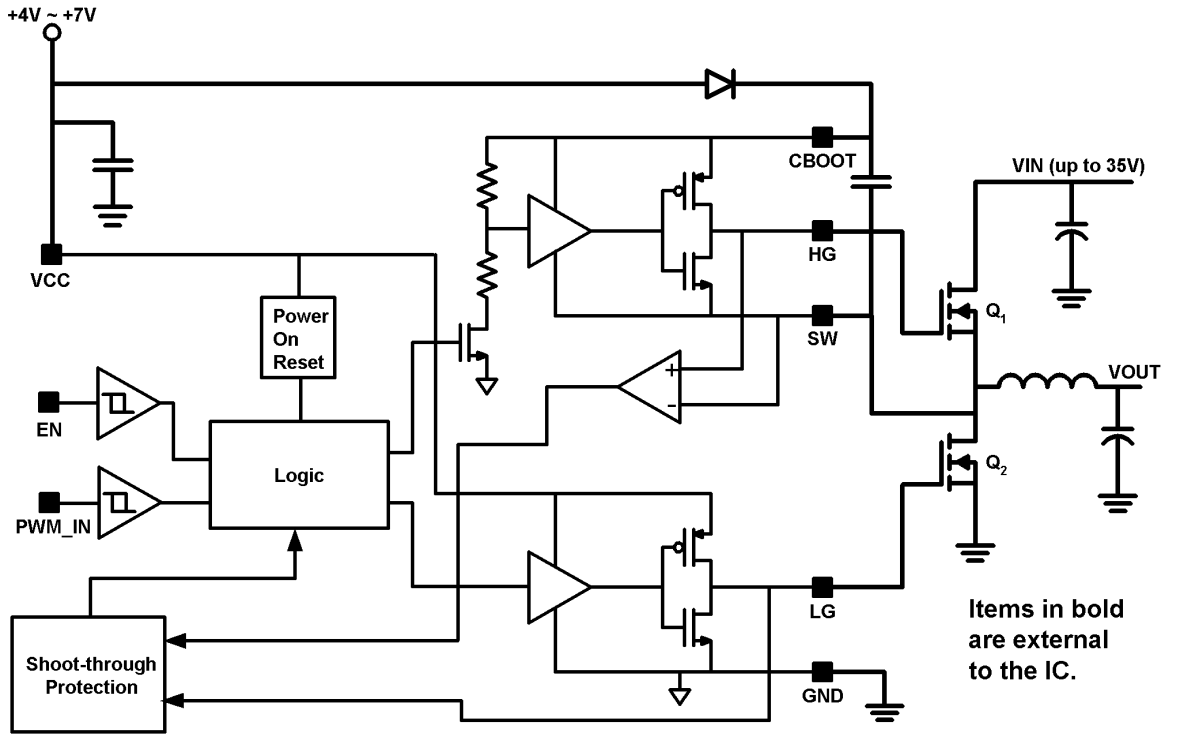
Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM2725	LM2725M	M08A	95 Units/Rail
	LM2725MX		2500 Units/Reel
LM2726	LM2726M		95 Units/Rail
	LM2726MX		2500 Units/Reel

Pin Description

Pin	Name	Function
1	SW	Top driver return. Should be connected to the common node of top and bottom FETs
2	HG	Top gate drive output
3	CBOOT	Bootstrap. Accepts a bootstrap voltage for powering the high-side driver
4	PWM_IN	Accepts a 5V-logic control signal
5	EN	Chip Enable
6	VCC	Connect to +5V supply
7	LG	Bottom gate drive output
8	GND	Ground

Block Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

VCC	7.5V
CBOOT	42V
CBOOT to SW	8V
SW to PGND	36V
Junction Temperature	+150˚C
Power Dissipation (Note 2)	720mW
Storage Temperature	−65˚ to 150˚C
ESD Susceptibility	
Human Body Model (Note 3)	1 kV
Soldering Time, Temperature	10sec., 300˚C

Operating Ratings (Note 1)

VCC	4V to 7V
Junction Temperature Range	0˚ to 125˚C

Electrical Characteristics LM2725

VCC = CBOOT = 5V, SW = GND = 0V, unless otherwise specified. Typicals and limits appearing in plain type apply for $T_A = T_J = +25^{\circ}C$. Limits appearing in **boldface** type apply over the entire operating temperature range.

Symbol	Parameter	Condition	Min	Typ	Max	Units
POWER SUPPLY						
I_{q_op}	Operating Quiescent Current	PWM_IN = 0V		180	**250**	µA
I_{q_sd}	Shutdown Quiescent Current	EN = 0V, PWM_IN = 0V		0.5	**15**	µA
TOP DRIVER						
	Peak Pull-Up Current	Test Circuit 1, V_{bias} = 5V, R = 0.1Ω		1.2		A
	Pull-Up Rds_on	$I_{CBOOT} = I_{HG}$ = 0.7A		2.4		Ω
	Peak Pull-down Current	Test Circuit 2, V_{bias} = 5V, R = 0.1Ω		−1.0		A
	Pull-down Rds_on	$I_{SW} = I_{HG}$ = 0.7A		1.4		Ω
t_4	Rise Time	Timing Diagram, C_{LOAD} = 3.3nF		17		ns
t_6	Fall Time			10		ns
t_3	Pull-Up Dead Time	Timing Diagram		23		ns
t_5	Pull-Down Delay	Timing Diagram, from PWM_IN Falling Edge		21		ns
BOTTOM DRIVER						
	Peak Pull-Up Current	Test Circuit 3, V_{bias} = 5V, R = 0.1Ω		1.2		A
	Pull-up Rds_on	$I_{VCC} = I_{LG}$ = 0.7A		2.6		Ω
	Peak Pull-down Current	Test Circuit 4, V_{bias} = 5V, R = 0.1Ω		−2		A
	Pull-down Rds_on	$I_{GND} = I_{LG}$ = 0.7A		0.65		Ω
t_8	Rise Time	Timing Diagram, C_{LOAD} = 3.3nF		18		ns
t_2	Fall Time			6		ns
t_7	Pull-up Dead Time	Timing Diagram		28		ns
t_1	Pull-down Delay	Timing Diagram, from PWM_IN Rising Edge		15		ns
LOGIC						
V_{uvlo_up}	Power On Threshold	VCC rises from 0V toward 5V		3.0		V
V_{uvlo_dn}	Under-Voltage-Lock-Out Threshold			2.5		V
V_{uvlo_hys}	Under-Voltage-Lock-Out Hysteresis			0.5		V

Electrical Characteristics
LM2725 (Continued)

VCC = CBOOT = 5V, SW = GND = 0V, unless otherwise specified. Typicals and limits appearing in plain type apply for $T_A = T_J = +25^{\circ}C$. Limits appearing in **boldface** type apply over the entire operating temperature range.

Symbol	Parameter	Condition	Min	Typ	Max	Units
LOGIC						
V_{IH_EN}	EN Pin High Input		**2.4**			V
V_{IL_EN}	EN Pin Low Input				**0.8**	V
I_{leak_EN}	EN Pin Leakage Current	EN = VCC = 5V	**−2**		**2**	µA
		VCC = 5V, EN = 0V	**−2**		**2**	
t_{on_min}	Minimum Positive Input Pulse Width (Note 4)			55		ns
t_{off_min}	Minimum Negative Input Pulse Width (Note 5)			55		
V_{IH_PWM}	PWM_IN High Level Input Voltage	When PWM_IN pin goes high from 0V	**2.4**			V
V_{IL_PWM}	PWM_IN Low Level Input Voltage	When PWM_IN pin goes low from 5V			**0.8**	

Electrical Characteristics
LM2726

VCC = CBOOT = 5V, SW = GND = 0V, unless otherwise specified. Typicals and limits appearing in plain type apply for $T_A = T_J = +25^{\circ}C$. Limits appearing in **boldface** type apply over the entire operating temperature range.

Symbol	Parameter	Condition	Min	Typ	Max	Units
POWER SUPPLY						
I_{q_op}	Operating Quiescent Current	PWM_IN = 0V		185	**250**	µA
I_{q_sd}	Shutdown Quiescent Current	EN = 0V, PWM_IN = 0V		0.5	**15**	µA
TOP DRIVER						
	Peak Pull-Up Current	Test Circuit 1, V_{bias} = 5V, R = 0.1Ω		3.0		A
	Pull-Up Rds_on	$I_{CBOOT} = I_{HG}$ = 1.0A		1.2		Ω
	Peak Pull-down Current	Test Circuit 2, V_{bias} = 5V, R = 0.1Ω		−3.2		A
	Pull-down Rds_on	$I_{SW} = I_{HG}$ = 1.0A		0.5		Ω
t_4	Rise Time	Timing Diagram, C_{LOAD} = 3.3nF		17		ns
t_6	Fall Time			12		ns
t_3	Pull-Up Dead Time	Timing Diagram		19		ns
t_5	Pull-Down Delay	Timing Diagram, from PWM_IN from Falling Edge		27		ns
BOTTOM DRIVER						
	Peak Pull-Up Current	Test Circuit 3, V_{bias} = 5V, R = 0.1Ω		3.2		A
	Pull-up Rds_on	$I_{VCC} = I_{LG}$ = 1.0A		1.1		Ω
	Peak Pull-down Current	Test Circuit 4, V_{bias} = 5V, R = 0.1Ω		−3.2		A
	Pull-down Rds_on	$I_{GND} = I_{LG}$ = 1.0A		0.6		Ω
t_8	Rise Time	Timing Diagram, C_{LOAD} = 3.3nF		17		ns
t_2	Fall Time			14		ns
t_7	Pull-up Dead Time	Timing Diagram		12		ns

Electrical Characteristics

LM2726 (Continued)

VCC = CBOOT = 5V, SW = GND = 0V, unless otherwise specified. Typicals and limits appearing in plain type apply for $T_A = T_J = +25^\circ C$. Limits appearing in **boldface** type apply over the entire operating temperature range.

Symbol	Parameter	Condition	Min	Typ	Max	Units
BOTTOM DRIVER						
t_1	Pull-down Delay	Timing Diagram, from PWM_IN Rising Edge		13		ns
LOGIC						
V_{uvlo_up}	Power On Threshold	VCC rises from 0V toward 5V		2.8		V
V_{uvlo_dn}	Under-Voltage-Lock-Out Threshold			2.5		V
V_{uvlo_hys}	Under-Voltage-Lock-Out Hysteresis			0.3		V
V_{IH_EN}	EN Pin High Input		**2.4**			V
V_{IL_EN}	EN Pin Low Input				**0.25**	V
I_{leak_EN}	EN Pin Leakage Current	EN = VCC = 5V	**−2**		**2**	µA
		VCC = 5V, EN = 0V	**−2**		**2**	
t_{on_min}	Minimum Positive Input Pulse Width (Note 4)			55		ns
t_{off_min}	Minimum Negative Input Pulse Width (Note 5)			55		
V_{IH_PWM}	PWM_IN High Level Input Voltage	When PWM_IN pin goes high from 0V	**2.4**			V
V_{IL_PWM}	PWM_IN Low Level Input Voltage	When PWM_IN pin goes low from 5V			**0.25**	

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. **Operating ratings** are conditions under which the device operates correctly. Operating Ratings do not imply guaranteed performance limits.

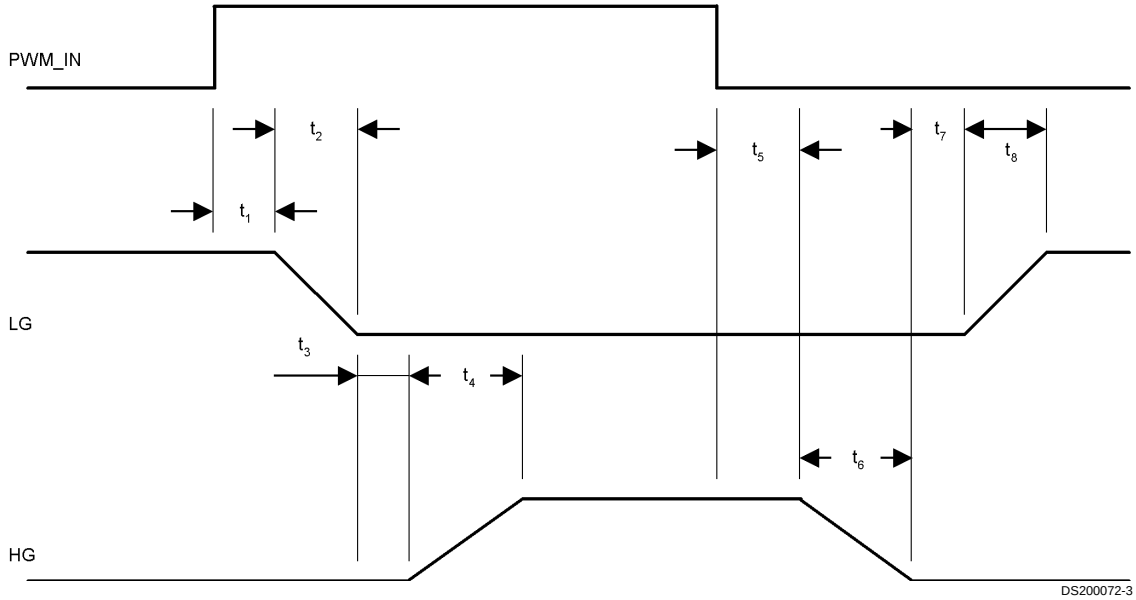
Note 2: Maximum allowable power dissipation is a function of the maximum junction temperature, T_{JMAX}, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{MAX} = (T_{JMAX}-T_A) / \theta_{JA}$. The junction-to-ambient thermal resistance, θ_{JA}, for LM2725/LM2726 is 172°C/W. For a T_{JMAX} of 150°C and T_A of 25°C, the maximum allowable power dissipation is 0.7W.

Note 3: ESD machine model susceptibility is 100V.

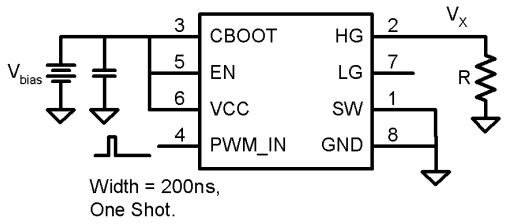
Note 4: If after a rising edge, a falling edge occurs sooner than the specified value, the IC may intermittently fail to turn on the bottom gate when the top gate is off. As the falling edge occurs sooner and sooner, the driver may start to ignore the pulse and produce no output.

Note 5: If after a falling edge, a rising edge occurs sooner than the specified value, the IC may intermittently fail to turn on the top gate when the bottom gate is off. As the rising edge occurs sooner and sooner, the driver may start to ignore the pulse and produce no output.

Timing Diagram



Test Circuits



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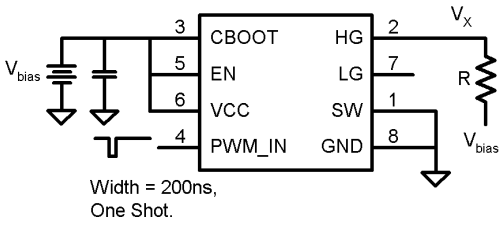
Test Circuit 1



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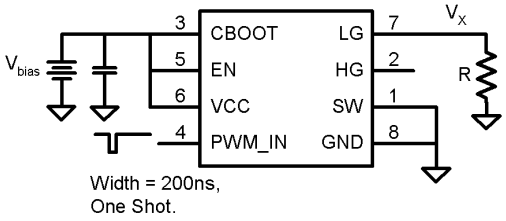
Test Circuit 2



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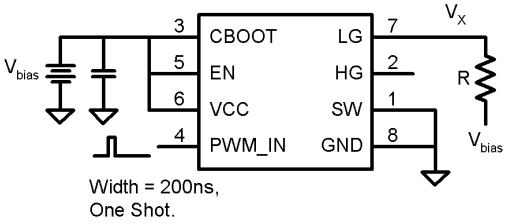
Test Circuit 3



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Test Circuit 4

$$I_{pull\_up} = \frac{V_x}{R}$$

$$I_{pull\_down} = \frac{V_{bias} - V_x}{R}$$

$$R_{ds\_pull\_up} = \frac{V_{bias} - V_x}{V_x} \cdot R$$

$$R_{ds\_pull\_up} = \frac{V_x}{V_{bias} - V_x} \cdot R$$

Typical Waveforms

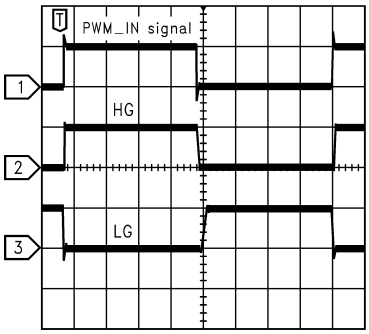


FIGURE 1. Switching Waveforms of Test Circuit

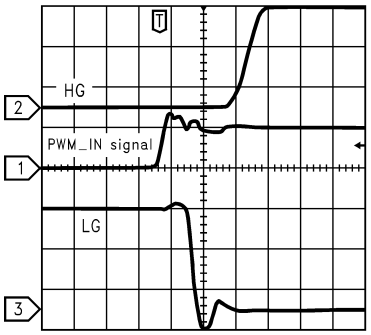


FIGURE 2. When Input Goes High

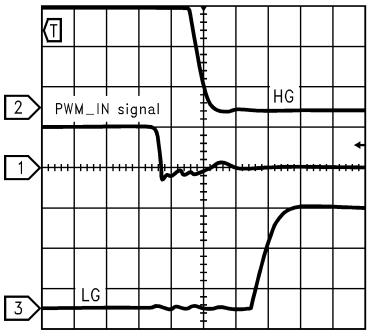


FIGURE 3. When Input Goes Low

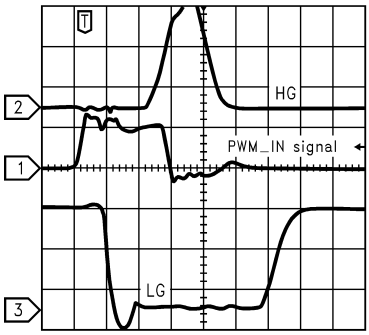
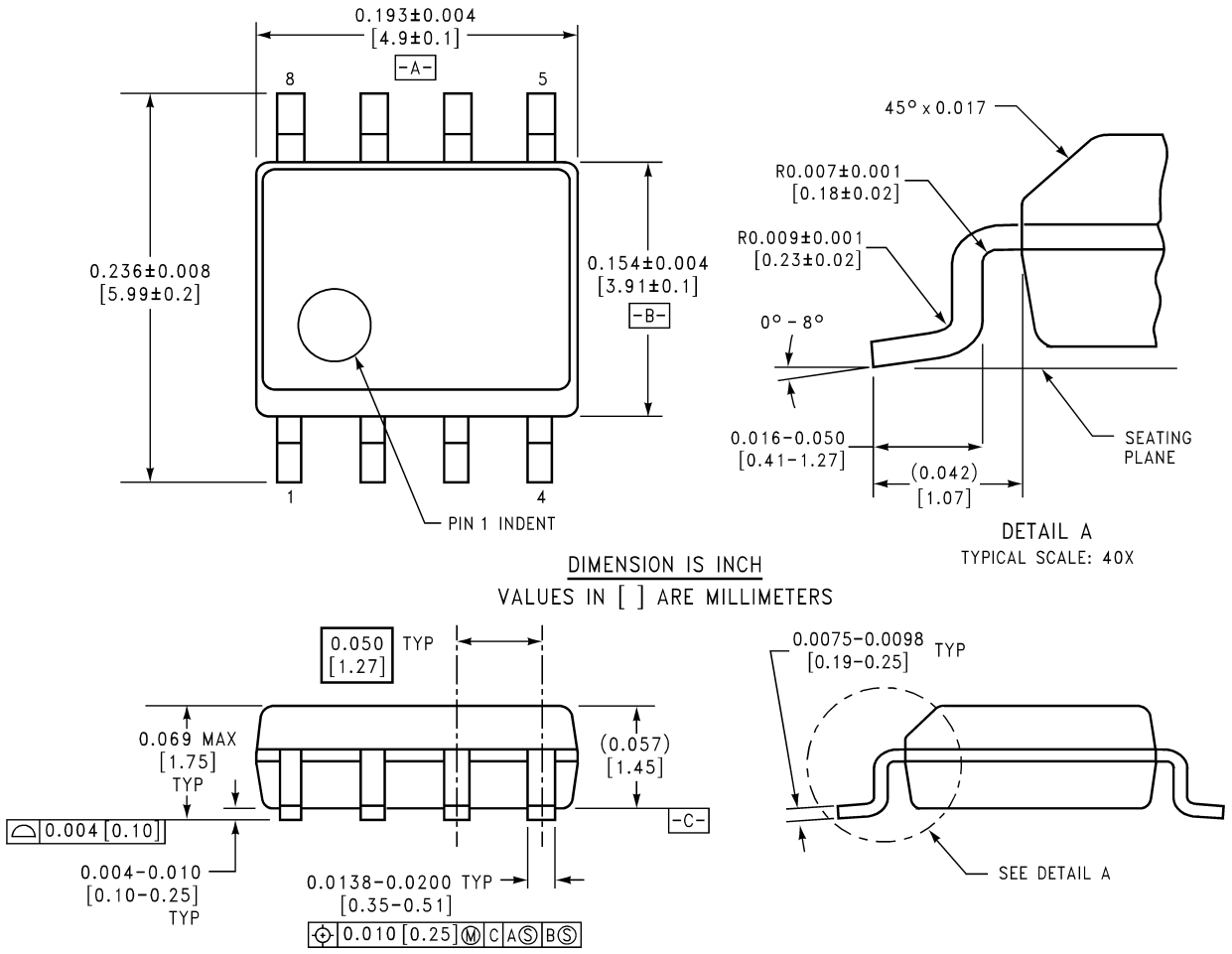


FIGURE 4. Minimum Positive Pulse

Physical Dimensions inches (millimeters) unless otherwise noted



8-Lead Small Outline Package
NS Package Number M08A

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