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National Semiconductor

LM2476
Monolithic Triple Channel 6.5 ns High Gain CRT Driver and Bias Clamp

General Description

The LM2476 is a monolithic triple channel CRT driver and triple bias clamp for low-cost color monitor applications. The highly integrated IC contains three wide-band amplifiers for driving the RGB cathodes of a CRT through external coupling capacitors and three low-band clamp amplifiers for DC restoration and cutoff adjustment of the video outputs. The CRT drivers have a high, fixed gain of -27 and can drive CRT capacitive loads as well as resistive loads present in other applications, limited only by the package's power dissipation.

The IC is packaged in a 19-lead TO-247 molded plastic package and must be operated with a properly chosen heat sink. See the Package Mounting and Thermal Considerations sections for more information.

Features

- Well-matched to the LM123X/4X family of preamplifiers
- Operates with V_{CC} = 60V to 90V
- Convenient TO-247 staggered lead package style

CRT Drivers

- High gain of –27 for up to 60V_{P-P} output swing
- Stable with capacitive loads and inductive peaking networks

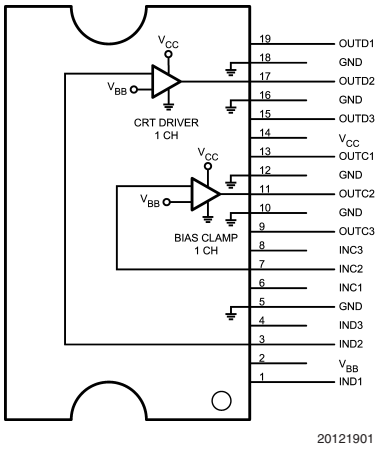
Bias Clamps

- Gain of –17 for up to 60V DC output range

Applications

- 1024 x 768 displays up to 85 Hz refresh rate
- Pixel clock frequencies up to 95 MHz
- Monitors using video blanking

Pinout Diagram and Pin Descriptions



Note: Tab is at GND

FIGURE 1. Pinout and Connection Diagram

Pin Name	Pin Description
IND	Driver Input Pins (1, 3, 4)
INC	Clamp Input Pins (6, 7, 8)
V_{BB}	Bias Voltage Pin (2)
V_{CC}	Supply Voltage Pin (14)
GND*	Ground Pins (5, 10, 12, 16, 18)
OUTC	Clamp Output Pins (9, 11, 13)
OUTD	Driver Output Pins (15, 17, 19)

***Note:** All GND pins should be connected together via low HF impedance traces on the PCB.

Schematic Diagrams

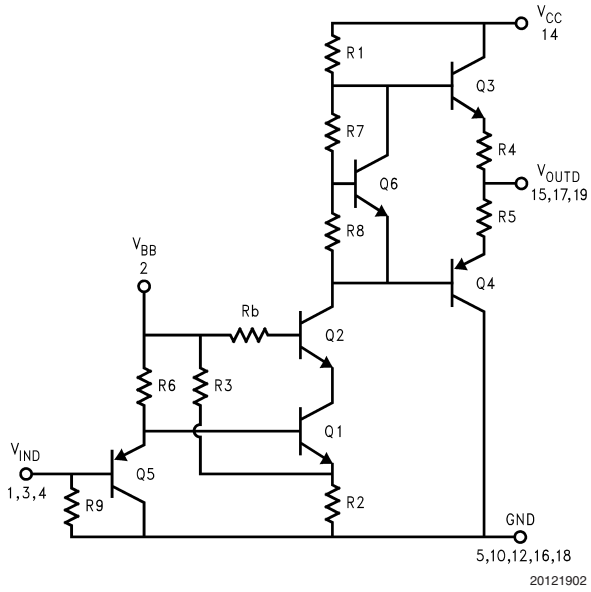


FIGURE 2. CRT Driver Simplified Schematic (One Channel)

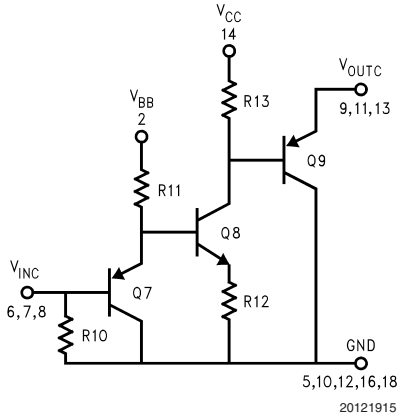


FIGURE 3. Bias Clamp Simplified Schematic (One Channel)

Absolute Maximum Ratings (Notes 1, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	96V
Bias Voltage (V_{BB})	10V
Driver Input Voltage (V_{IND})	0V to 4.5V
Clamp Input Voltage (V_{INC})	0V to 5.0V
Storage Temperature Range (T_{STG})	−65˚C to +150˚C
Lead Temperature (Soldering, <10 sec.)	300˚C

ESD Tolerance

Human Body Model	2 KV
Machine Model	200V

Operating Ranges (Note 2)

V_{CC}	60V to 85V
V_{BB}	7V to 9V
V_{IND}	0V to 3.5V
V_{INC}	0V to 4.0V
V_{OUTD} (Driver Output Voltage)	12V to V_{CC}
V_{OUTC} (Clamp Output Voltage)	12V to V_{CC}
Case Temperature (device tab)	−20˚C to +100˚C

Do not operate the part without a heat sink.

Electrical Characteristics

(See *Figure 4* for Test Circuit)
Unless otherwise noted: V_{CC} = 85V, V_{BB} = 8V, C_L = 8 pF, T_C = 40˚C
DC Tests: V_{IND} = 2.30V, V_{INC} = 2.35V
AC Tests: V_{OUTD} = 40V_{P-P} (35V − 75V) at 1 MHz, V_{INC} = 2.35V

Symbol	Parameter	Conditions	LM2476			Units
			Min	Typical	Max	
I_{CC}	Supply Current	All Three Channels, No AC Input Signal, No Output Load		34	45	mA
I_{BB}	Bias Current	All Three Channels, No AC Input Signal, No Output Load		21	30	mA
$V_{OUTD, 1}$	Driver DC Output Voltage	No AC Input Signal, V_{IND} = 2.30V	41	46	51	V
$V_{OUTD, 2}$	Driver DC Output Voltage	No AC Input Signal, V_{IND} = 1.15V	72	77	82	V
A_{V-OUTD}	Driver DC Voltage Gain	No AC Input Signal	−24	−27	−30	
ΔA_{V-OUTD}	Driver Gain Matching	(Note 4), No AC Input Signal		1.0		dB
LE_{OUTD}	Driver Linearity Error	(Notes 4, 5), No AC Input Signal		5		%
t_R	Rise Time	(Note 6), 10% to 90%		6.0		ns
t_F	Fall Time	(Note 6), 90% to 10%		6.7		ns
OS	Overshoot	(Note 6)		3		%
V_{OUTC}	Clamp DC Output Voltage	V_{INC} = 2.35V	46	51	56	V
$V_{OUTC-RANGE}$	Clamp DC Output Voltage Range	$V_{INC-RANGE}$ = 0.5V to 4.0V		58		VDC
A_{V-OUTC}	Clamp DC Voltage Gain	No AC Input Signal	−14.5	−16.5	−18.5	
LE_{OUTC}	Clamp Linearity Error	(Notes 4, 5), No AC Input Signal		5		%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may change when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to GND, unless otherwise specified.

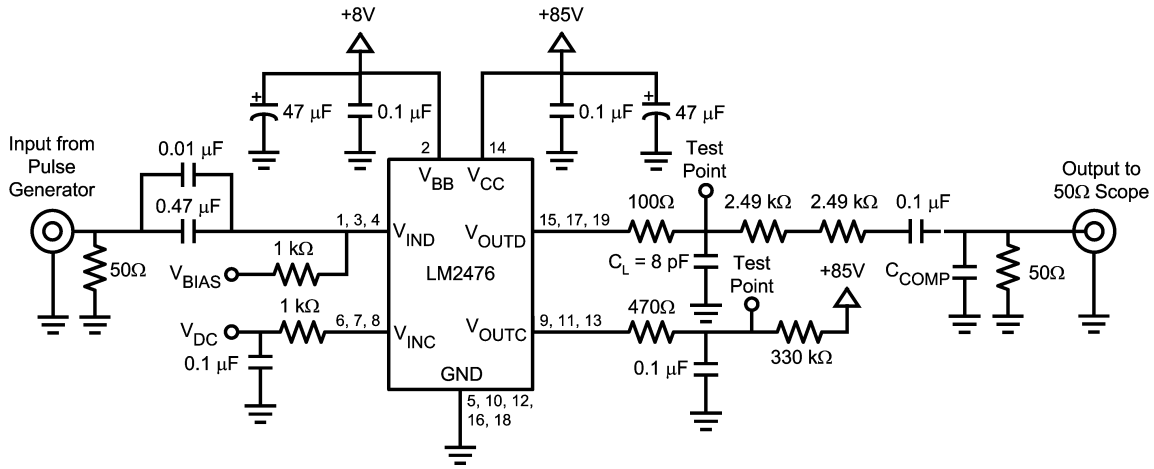
Note 4: Calculated value from Voltage Gain test on each channel.

Note 5: Driver Linearity Error is the variation in dc gain from V_{IND} = 1.1V to V_{IND} = 3.6V.

Note 6: Input from signal generator: t_r, t_f < 1 ns.

Note 7: Clamp Linearity Error is the variation in dc gain from V_{INC} = 1.0V to V_{INC} = 4.0V.

LM2476 Test Circuits



Note: 8 pF load includes parasitic capacitance.

FIGURE 4. CRT Driver and Bias Clamp Test Circuits (One Channel)

Figure 4 shows a typical test circuit to evaluate the LM2476 CRT Driver and Bias Clamp electrical characteristics. The driver test circuit is designed to allow for testing the transient response in a 50Ω environment without the use of an expensive FET probe. An input from a 50Ω pulse generator output can be AC coupled and biased with an external supply via the V_{BIAS} input. The two 2.49 kΩ resistors form a 200:1 divider with the 50Ω resistor and the oscilloscope. The clamp test circuit is designed to allow for testing the clamp outputs. A clamp input can be biased with an external supply via the V_{DC} input and a high impedance voltmeter (>100MΩ) can be used to measure the DC voltage at the clamp outputs. Test points can included to accommodate voltmeter or oscilloscope probes.

Typical Performance Characteristics

(V_{CC} = 85V, V_{BB} = 8V, C_L = 8 pF, V_{OUTD} = 40V_{P-P} (35V – 75V), V_{INC} = 2.35V, Test Circuit - *Figure 4* unless otherwise specified)

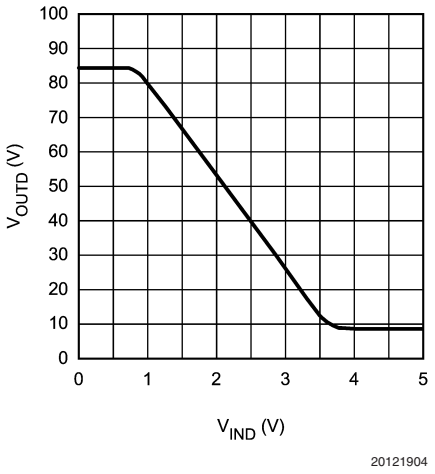


FIGURE 5. V_{OUTD} vs V_{IND}

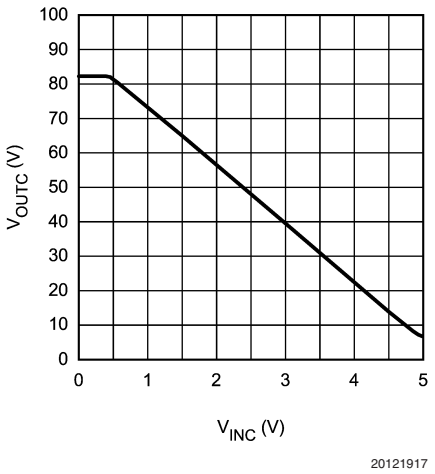


FIGURE 6. V_{OUTC} vs V_{INC}

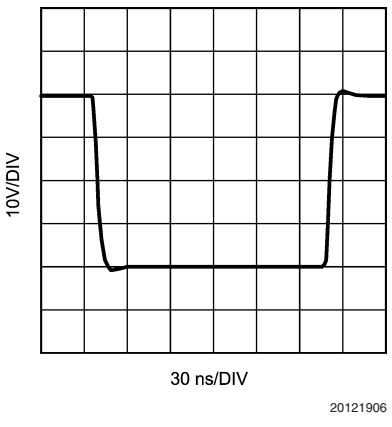


FIGURE 7. LM2476 Pulse Response

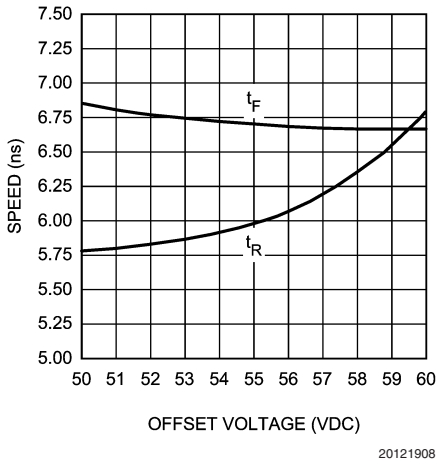


FIGURE 8. Speed vs Offset

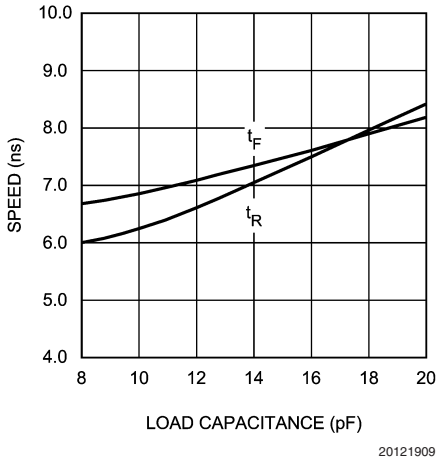


FIGURE 9. Speed vs Load Capacitance

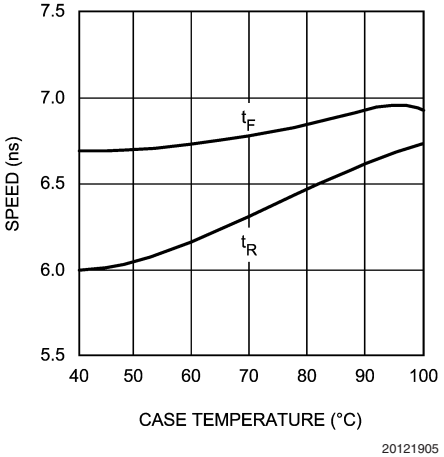


FIGURE 10. Speed vs Temperature

Typical Performance Characteristics (V_{CC} = 85V, V_{BB} = 8V, C_L = 8 pF, V_{OUTD} = 40V_{P-P} (35V – 75V), V_{INC} = 2.35V, Test Circuit - *Figure 4* unless otherwise specified) (Continued)

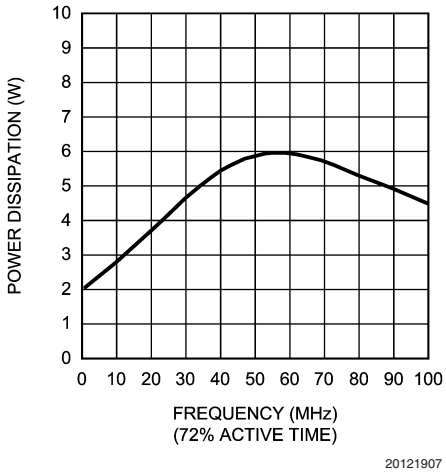


FIGURE 11. Power Dissipation vs Frequency

Theory of Operation

The LM2476 is a high voltage monolithic three channel CRT driver and triple bias clamp suitable for low-cost color monitor applications. The LM2476 operates with 85V and 8V power supplies. The part is housed in the 19-lead TO-247 molded plastic power package. The pinout and internal connection diagram is shown in *Figure 1*.

The CRT Driver circuit diagram is shown in *Figure 1*. The PNP emitter follower, Q5, provides input buffering. Q1 and Q2 form a fixed gain cascode amplifier with resistors R1 and R2 setting the gain at –27. Emitter followers Q3 and Q4 isolate the high output impedance of the cascode stage from the capacitance of the CRT cathode which decreases the sensitivity of the device to load capacitance. Q6 provides biasing to the output emitter follower stage to reduce crossover distortion at low signal levels. The typical driver DC transfer function is shown in *Figure 5*.

The Bias Clamp circuit diagram is shown in *Figure 3*. The clamp circuit amplifies the DC inputs, V_{INC}, by the internally fixed gain of –16.5. Each clamp output, V_{OUTC}, will require a pull-up resistor to V_{CC}. The typical clamp DC transfer function is shown in *Figure 6*.

Application Hints

INTRODUCTION

National Semiconductor (NSC) is committed to provide application information that assists our customers in obtaining the best performance possible from our products. The following information is provided in order to support this commitment. The reader should be aware that the optimization of performance was done using a specific printed circuit board designed at NSC. Variations in performance can be realized due to physical changes in the printed circuit board and the application. Therefore, the designer should know that component value changes may be required in order to optimize performance in a given application. The values shown in this document can be used as a starting point for evaluation purposes. When working with high bandwidth circuits, good layout practices are also critical to achieving maximum performance.

IMPORTANT INFORMATION

The LM2476 performance is targeted for the VGA (640 x 480) to XGA (1024 x 768, 85Hz) resolution market. The application circuits shown in this document to optimize performance and to protect against damage from CRT arcover are designed specifically for the LM2476. If another member of the NSC CRT Driver or Bias Clamp family is used, please refer to its data sheet.

POWER SUPPLY BYPASS

Since the LM2476 contains wide bandwidth video amplifiers, proper power supply bypassing is critical for optimum performance. Improper power supply bypassing can result in large overshoot, ringing or oscillation. 0.1 µF capacitors should be connected from the supply pins, V_{CC} and V_{BB}, to ground, as close to the LM2476 as is practical. Additionally, a 47 µF or larger electrolytic capacitor should be connected from both supply pins to ground reasonably close to the LM2476. For optimal supply bypassing, the bypass capacitors should have the shortest connections between the supply and ground pins of the LM2476.

ARC PROTECTION

During normal CRT operation, internal arcing may occasionally occur. A spark gap SG1 – in the range of 200V – connected from each of the CRT cathodes to CRT ground will limit the maximum voltage, but to a value that is much higher than allowable on the LM2476. This fast, high voltage, high energy pulse can damage the LM2476 driver and/or clamp output stages. The application circuit shown in *Figure 12* is designed to help clamp the voltage at the outputs of the LM2476 to a safe level. The arc protection clamp diodes, D1 and D2, should have a fast transient response, high peak current rating, low series impedance and low shunt capacitance. FDH400 or equivalent diodes are recommended. Do not use 1N4148 diodes for the clamp diodes. D1 and D2 should have short, low impedance connections to V_{CC} and ground respectively. The cathode of D1 should be located very close to a separately decoupled bypass capacitor (C1 in *Figure 12*). The ground connection of D2 and the decoupling capacitor should be closest to the CRT ground. This will significantly reduce the high frequency voltage transients that the LM2476 would be subjected to during an arcover condition. Resistor R2 limits the arcover current that is seen by the diodes while R1 limits the current into the LM2476 as well as the voltage stress at the outputs of the device. R2 should be a ½W solid carbon type resistor. R1 can be a ¼W metal or carbon film type resistor. Having large value resistors for R1 and R2 would be desirable, but this has the effect of increasing rise and fall times. Inductor L1 is critical to reduce the initial high frequency voltage levels that the LM2476 would be subjected to. The inductor will not only help protect the device but it will also help minimize rise and fall times as well as minimize EMI. Current-limiting resistor R3 and bypass capacitor C2 should be placed very close to the clamp output pins to protect the LM2476 against damage during an arcover condition. The ground connection of C2 should have a short return path to CRT ground to shunt arcover currents away from the LM2476. For proper arc protection, it is important to not omit any of the arc protection components shown in *Figure 12*.

Application Hints (Continued)

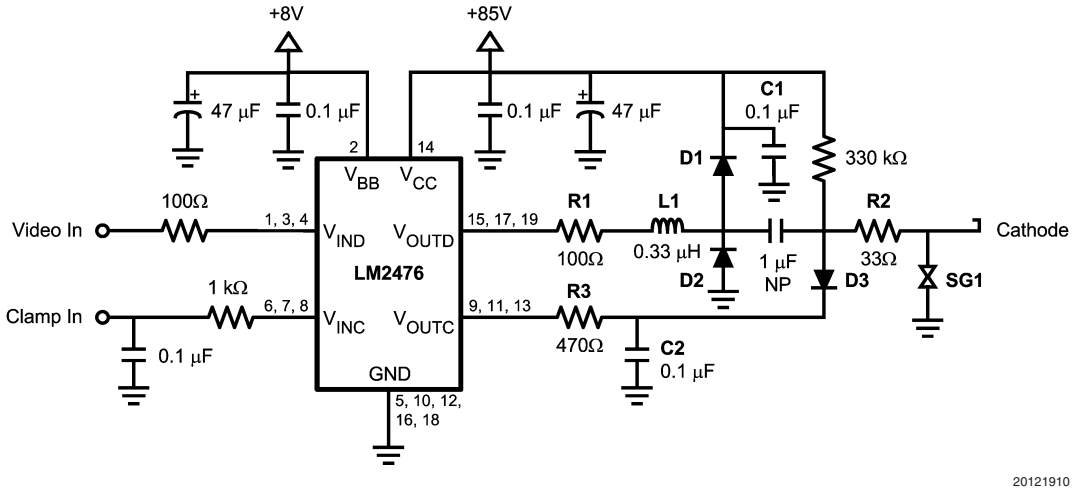


FIGURE 12. One Channel of the LM2476 with the Recommended Application Circuit

OPTIMIZING TRANSIENT RESPONSE

Referring to *Figure 12*, there are three components (R1, R2 and L1) that can be adjusted to optimize the transient response of the application circuit. Increasing the values of R1 and R2 will slow the circuit down while decreasing overshoot. Increasing the value of L1 will speed up the circuit as well as increase overshoot. It is very important to use inductors with very high self-resonant frequencies, preferably above 300 MHz. Ferrite core inductors from J.W. Miller Magnetics (part # 78FR--k) were used for optimizing the performance of the device in the NSC application board. The values shown in *Figure 14* can be used as a good starting point for the evaluation of the LM2476. Using a variable resistor for R1 will simplify finding the value needed for optimum performance in a given application. Once the optimum value is determined, the variable resistor can be replaced with a fixed value.

EFFECT OF OFFSET

Figure 8 shows the variation in rise and fall times when the output offset of the device is varied from 50 to 60VDC. The rise time shows a maximum variation of 13% relative to the center data point (55 V_{DC}). The fall time shows a maximum variation of less than 3% relative to the center data point.

EFFECT OF LOAD CAPACITANCE

Figure 9 shows the effect of increased load capacitance on the speed of the device. This demonstrates the importance of knowing the load capacitance in the application.

THERMAL CONSIDERATIONS

Figure 10 shows the performance of the LM2476 in the test circuit shown in *Figure 4* as a function of case temperature (on the device tab). The figure shows that the rise and fall times of the LM2476 increase by approximately 10% and 5%, respectively, as the case temperature increases from 50˚C to 100˚C. This corresponds to a speed degradation of 2% and 1%, respectively, for every 10˚C rise in case temperature.

Figure 11 shows the maximum power dissipation of the LM2476 vs. Frequency when all three channels of the device are driving an 8 pF load with a 40 V_{P-P} alternating one pixel on, one pixel off signal. The graph assumes a 72% active time (device operating at the specified frequency) which is typical in a monitor application. The other 28% of the time the device is assumed to be sitting at the black level (75V in this case). This graph gives the designer the information needed to determine the heat sink requirement for his application. The designer should note that if the load capacitance is increased the AC component of the total power dissipation will also increase.

The LM2476 case temperature must be maintained below 100˚C. If the maximum expected ambient temperature is 70˚C and the maximum power dissipation is about 6W (from *Figure 11*, 95 MHz bandwidth), then a maximum heat sink thermal resistance can be calculated:

$$R_{TH} = \frac{100°C - 70°C}{6W} = 5°C/W$$

PACKAGE MOUNTING CONSIDERATIONS

Mounting of the TO-247 package to a heat sink must be done such that there is sufficient pressure from the mounting screws to insure good contact with the heat sink for efficient heat flow. The surface of the heat sink should be free of contaminants before mounting to insure good contact. Incorrect mounting may lead to both thermal and mechanical problems. Over tightening the mounting screws will cause the package to warp, reducing contact area with the heat sink. Less contact with the heat sink will increase the thermal resistance from the package case to the heat sink (θ_{CS}) resulting in higher operating die temperatures. Extreme over tightening of the mounting screws will cause severe physical stress resulting in a cracked or chipped package and possible catastrophic IC failure.

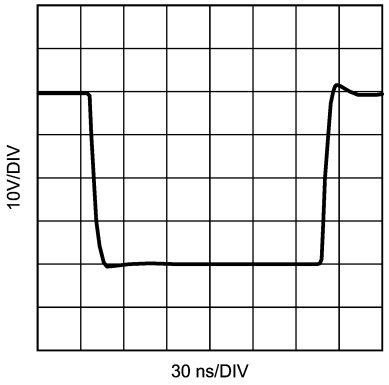
The recommended mounting screw size is M3 with a maximum torque of 50 N-cm. It is best to use fiber washers under the screws to distribute the force over a wider area. Additionally, if the mounting screws are used to force the package into correct alignment with the heat sink, package stress

Application Hints (Continued)

will be increased. This increase in package stress will result in reduced contact area with the heat sink increasing die operating temperature and possible catastrophic IC failure.

TYPICAL APPLICATION

A typical application of the LM2476 is shown in *Figure 14*. Used in conjunction with an LM123X/4X preamplfier, a complete video channel from monitor input to CRT cathode can be achieved. Performance is ideal for 1024 x 768 resolution displays with pixel clock frequencies up to 95 MHz. Please see the next two sections below for hints on how to properly evaluate the LM123X/4X and LM2476 combination in a monitor. *Figure 13* shows the typical cathode response for this application. The peaking component values used are shown in *Figure 12* and *Figure 14*.



$40V_{P-P}$ (35V – 75V)

FIGURE 13. Typical Cathode Response

PC BOARD LAYOUT CONSIDERATIONS

For optimum performance, use single-point grounds systems with adequate ground planes, isolate between channels, apply good supply bypassing, and minimize unwanted feedback and parasitic capacitance. Also, the length of the video signal traces from the preamplifier to the LM2476 and from the LM2476 to the CRT cathodes should be as short as possible. The following references are recommended:

Ott, Henry W., "Noise Reduction Techniques in Electronic Systems", John Wiley & Sons, New York, 1976.

"Video Amplifier Design for Computer Monitors", National Semiconductor Application Note 1013.

Pease, Robert A., "Troubleshooting Analog Circuits", Butterworth-Heinemann, 1991.

Because of its high small signal bandwidth, the part may oscillate in a monitor if feedback occurs around the video channel through the chassis wiring. To prevent this, leads to the video amplifier input circuit should be shielded, and input circuit wiring should be spaced as far as possible from output circuit wiring.

NSC DEMONSTRATION BOARD

Figure 14 is the schematic for the NSC LM1276/3X/4X_2476 Demonstration PCB that can be used to evaluate the LM1276, LM123X, or LM124X preamp with the LM2476 in a monitor. *Figure 15* shows the routing and component placement on the NSC Demonstration PCB. This board provides a good example of a layout that can be used as a guide for future layouts. Note the location of the following components:

- C26 — V_{CC} bypass capacitor, located very close to Pin 14 and GND Pins
- C27 — V_{BB} bypass capacitors, located close to Pin 2 and GND Pins
- C28, C30, C33 — V_{CC} bypass capacitors, near LM2476 and V_{CC} clamp diodes. These are very important for arc protection.

The routing of the LM2476 driver outputs to the CRT is very critical to achieving optimum performance. *Figure 16* shows the routing and component placement from Pin 17 of the LM2476 to the Red cathode. Note that the components are placed so that they almost line up from the output pin of the LM2476 to the Red cathode pin of the CRT connector. This is done to minimize the length of the video path between these two components for optimal performance and to minimize EMI. Note also that L4, D9, D13 and R23, R19, D10 are placed to minimize the size of the video nodes that they are attached to. This minimizes parasitic capacitance in the video path and also enhances the effectiveness of the protection diodes. The anode of protection diode D13 is connected directly to a section of the ground trace that has a short and direct path to CRT ground to shunt arcover current away from the LM2476. The cathode of D9 is connected to V_{CC} very close to decoupling capacitor C30 (see *Figure 16*) which is connected to the same section of the ground trace as D13. The diode placement and routing is very important for minimizing the voltage stress on the LM2476 during an arcover event. R37 and C29 are placed very close to the clamp output on Pin 11. These components will help limit the current and voltage stress to the clamp output. Lastly, notice that S2 is placed very close to the Red cathode and is connected directly to CRT ground.

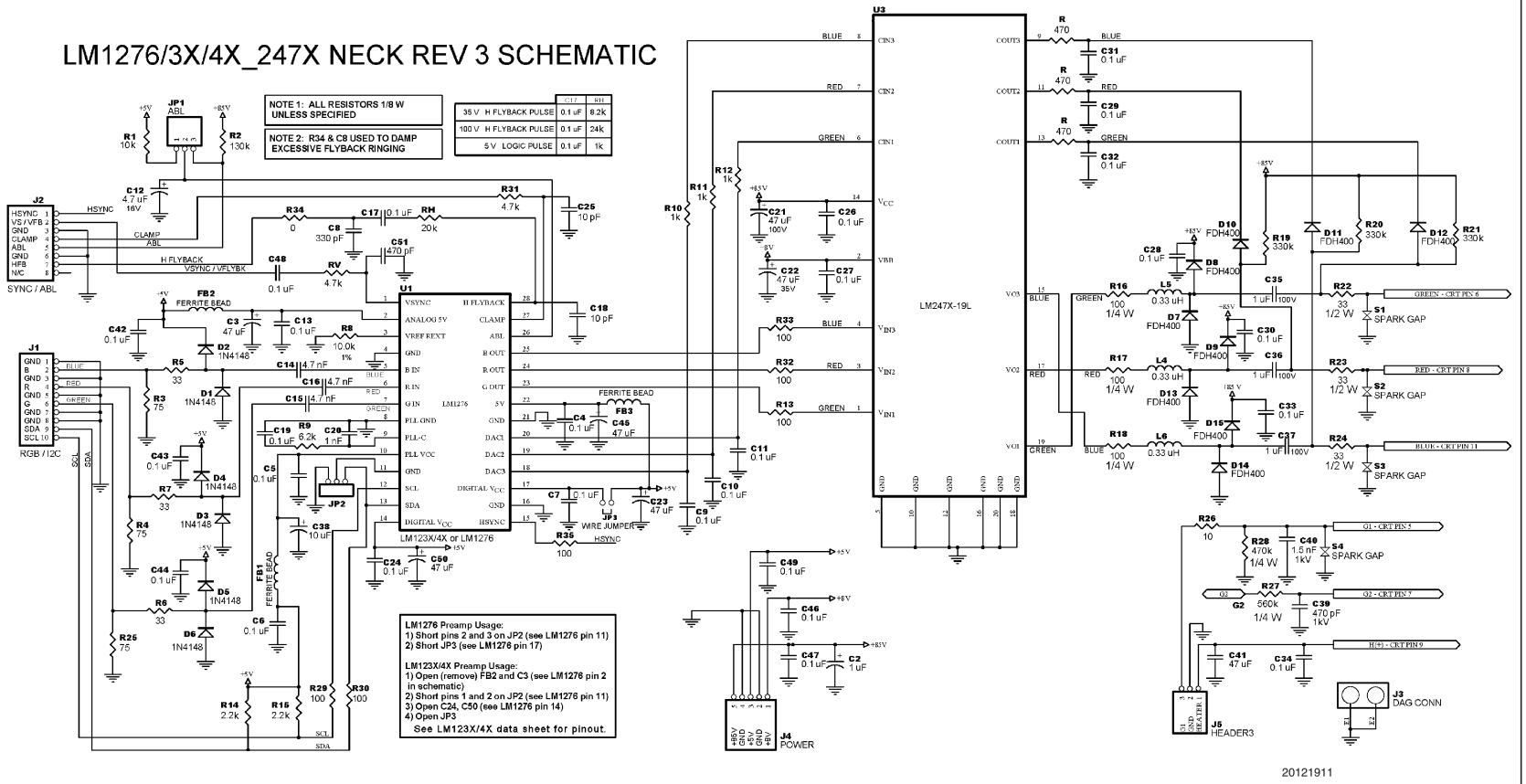


FIGURE 14. NSC Demonstration PCB Schematic

Application Hints (Continued)

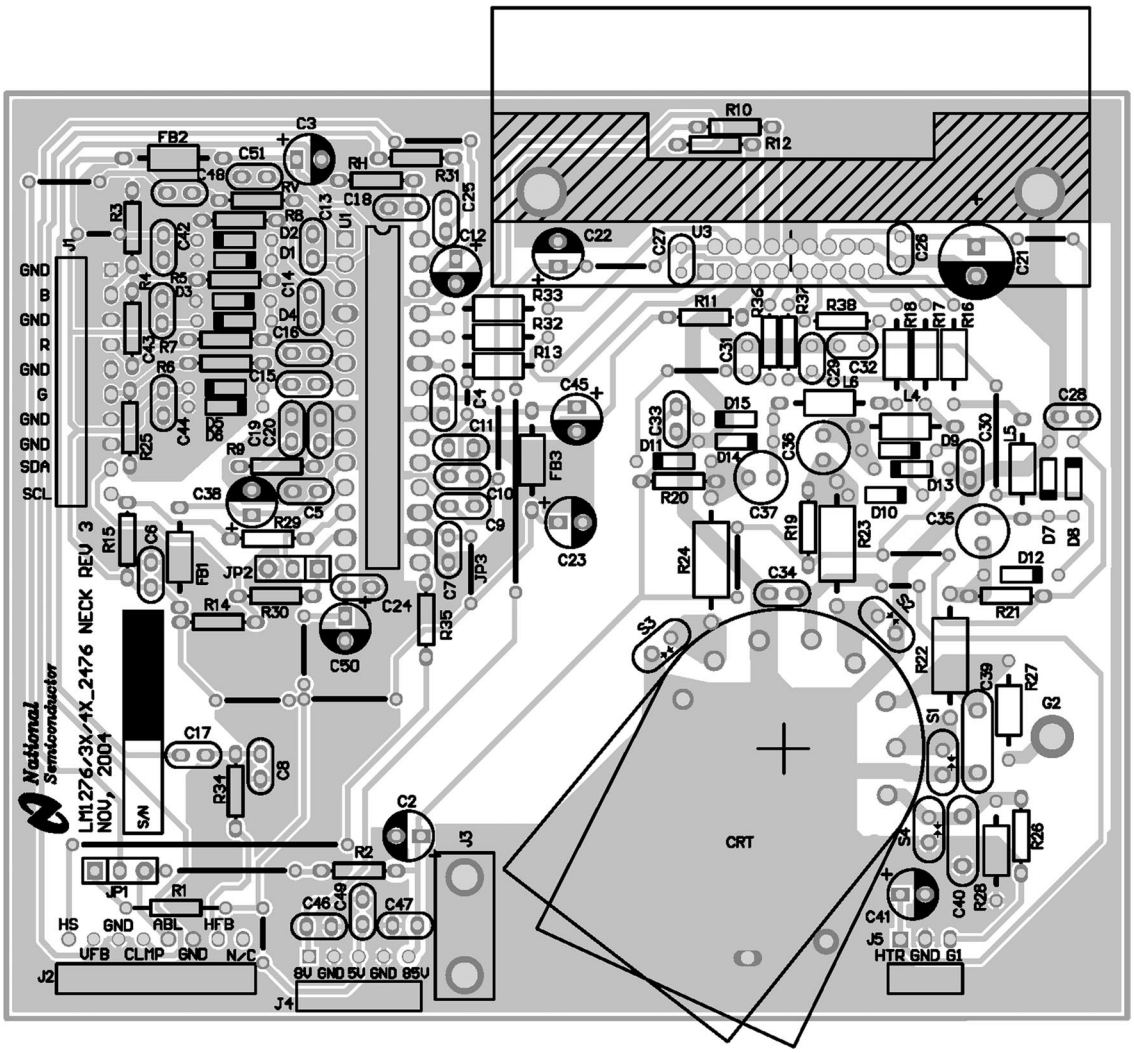


FIGURE 15. NSC Demonstration PCB Layout

Application Hints (Continued)

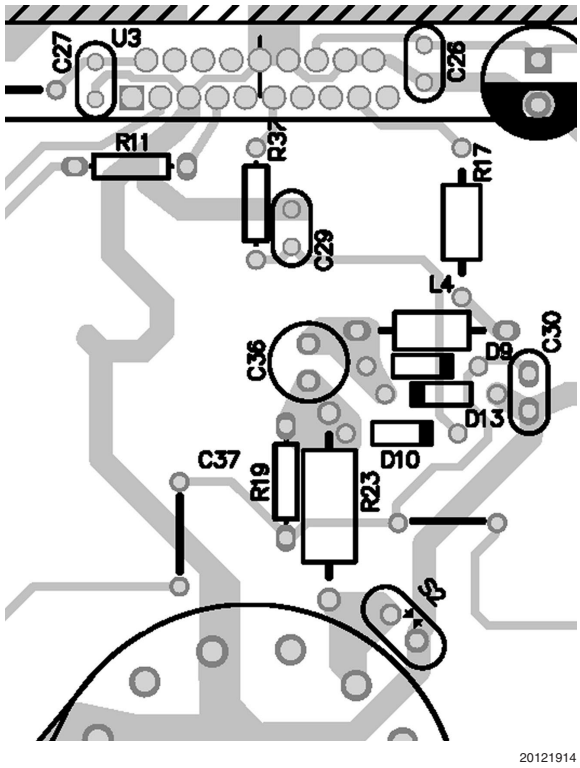
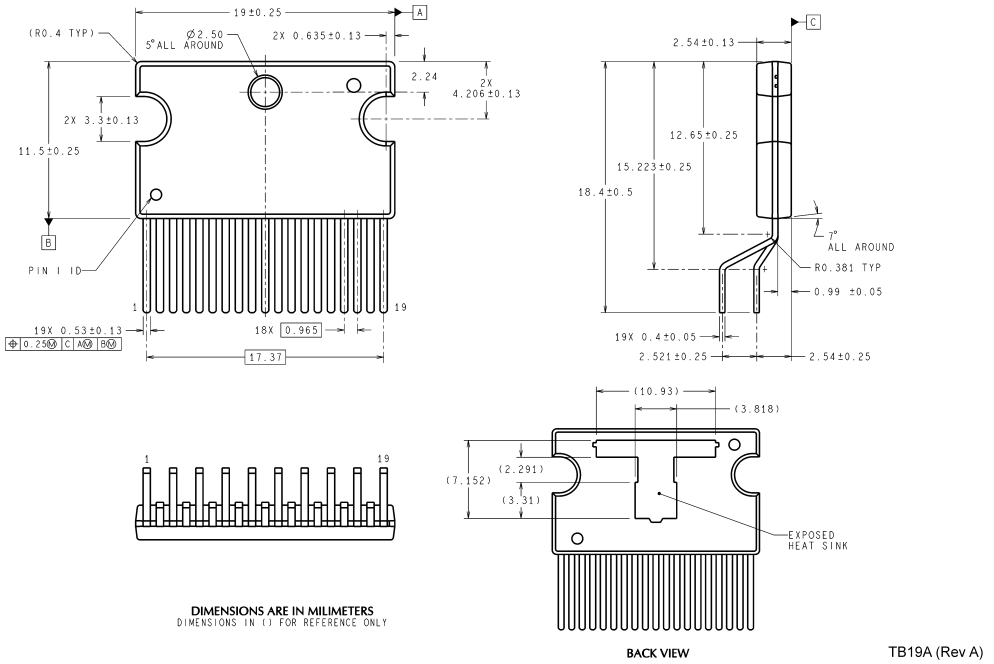


FIGURE 16. Trace Routing and Component Placement for Red Channel Output

Physical Dimensions inches (millimeters) unless otherwise noted



TB19A (Rev A)

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