National Semiconductor

May 2005

LM111JAN
Voltage Comparator

General Description

The LM111 is a voltage comparator that has input currents nearly a thousand times lower than devices such as the LM106 or LM710. It is also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. The output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, it can drive lamps or relays, switching voltages up to 50V at currents as high as 50 mA.

Both the inputs and the outputs of the LM111 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM106 and LM710 (200 ns response time vs 40 ns) the device is also much less prone to spurious oscillations. The LM111 has the same pin configuration as the LM106 and LM710.

Features

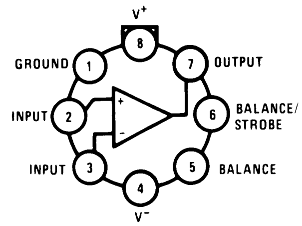
- Operates from single 5V supply
- Input current: 200 nA max. over temperature
- Offset current: 20 nA max. over temperature
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V
- Power supply voltage, single 5V to ±15V
- Offset voltage null capability
- Strobe capability

Ordering Information

NS PART NUMBER	SMD PART NUMBER	NS PACKAGE NUMBER	PACKAGE DESCRIPTION
JL111BCA	JM38510/10304BCA	J14A	14LD CERDIP
JL111BGA	JM38510/10304BGA	H08C	8LD TO-99 Metal Can
JL111BHA	JM38510/10304BHA	W10A	10LD CERPACK
JL111BPA	JM38510/10304BPA	J08A	8LD CERDIP
JL111SGA	JM38510/10304SGA	H08C	8LD TO-99 Metal Can
JL111SHA	JM38510/10304SHA	W10A	10LD CERPACK
JL111SPA	JM38510/10304SPA	J08A	8LD CERDIP
JL111SZA	JM38510/10304SZA	WG10A	10LD Ceramic SOIC

Connection Diagrams

Metal Can Package



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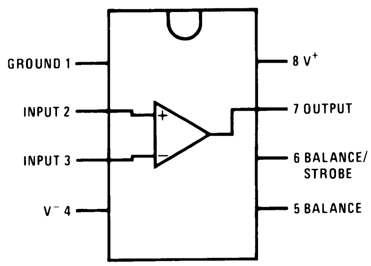
Note: Pin 4 connected to case

Top View
See NS Package Number H08C

Dual-In-Line Package



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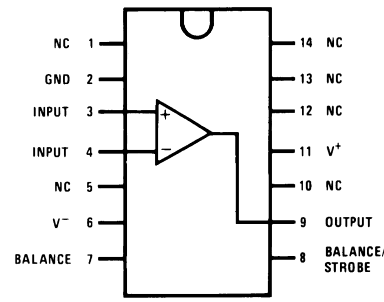
Top View
See NS Package Number J08A

Dual-In-Line Package



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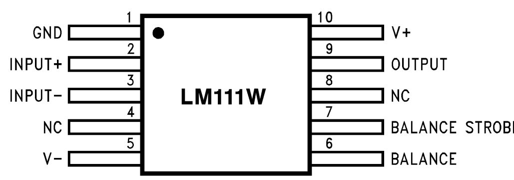
Top View
See NS Package Number J14A



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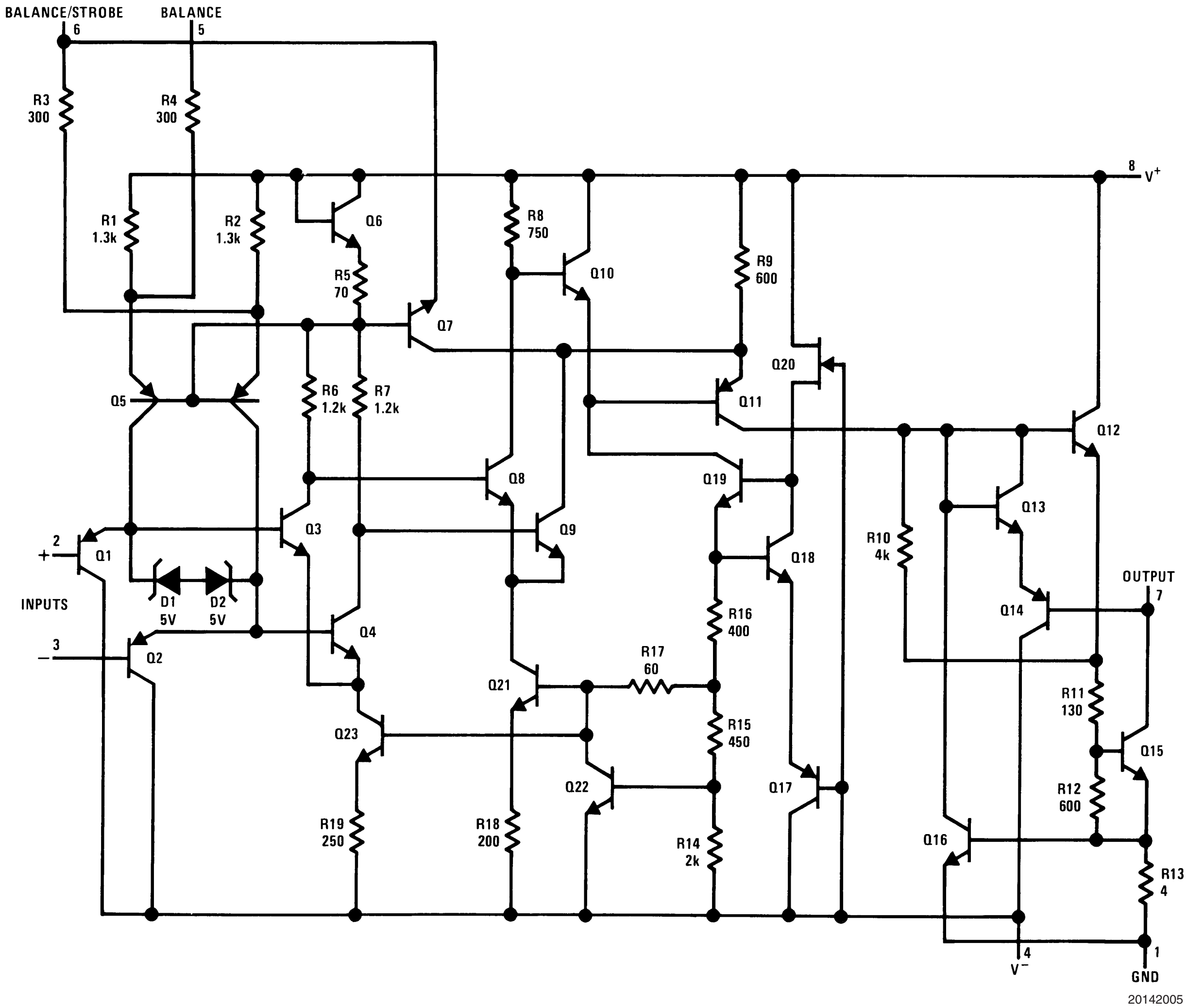
See NS Package Number W10A, WG10A

Schematic Diagram (Note 1)



Note 1: Pin connections shown on schematic diagram are for H08 package.

Absolute Maximum Ratings (Note 2)

Positive Supply Voltage	+30.0V
Negative Supply Voltage	-30.0V
Total Supply Voltage	36V
Output to Negative Supply Voltage	50V
GND to Negative Supply Voltage	30V
Differential Input Voltage	±30V
Sink Current	50mA
Input Voltage (Note 3)	±15V
Power Dissipation (Note 4)	
8 LD CERDIP	400mW @ 25˚C
8 LD Metal Can	330mW @ 25˚C
10 LD CERPACK	330mW @ 25˚C
10 LD Ceramic SOIC	330mW @ 25˚C
14 LD CERDIP	400mW @ 25˚C
Output Short Circuit Duration	10 seconds
Maximum Strobe Current	10mA
Operating Temperature Range	-55˚C ≤ T_A ≤ 125˚C
Thermal Resistance	
θ_{JA}	
8 LD CERDIP (Still Air @ 0.5W)	120˚C/W
8 LD CERDIP (500LF/Min Air flow @ 0.5W)	76˚C/W
8 LD Metal Can (Still Air @ 0.5W)	150˚C/W
8 LD Metal Can (500LF/Min Air flow @ 0.5W)	92˚C/W
10 Ceramic SOIC (Still Air @ 0.5W)	231˚C/W
10 Ceramic SOIC (500LF/Min Air flow @ 0.5W)	153˚C/W
10 CERPACK (Still Air @ 0.5W)	231˚C/W
10 CERPACK (500LF/Min Air flow @ 0.5W)	153˚C/W
14 LD CERDIP (Still Air @ 0.5W)	120˚C/W
14 LD CERDIP (500LF/Min Air flow @ 0.5W)	65˚C/W
θ_{JC}	
8 LD CERDIP	35˚C/W
8 LD Metal Can Pkg	40˚C/W
10 LD Ceramic SOIC	60˚C/W
10 LD CERPACK	60˚C/W
14 LD CERDIP	35˚C/W
Storage Temperature Range	-65˚C ≤ T_A ≤ 150˚C
Maximum Junction Temperature	175˚C
Lead Temperature (Soldering, 60 seconds)	300˚C
Voltage at Strobe Pin	V^+ -5V
Package Weight (Typical)	
8 LD Metal Can	965mg
8 LD CERDIP	1100mg
10 LD CERPACK	250mg
10 LD Ceramic SOIC	225mg
14 LD CERDIP	TBD
ESD Rating (Note 5)	300V

Recommended Operating Conditions

Supply Voltage	$V_{CC} = \pm 15V_{DC}$
Operating Temperature Range	$-55^\circ C \le T_A \le 125^\circ C$

Quality Conformance Inspection

Mil-Std-883, Method 5005 — Group A

Subgroup	Description	Temperature (˚C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

LM111 JAN Electrical Characteristics

DC Parameters

The following conditions apply, unless otherwise specified.

DC: V_{CC} = ±15V, V_{CM} = 0

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	V_I = 0V, R_S = 50Ω		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50Ω		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50Ω		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
		$+V_{CC}$ = +2.5V, $-V_{CC}$ = -2.5V, V_I = 0V, R_S = 50Ω		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
V_{IO} R	Raised Input Offset Voltage	V_I = 0V, R_S = 50Ω		-3.0	+3.0	mV	1
				-4.5	+4.5	mV	2, 3
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50Ω		-3.0	+3.0	mV	1
				-4.5	+4.5	mV	2, 3
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50Ω		-3.0	+3.0	mV	1
				-4.5	+4.5	mV	2, 3
I_{IO}	Input Offset Current	V_I = 0V, R_S = 50KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
$I_{IO}R$	Raised Input Offset Current	V_I = 0V, R_S = 50KΩ		-25	+25	nA	1, 2
				-50	+50	nA	3
$\pm I_{IB}$	Input Bias Current	V_I = 0V, R_S = 50KΩ		-100	0.1	nA	1, 2
				-150	0.1	nA	3
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50KΩ		-150	0.1	nA	1, 2
				-200	0.1	nA	3
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50KΩ		-150	0.1	nA	1, 2
				-200	0.1	nA	3
V_OSt	Collector Output Voltage (Strobe)	$+V_I$ = Gnd, $-V_I$ = 15V, I_{St} = -3mA, R_S = 50Ω	(Note 7)	14		V	1, 2, 3
CMRR	Common Mode Rejection	-28V ≤ $-V_{CC}$ ≤ -0.5V, R_S=50Ω, 2V ≤ $+V_{CC}$ ≤ 29.5V, R_S = 50Ω, -14.5V ≤ V_{CM} ≤ 13V,R_S = 50Ω		80		dB	1, 2, 3

LM111 JAN Electrical Characteristics (Continued)

DC Parameters (Continued)

The following conditions apply, unless otherwise specified.

DC: V_{CC} = ±15V, V_{CM} = 0

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{OL}	Low Level Output Voltage	$+V_{CC}$ = 4.5V, $-V_{CC}$ = Gnd, I_O = 8mA, $\pm V_I$ = 0.5V, V_{ID} = -6mV	(Note 9)		0.4	V	1, 2, 3
		$+V_{CC}$ = 4.5V, $-V_{CC}$ = Gnd, I_O = 8mA, $\pm V_I$ = 3V, V_{ID} = -6mV	(Note 9)		0.4	V	1, 2, 3
		I_O = 50mA, ±VI = 13V, V_{ID} = -5mV	(Note 9)		1.5	V	1, 2, 3
		I_O = 50mA, ±VI = -14V, V_{ID} = -5mV	(Note 9)		1.5	V	1, 2, 3
I_{CEX}	Output Leakage Current	$+V_{CC}$ = 18V, $-V_{CC}$ = -18V, V_O = 32V		-1.0	10	nA	1
				-1.0	500	nA	2
I_{IL}	Input Leakage Current	$+V_{CC}$ = 18V, $-V_{CC}$ = -18V, $+V_I$ = +12V, $-V_I$ = -17V		-5.0	500	nA	1, 2, 3
		$+V_{CC}$ = 18V, $-V_{CC}$ = -18V, $+V_I$ = -17V, $-V_I$ = +12V		-5.0	500	nA	1, 2, 3
$+I_{CC}$	Power Supply Current				6.0	mA	1, 2
					7.0	mA	3
$-I_{CC}$	Power Supply Current			-5.0		mA	1, 2
				-6.0		mA	3
$\Delta V_{IO} / \Delta T$	Temperature Coefficient Input Offset Voltage	25˚C ≤ T ≤ 125˚C	(Note 8)	-25	25	uV/˚C	2
		-55˚C ≤ T ≤ 25˚C	(Note 8)	-25	25	uV/˚C	3
$\Delta I_{IO} / \Delta T$	Temperature Coefficient Input Offset Current	25˚C ≤ T ≤ 125˚C	(Note 8)	-100	100	pA/˚C	2
		-55˚C ≤ T ≤ 25˚C	(Note 8)	-200	200	pA/˚C	3
I_{OS}	Short Circuit Current	V_O = 5V, t ≤ 10mS, $-V_I$ = 0.1V, $+V_I$ = 0V			200	mA	1
					150	mA	2
					250	mA	3
$+V_{IO}$ adj.	Input Offset Voltage (Adjustment)	V_O = 0V, V_I = 0V, R_S = 50Ω		5.0		mV	1
$-V_{IO}$ adj.	Input Offset Voltage (Adjustment)	V_O = 0V, V_I = 0V, R_S = 50Ω			-5.0	mV	1
$\pm A_{VE}$	Voltage Gain (Emitter)	R_L = 600Ω	(Note 6)	10		V/mV	4
			(Note 6)	8.0		V/mV	5, 6

AC Parameters

The following conditions apply, unless otherwise specified.

AC: V_{CC} = ±15V, V_{CM} = 0

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
tR_{LHC}	Response Time (Collector Output)	V_{OD}(Overdrive) = -5mV, C_L = 50pF, V_I = -100mV			300	nS	7, 8B
					640	nS	8A
tR_{HLC}	Response Time (Collector Output)	V_{OD}(Overdrive) = 5mV, C_L = 50pF, V_I = 100mV			300	nS	7, 8B
					500	nS	8A

LM111 JAN Electrical Characteristics (Continued)

DC Drift Parameters

The following conditions apply, unless otherwise specified.

DC: V_{CC} = ±15V, V_{CM} = 0

Delta calculations performed on JANS devices at group B , subgroup 5.

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	V_I = 0V, R_S = 50Ω		-0.5	0.5	mV	1
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50Ω		-0.5	0.5	mV	1
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50Ω		-0.5	0.5	mV	1
$\pm I_{IB}$	Input Bias Current	V_I = 0V, R_S = 50KΩ		-12.5	12.5	nA	1
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50KΩ		-12.5	12.5	nA	1
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50KΩ		-12.5	12.5	nA	1
I_{CEX}	Output Leakage Current	$+V_{CC}$ = 18V, $-V_{CC}$ = -18V, V_O = 32V		-5.0	5.0	nA	1

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: This rating applies for ±15V supplies. The positive input voltage limit is 30 V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 5: Human body model, 1.5 kΩ in series with 100 pF.

Note 6: Datalog reading in K=V/mV.

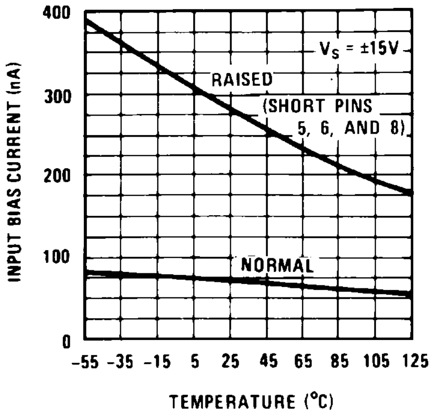
Note 7: I_{ST} = −2mA at −55˚C

Note 8: Calculated parameter.

Note 9: V_{ID} is voltage difference between inputs.

LM111 Typical Performance Characteristics

Input Bias Current



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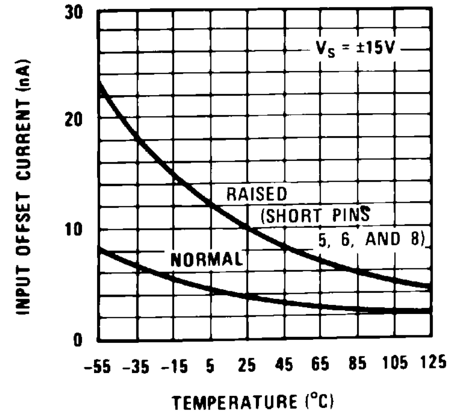
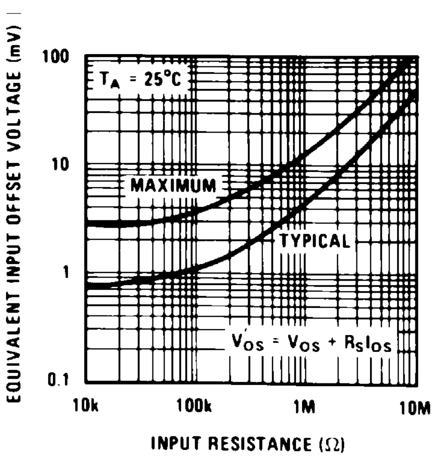
Input Bias Current



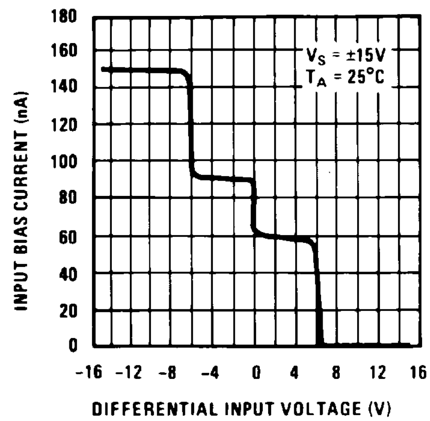
20142044

Input Bias Current



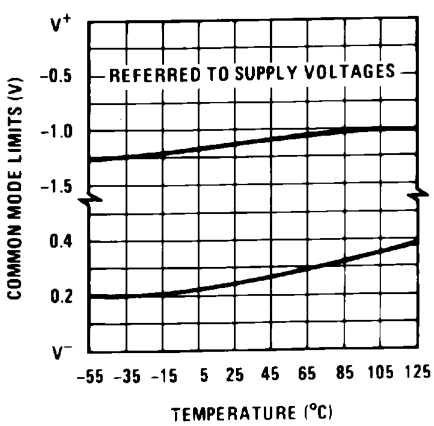
20142045

Input Bias Current



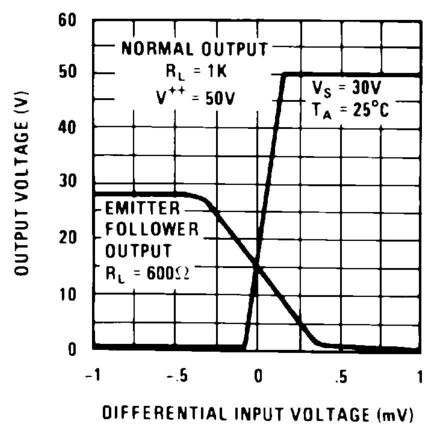
20142046

Input Bias Current



20142047

Input Bias Current



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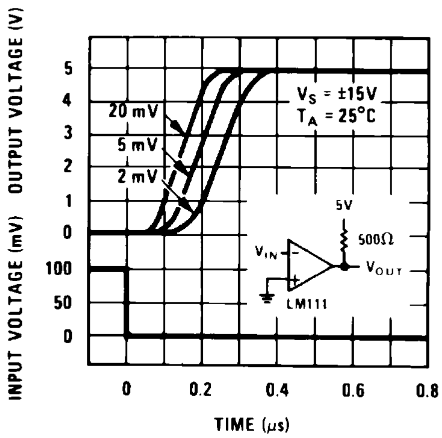
LM111 Typical Performance Characteristics (Continued)

Input Bias Current Input Overdrives



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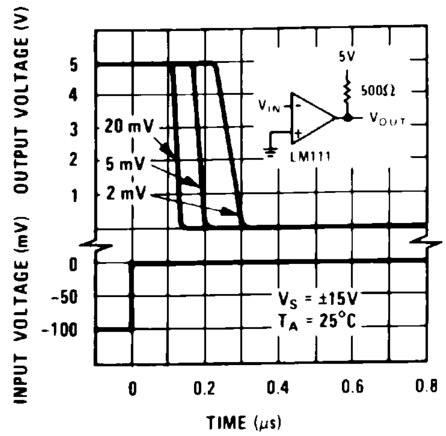
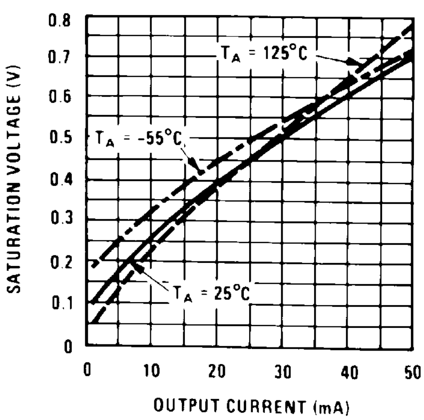
Input Bias Current Input Overdrives



20142050

Input Bias Current



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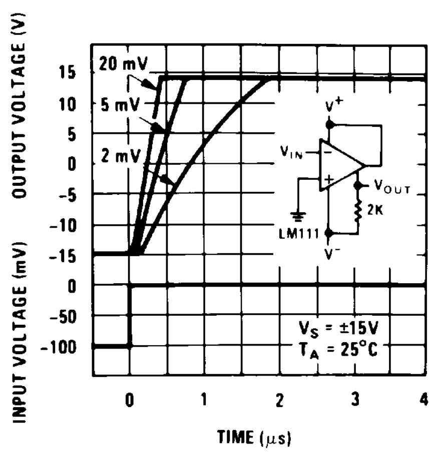
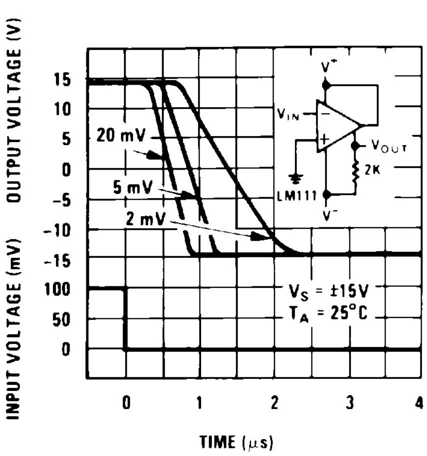
Response Time for Various Input Overdrives



20142052

Response Time for Various Input Overdrives



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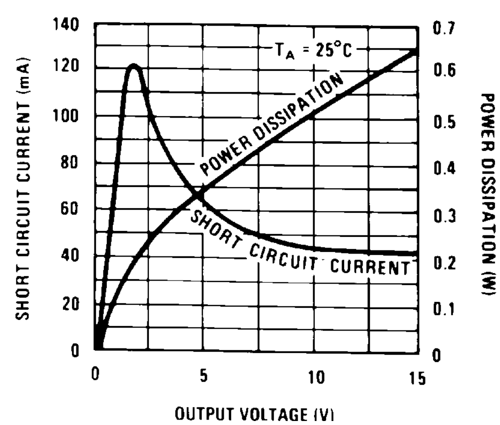
Output Limiting Characteristics



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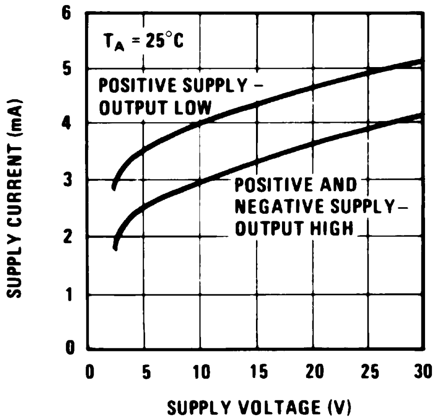
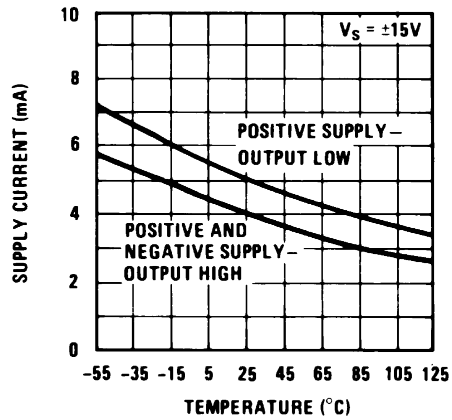
LM111 Typical Performance Characteristics (Continued)

Supply Current



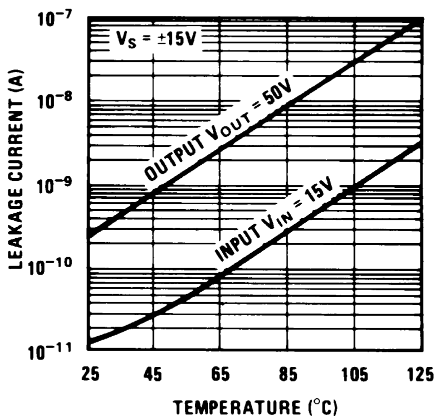
20142055

Supply Current



20142056

Leakage Currents



20142057

Application Hints

CIRCUIT TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

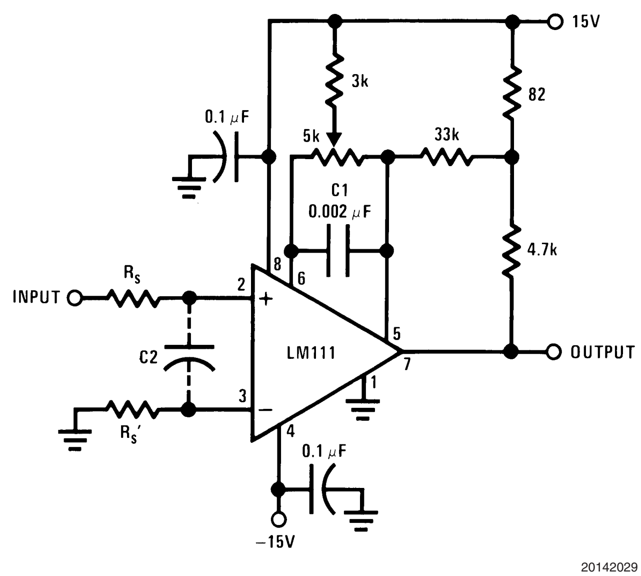
When a high-speed comparator such as the LM111 is used with fast input signals and low source impedances, the output response will normally be fast and stable, assuming that the power supplies have been bypassed (with 0.1 µF disc capacitors), and that the output signal is routed well away from the inputs (pins 2 and 3) and also away from pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1 kΩ to 100 kΩ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators such as the LM111. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in *Figure 1* below.

1. The trim pins (pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a 0.01 µF capacitor C1 between pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if pin 5 is used for positive feedback as in *Figure 1*.
2. Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor C2 is connected directly across the input pins.
3. When the signal source is applied through a resistive network, R_S, it is usually advantageous to choose an R_S' of substantially the same value, both for DC and for dynamic (AC) considerations. Carbon, tin-oxide, and metal-film resistors have all been used successfully in comparator input circuitry. Inductive wire wound resistors are not suitable.
4. When comparator circuits use input resistors (e.g. summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words there should be very little lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if R_S=10 kΩ, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to damp. Twisting these input leads tightly is the only (second best) alternative to placing resistors close to the comparator.

Application Hints (Continued)

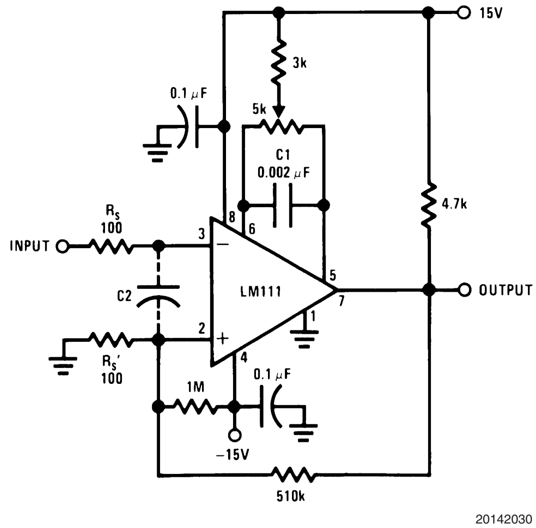
5. Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a ground plane under the LM111 circuitry, for example, one side of a double-layer circuit card. Ground foil (or, positive supply or negative supply foil) should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any high-level signals (such as the output). If pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located, at most, a few inches away from the LM111, and the 0.01 µF capacitor should be installed. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM111. (Some other comparators require the power-supply bypass to be located immediately adjacent to the comparator.)
6. It is a standard procedure to use hysteresis (positive feedback) around a comparator, to prevent oscillation, and to avoid excessive noise on the output because the comparator is a good amplifier for its own noise. In the circuit of *Figure 2*, the feedback from the output to the positive input will cause about 3 mV of hysteresis. However, if R_S is larger than 100Ω, such as 50 kΩ, it would not be reasonable to simply increase the value of the positive feedback resistor above 510 kΩ. The circuit of *Figure 3* could be used, but it is rather awkward. See the notes in paragraph 7 below.
7. When both inputs of the LM111 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM111 so that positive feedback would be disruptive, the circuit of *Figure 1* is ideal. The positive feedback is to pin 5 (one of the offset adjustment pins). It is sufficient to cause 1 to 2 mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz. The positive-feedback signal across the 82Ω resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at pin 5, so this feedback does not add to the V_{OS} of the comparator. As much as 8 mV of V_{OS} can be trimmed out, using the 5 kΩ pot and 3 kΩ resistor as shown.
8. These application notes apply specifically to the LM111 and LF111 families of comparators, and are applicable to all high-speed comparators in general, (with the exception that not all comparators have trim pins).



Pin connections shown are for LM111H in the H08 hermetic package

FIGURE 1. Improved Positive Feedback

Application Hints (Continued)



Pin connections shown are for LM111H in the H08 hermetic package

FIGURE 2. Conventional Positive Feedback

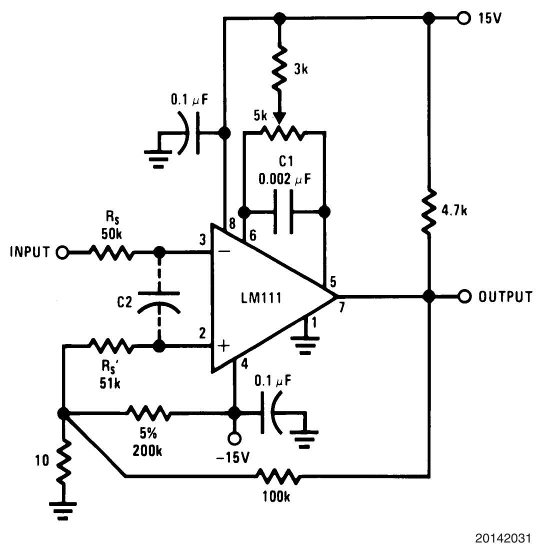
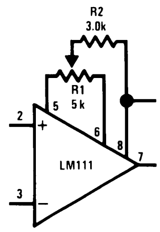


FIGURE 3. Positive Feedback with High Source Resistance

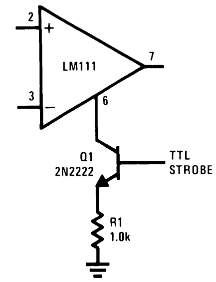
Typical Applications (Note 12)

Offset Balancing



20142036

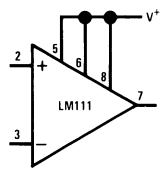
Strobing



20142037

Note: Do Not Ground Strobe Pin. Output is turned off when current is pulled from Strobe Pin.

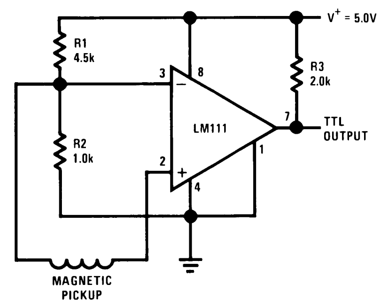
Increasing Input Stage Current (Note 10)



20142038

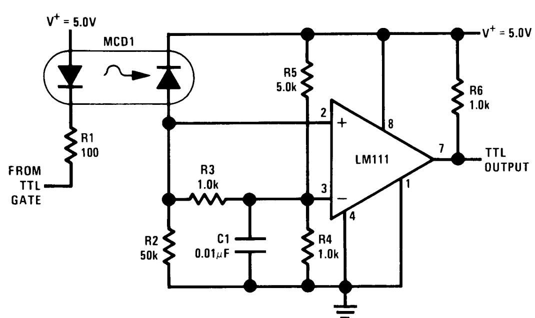
Note 10: Increases typical common mode slew from 7.0V/μs to 18V/μs.

Detector for Magnetic Transducer



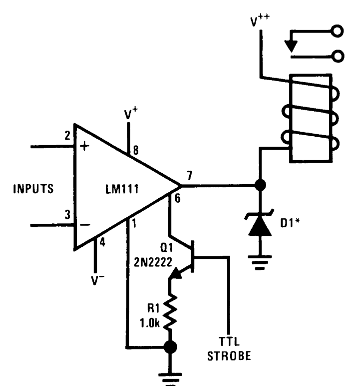
20142039

Digital Transmission Isolator



20142040

Relay Driver with Strobe



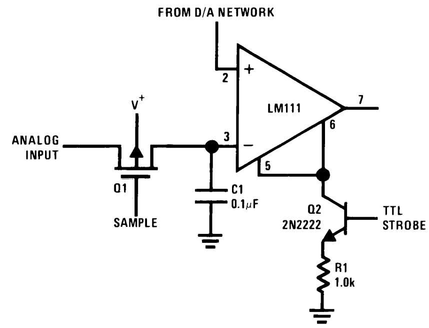
20142041

*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V^{++} line.

Note: Do Not Ground Strobe Pin.

Typical Applications (Note 12) (Continued)

Strobing off Both Input and Output Stages (Note 11)



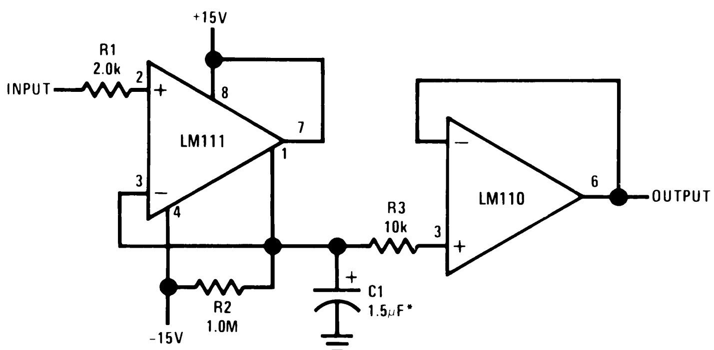
20142042

Note: Do Not Ground Strobe Pin.

Note 11: Typical input current is 50 pA with inputs strobed off.

Note 12: Pin connections shown on schematic diagram and typical applications are for H08 metal can package.

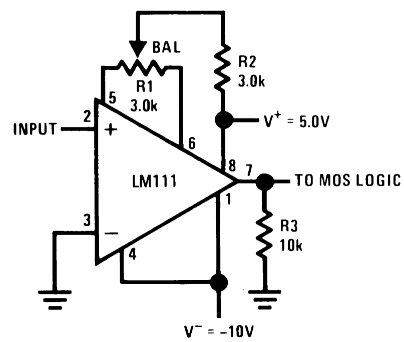
Positive Peak Detector



20142023

*Solid tantalum

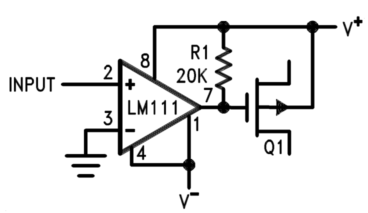
Zero Crossing Detector Driving MOS Logic



20142024

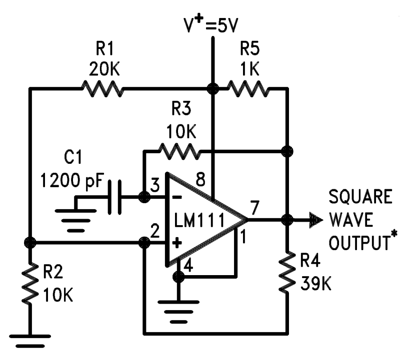
Typical Applications (Pin numbers refer to H08 package)

Zero Crossing Detector Driving MOS Switch



20142013

100 kHz Free Running Multivibrator

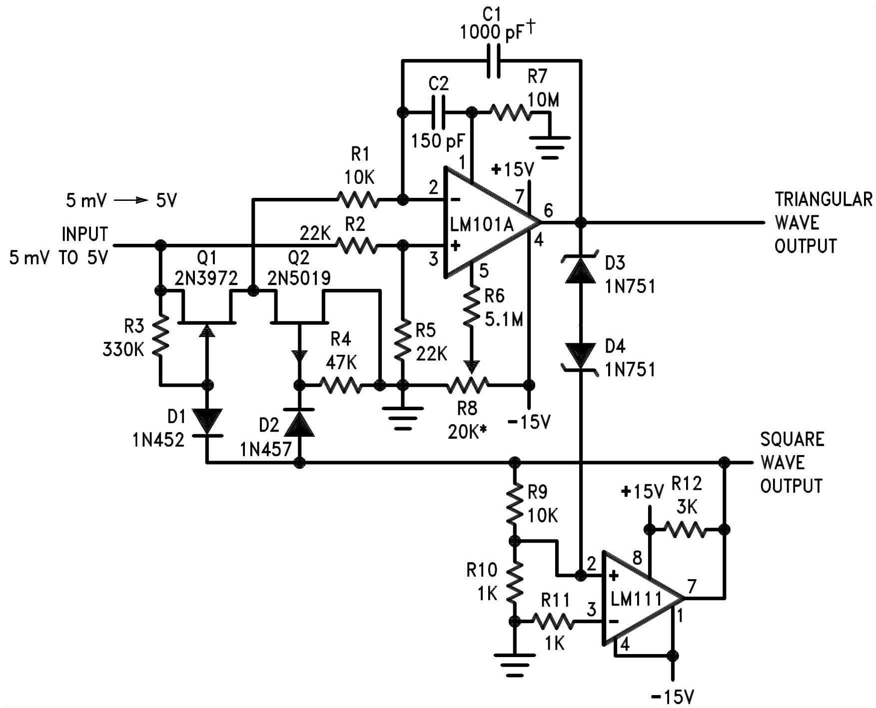


20142014

*TTL or DTL fanout of two

Typical Applications (Pin numbers refer to H08 package) (Continued)

10 Hz to 10 kHz Voltage Controlled Oscillator

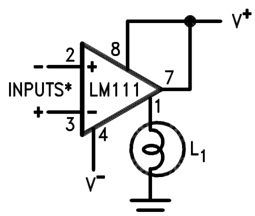


20142015

*Adjust for symmetrical square wave time when V_{IN} = 5 mV

†Minimum capacitance 20 pF Maximum frequency 50 kHz

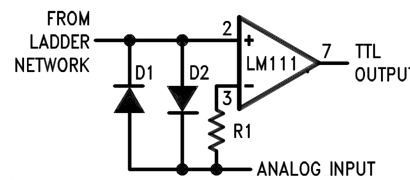
Driving Ground-Referred Load



20142016

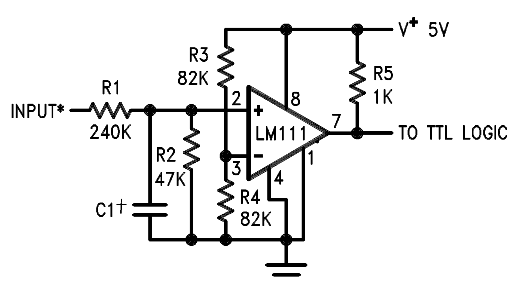
*Input polarity is reversed when using pin 1 as output.

Using Clamp Diodes to Improve Response



20142017

TTL Interface with High Level Logic



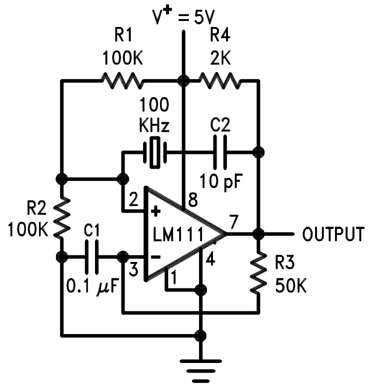
20142018

*Values shown are for a 0 to 30V logic swing and a 15V threshold.

†May be added to control speed and reduce susceptibility to noise spikes.

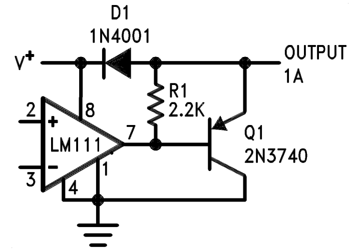
Typical Applications (Pin numbers refer to H08 package) (Continued)

Crystal Oscillator



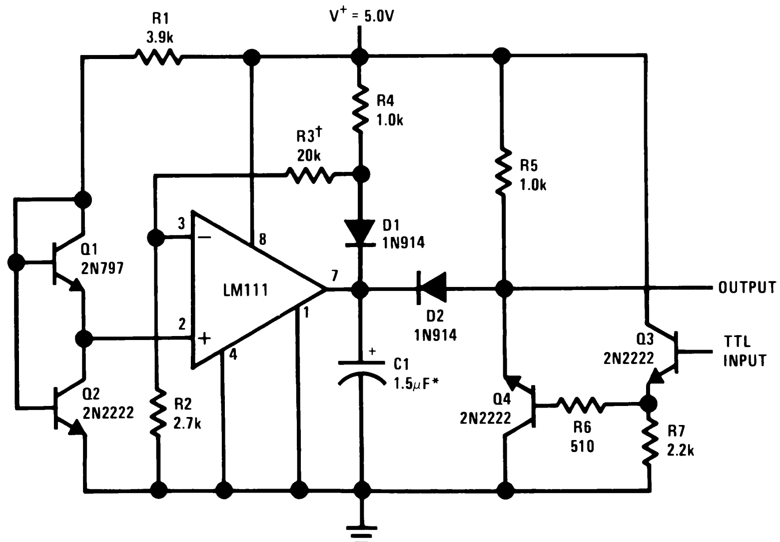
20142019

Comparator and Solenoid Driver



20142020

Precision Squarer



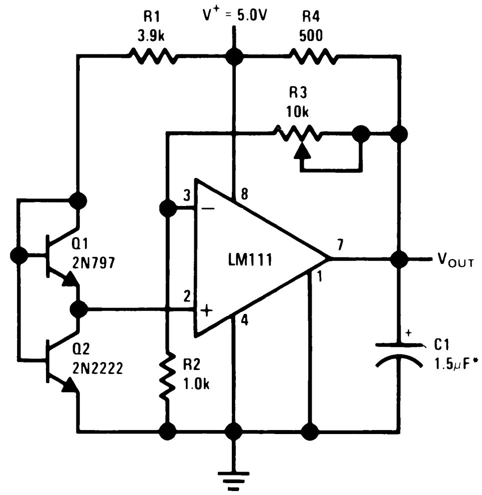
20142021

*Solid tantalum

†Adjust to set clamp level

Typical Applications (Pin numbers refer to H08 package) (Continued)

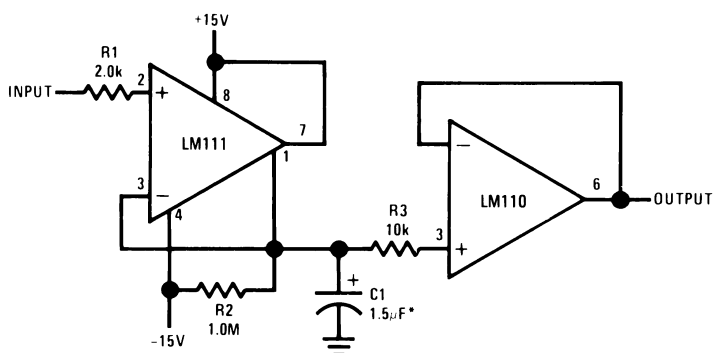
Low Voltage Adjustable Reference Supply



20142022

*Solid tantalum

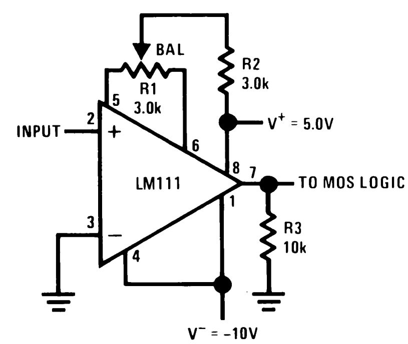
Positive Peak Detector



20142023

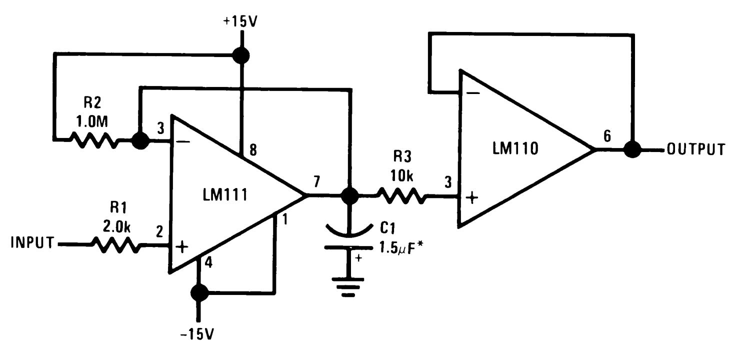
*Solid tantalum

Zero Crossing Detector Driving MOS Logic



20142024

Negative Peak Detector

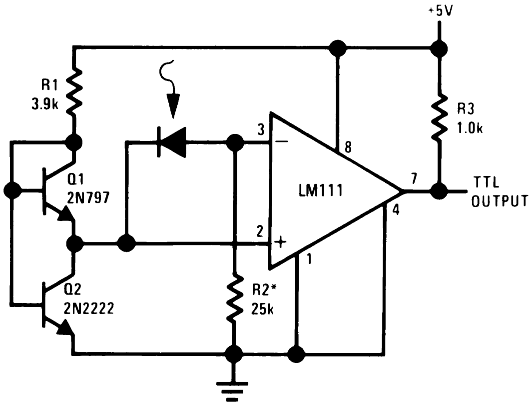


20142025

*Solid tantalum

Typical Applications (Pin numbers refer to H08 package) (Continued)

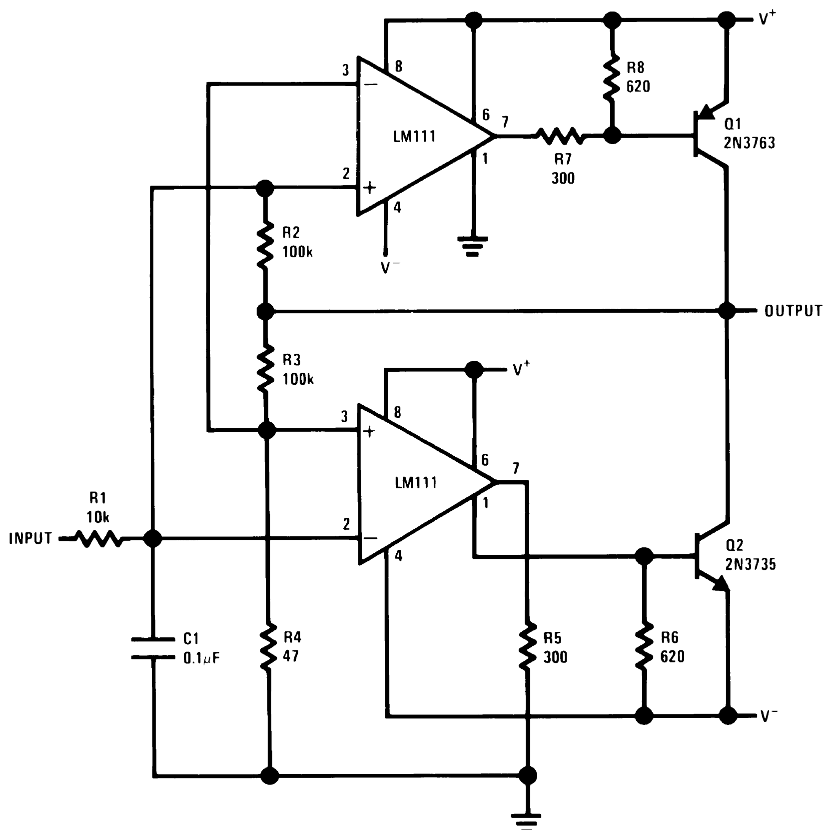
Precision Photodiode Comparator



20142026

*R2 sets the comparison level. At comparison, the photodiode has less than 5 mV across it, decreasing leakages by an order of magnitude.

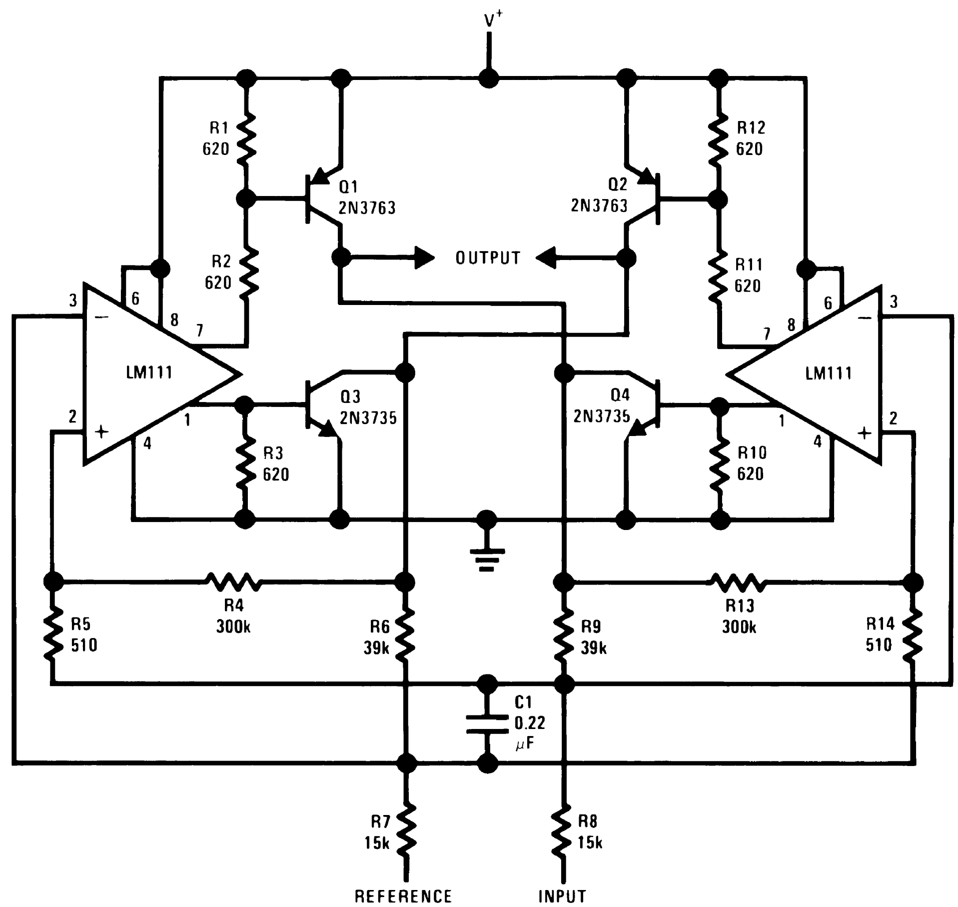
Switching Power Amplifier



20142027

Typical Applications (Pin numbers refer to H08 package) (Continued)

Switching Power Amplifier

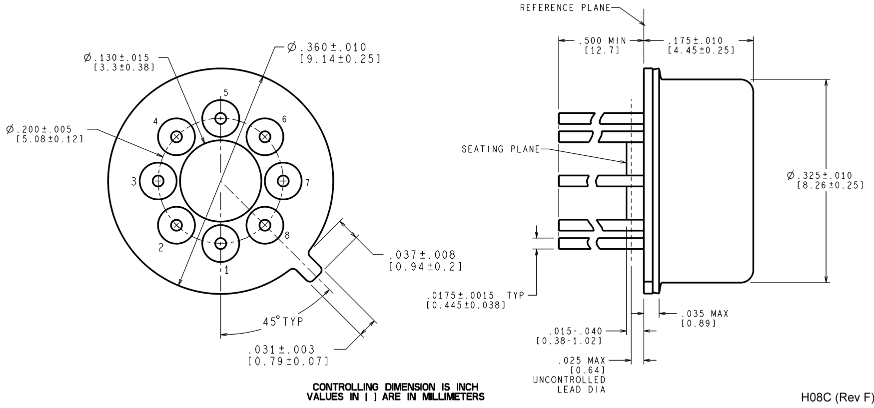


20142028

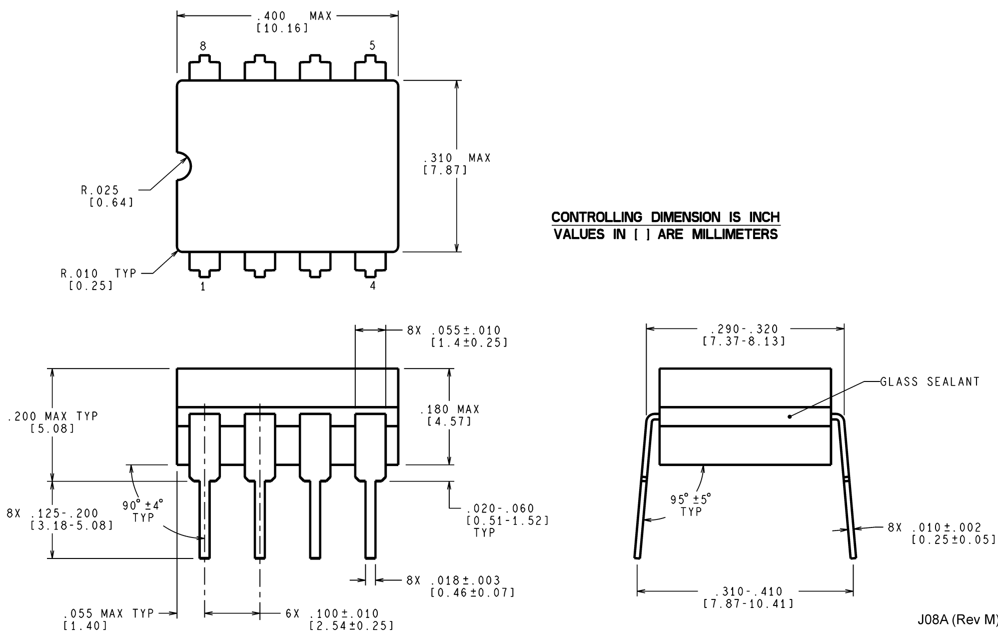
Revision History Section

Released	Revision	Section	Originator	Changes
05/09/05	A	New Release, Corporate format	L. Lytle	1 MDS data sheets converted into one Corp. data sheet format. MJLM111–X Rev 0D3 will be archived.

Physical Dimensions inches (millimeters) unless otherwise noted

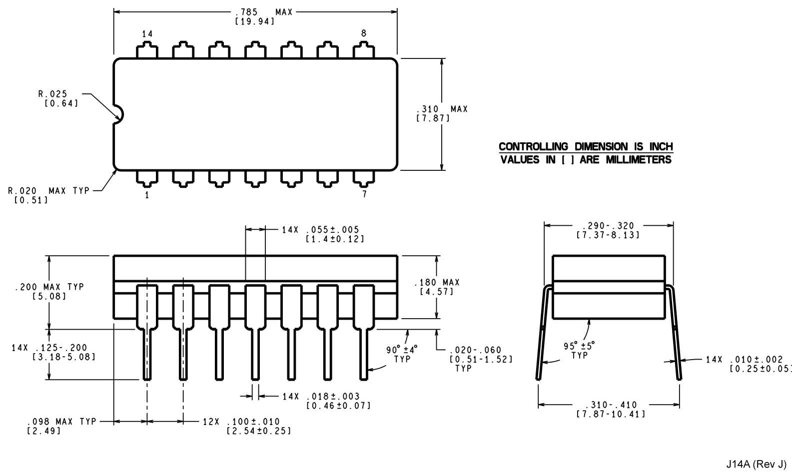


Metal Can Package (H)
NS Package Number H08C

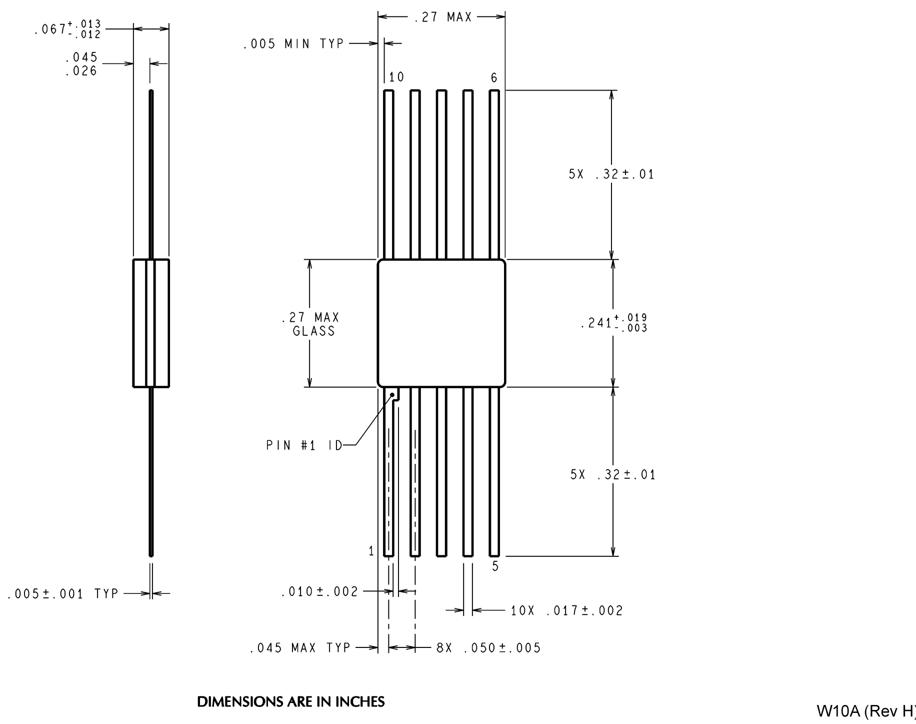


Cavity Dual-In-Line Package (J)
NS Package Number J08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

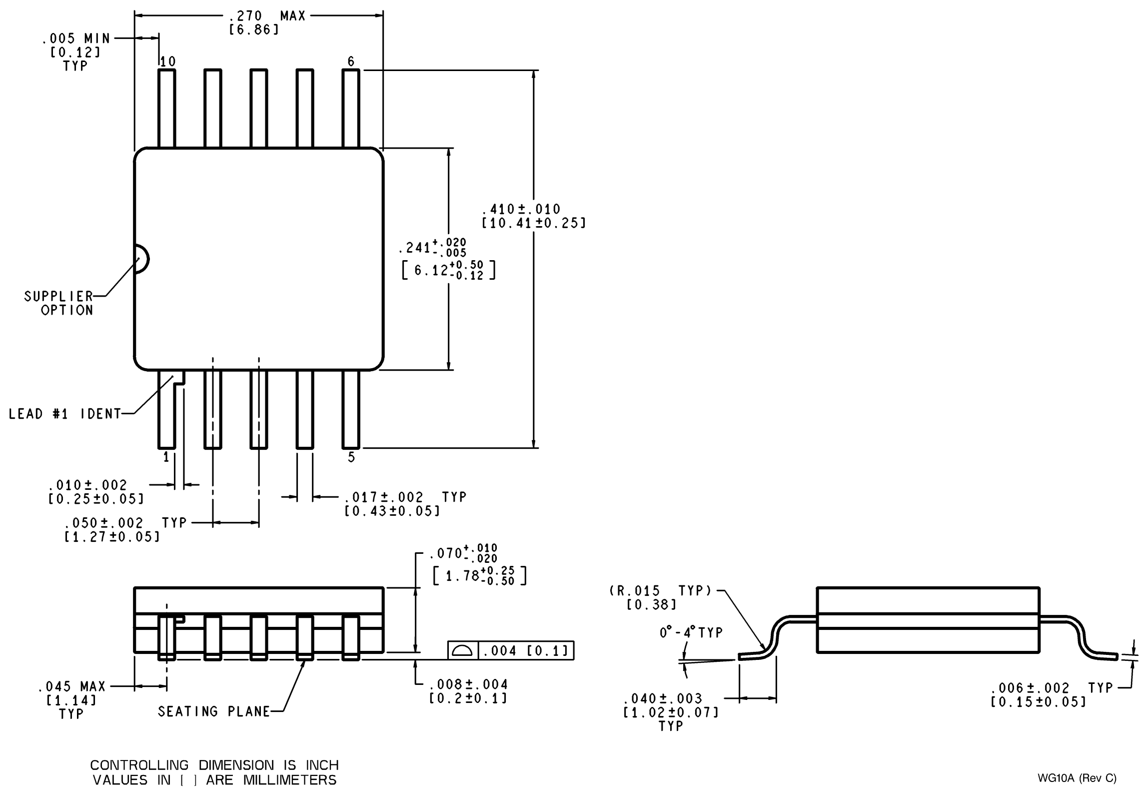


Dual-In-Line Package (J)
NS Package Number J14A



NS Package Number W10A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NS Package Number WG10A

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