National Semiconductor

April 2005

LF147JAN
Wide Bandwidth Quad JFET Input Operational Amplifier

General Description

The LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF147 is pin compatible with the standard LM148. This feature allows designers to immediately upgrade the overall performance of existing LF148 and LM124 designs.

The LF147 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Features

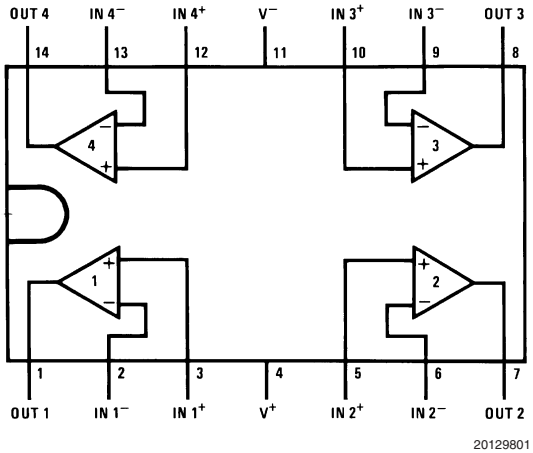
- Internally trimmed offset voltage: 5 mV max
- Low input bias current: 50 pA Typ.
- Low input noise current: 0.01 pA/√Hz Typ.
- Wide gain bandwidth: 4 MHz Typ.
- High slew rate: 13 V/µs Typ.
- Low supply current: 7.2 mA Typ.
- High input impedance: $10^{12}\Omega$ Typ.
- Low total harmonic distortion:
  A_V = 10, R_L = 10KΩ, V_O = $20V_{P-P}$
  BW = 20Hz — 20KHz ≤0.02% Typ.
- Low 1/f noise corner: 50 Hz Typ.
- Fast settling time to 0.01%: 2 µs Typ.

Ordering Information

NS Part Number	JAN Part Number	NS Package Number	Package Description
JL147BCA	JM38510/11906BCA	J14A	14LD CERDIP

Connection Diagram

Dual-In-Line Package



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Top View
See NS Package Number J14A

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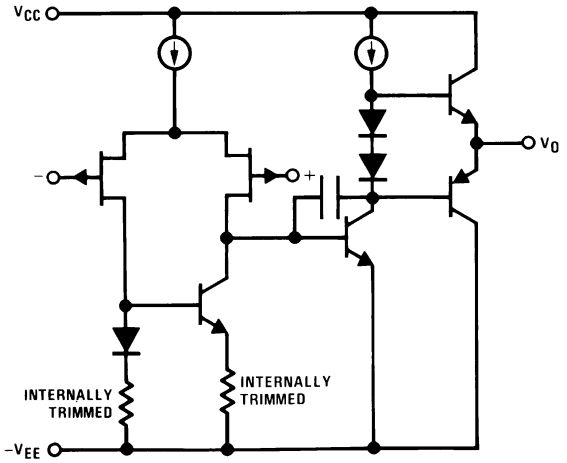
Simplified Schematic

¼ Quad



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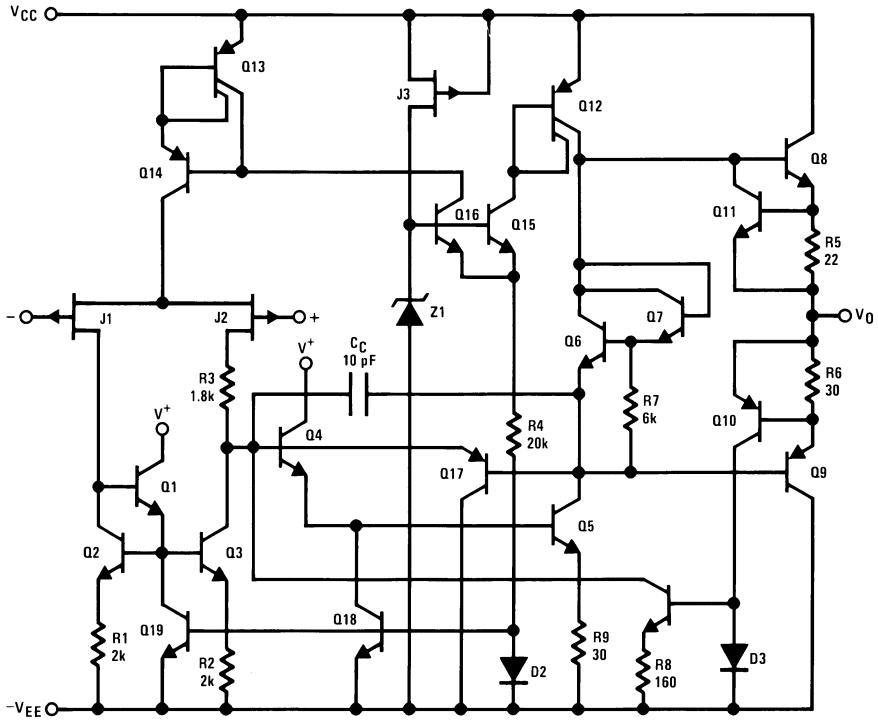
Detailed Schematic



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Absolute Maximum Ratings (Note 1)

Supply Voltage	±18V
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration (Note 3)	Continuous
Power Dissipation (Notes 4, 5)	900 mW
T_J max	150˚C
θ_{JA} CERDIP	70˚C/W
Operating Temperature Range	$-55˚C \leq T_A \leq 125˚C$
Storage Temperature Range	$-65˚C \leq T_A \leq 150˚C$
Lead Temperature (Soldering, 10 sec.)	260˚C
ESD (Note 6)	900V

Recommended Operating Conditions

Supply Voltage Range	±5V to ±15V

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (˚C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55
12	Settling Time at	25

LF147 JAN Electrical Characteristics

DC Parameters

The following conditions apply, unless otherwise specified: V_{CC} = ±15V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	+V_{CC} = 26V, -V_{CC} = -4V, V_{CM} = -11V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		+V_{CC} = 4V, -V_{CC} = -26V, V_{CM} = 11V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		+V_{CC} = 15V, -V_{CC} = -15V, V_{CM} = 0V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		+V_{CC} = 5V, -V_{CC} = -5V, V_{CM} = 0V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
±I_{IB}	Input Bias Current	+V_{CC} = 26V, -V_{CC} = -4V, V_{CM} = -11V		-0.4	0.2	nA	1
				-10	50	nA	2
		+V_{CC} = 15V, -V_{CC} = -15V, V_{CM} = 0V		-0.2	0.2	nA	1
				-10	50	nA	2
		+V_{CC} = 4V, -V_{CC} = -26V, V_{CM} = 11V		-0.2	1.2	nA	1
				-10	70	nA	2
I_{IO}	Input Offset Current	+V_{CC} = 15V, -V_{CC} = -15V, V_{CM} = 0V		-0.1	0.1	nA	1
				-20	20	nA	2
+PSRR	Power Supply Rejection Ratio	-V_{CC} = -15V, +V_{CC} = 20V to 10V		80		dB	1, 2, 3
-PSRR	Power Supply Rejection Ratio	+V_{CC} = 15V, -V_{CC} = -20V to -10V		80		dB	1, 2, 3
CMRR	Input Voltage Common Mode Rejection	±V_{CC} = ±4V to ±26V, V_{CM} = -11V to +11V		80		dB	1, 2, 3
+I_{OS}	Output Short Circuit Current	+V_{CC} = 15V, -V_{CC} = -15V, V_{CM} = -10V, t ≤ 25mS		-80		mA	1, 2, 3
−I_{OS}	Output Short Circuit Current	+V_{CC} = 15V, -V_{CC} = -15V, V_{CM} = 10V, t ≤ 25mS			80	mA	1, 2, 3
I_{CC}	Supply Current	+V_{CC} = 15V, -V_{CC} = -15V			14	mA	1, 2
					16	mA	3
Delta V_{IO} / Delta T	Input Offset Voltage Temp. Sensitivity	25˚C ≤ T_A ≤ +125˚C	(Note 7)	-30	30	µV/˚C	2
		-55˚C ≤ T_A ≤ 25˚C	(Note 7)	-30	30	µV/˚C	3
+V_{OP}	Output Voltage Swing	+V_{CC} = 15V, -V_{CC} = -15V, R_L=10KΩ, V_{CM} = -15V		12		V	4, 5, 6
		+V_{CC} = 15V, -V_{CC} = -15V, R_L=2KΩ, V_{CM} = -15V		10		V	4, 5, 6
-V_{OP}	Output Voltage Swing	+V_{CC} = 15V, -V_{CC} = -15V, R_L=10KΩ, V_{CM} = 15V			-12	V	4, 5, 6
		+V_{CC} = 15V, -V_{CC} = -15V, R_L = 2KΩ, V_{CM} = 15V			-10	V	4, 5, 6
+A_{VS}	Open Loop Voltage Gain	+V_{CC} = 15V, -V_{CC} = -15V, R_L = 2KΩ, V_O = 0 to 10V		50		V/mV	4
				25		V/mV	5, 6
−A_{VS}	Open Loop Voltage Gain	+V_{CC} = 15V, -V_{CC} = -15V, R_L = 2KΩ, V_O = 0 to -10V		50		V/mV	4
				25		V/mV	5, 6
A_{VS}	Open Loop Voltage Gain	+V_{CC} = 5V, -V_{CC} = -5V, R_L = 10KΩ, V_O = ±2V		20		V/mV	4, 5, 6

LF147 JAN Electrical Characteristics (Continued)

AC Parameters

The following conditions apply, unless otherwise specified: V_{CC} = ±15V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
+SR	Slew Rate	V_I = -5V to +5V		7		V/µS	7
				5		V/µS	8A, 8B
-SR	Slew Rate	V_I = +5V to -5V		7		V/µS	7
				5		V/µS	8A, 8B
TR_{TR}	Transient Response Rise Time	AV=1, V_I=50mV, C_L= 100pF, R_L=2KΩ			200	nS	7, 8A, 8B
TR_{OS}	Transient Response Overshoot	AV=1, V_I=50mV, C_L= 100pF, R_L=2KΩ			40	%	7, 8A, 8B
NI_{BB}	Noise Broadband	BW = 10Hz to 15KHz, R_S = 0Ω			15	μV_{RMS}	7
NI_{PC}	Noise Popcorn	BW = 10Hz to 15KHz, R_S = 100KΩ			80	μV_{PK}	7
C_S	Channel Separation	R_L = 2KΩ		80		dB	7
		R_L = 2KΩ, V_I = ±10V, A to B		80		dB	7
		R_L = 2KΩ, V_I = ±10V, A to C		80		dB	7
		R_L = 2KΩ, V_I = ±10V, A to D		80		dB	7
		R_L = 2KΩ, V_I = ±10V, B to A		80		dB	7
		R_L = 2KΩ, V_I = ±10V, B to C		80		dB	7
		R_L = 2KΩ, V_I = ±10V, B to D		80		dB	7
		R_L = 2KΩ, V_I = ±10V, C to A		80		dB	7
		R_L = 2KΩ, V_I = ±10V, C to B		80		dB	7
		R_L = 2KΩ, V_I = ±10V, C to D		80		dB	7
		R_L = 2KΩ, V_I = ±10V, D to A		80		dB	7
		R_L = 2KΩ, V_I = ±10V, D to B		80		dB	7
		R_L = 2KΩ, V_I = ±10V, D to C		80		dB	7
$\pm t_S$	Settling Time	A_V = 1			1,500	nS	12

Drift Values

The following conditions apply, unless otherwise specified: DC ±V_{CC} = ±15V, V_{CM} = 0V, "Delta calculations performed on JAN S and QMLV devices at group B, subgroup 5 only"

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	+V_{CC} = 15V, -V_{CC} = -15V, V_{CM} = 0V		-1.0	1.0	mV	1
$+I_{IB}$	Input Bias Current	+V_{CC} = 15V, -V_{CC} = -15V, V_{CM} = 0V		-0.1	0.1	nA	1
$-I_{IB}$	Input Bias Current	+V_{CC} = 15V, -V_{CC} = -15V, V_{CM} = 0V		-0.1	0.1	nA	1

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (Package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A) / \theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

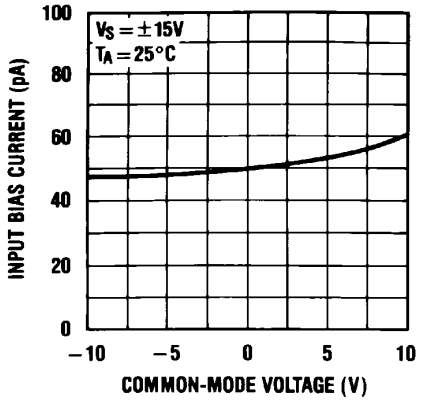
Note 5: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Note 6: Human body model, 1.5 kΩ in series with 100 pF.

Note 7: Calculated parameters.

Typical Performance Characteristics

Input Bias Current



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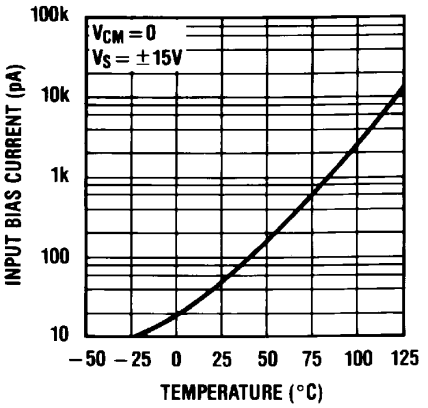
Input Bias Current



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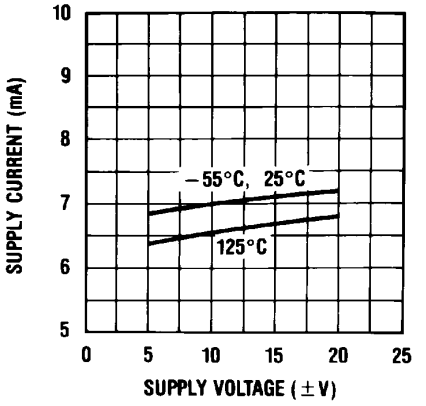
Supply Current



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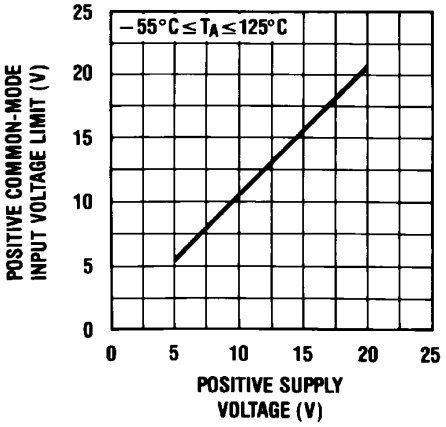
Positive Common-Mode Input Voltage Limit



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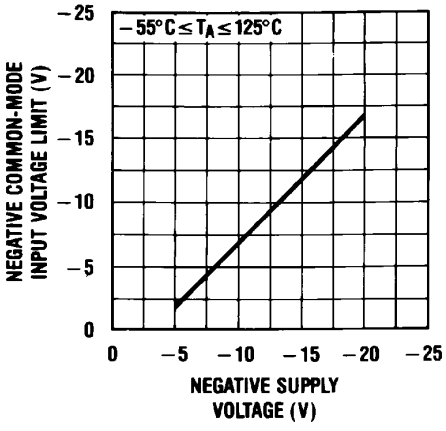
Negative Common-Mode Input Voltage Limit



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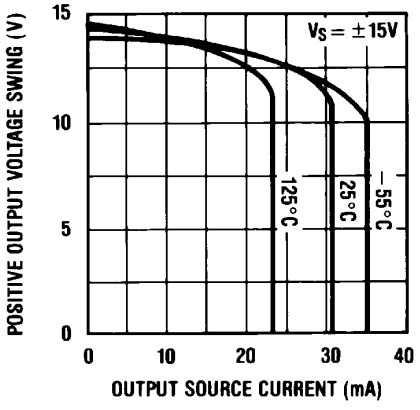
Positive Current Limit



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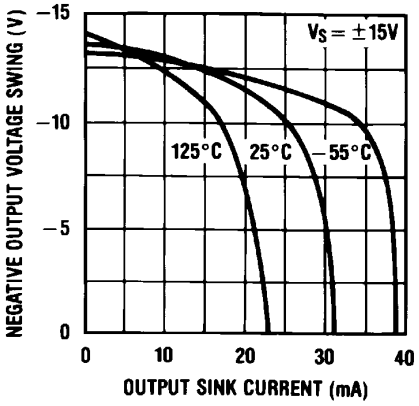
Typical Performance Characteristics (Continued)

Negative Current Limit



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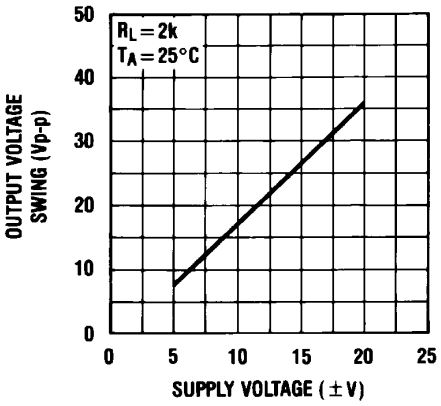
Output Voltage Swing



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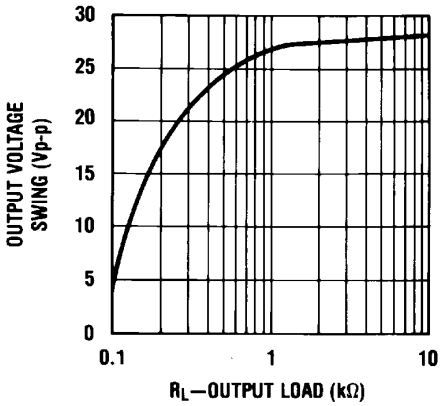
Output Voltage Swing



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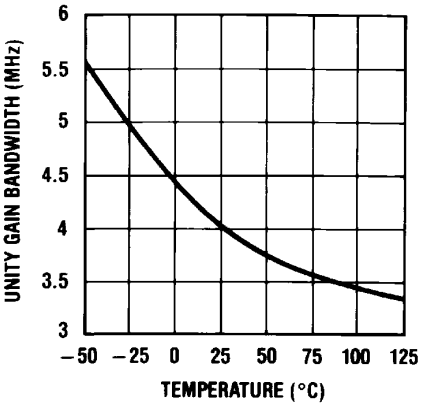
Gain Bandwidth



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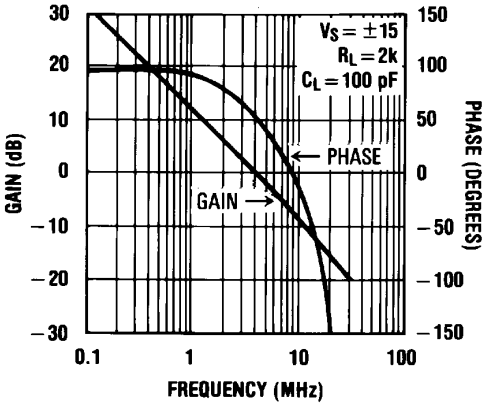
Bode Plot



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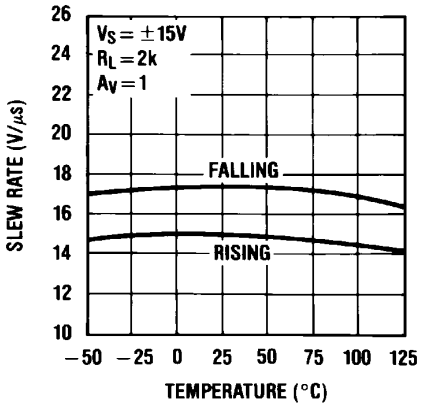
Slew Rate



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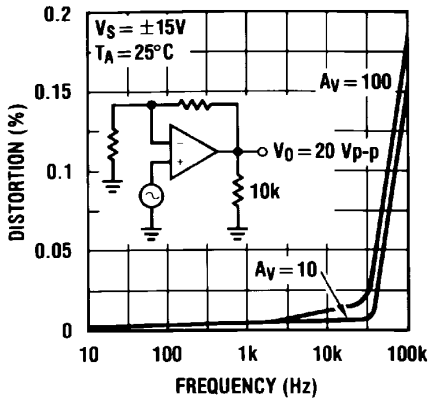
Typical Performance Characteristics (Continued)

Distortion vs Frequency



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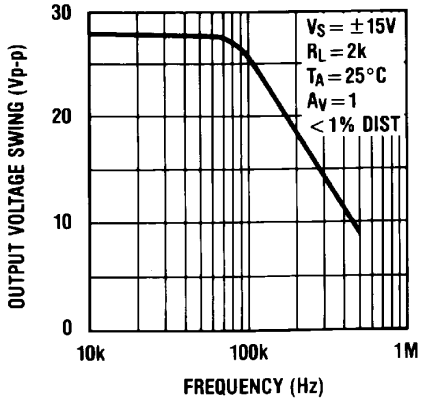
Undistorted Output Voltage Swing



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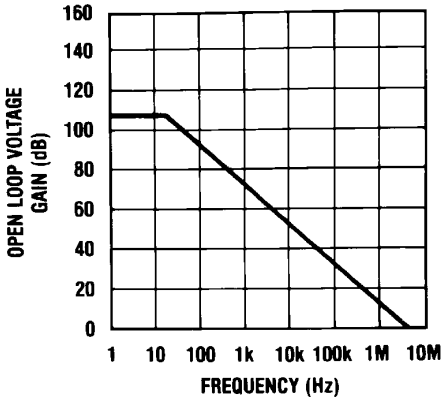
Open Loop Frequency Response



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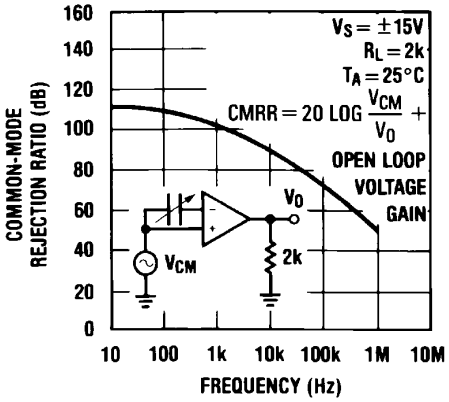
Common-Mode Rejection Ratio



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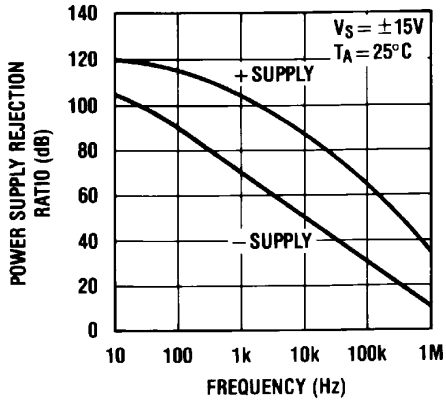
Power Supply Rejection Ratio



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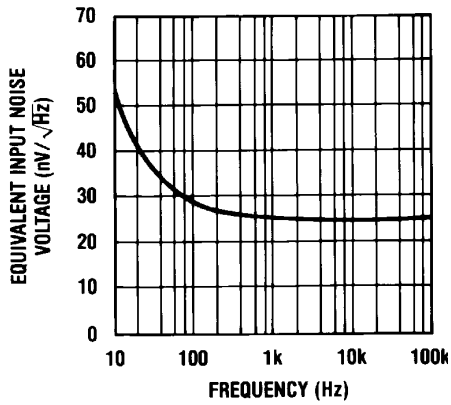
Equivalent Input Noise Voltage



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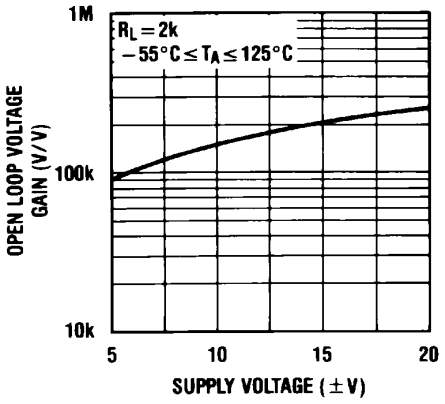
Typical Performance Characteristics (Continued)

Open Loop Voltage Gain



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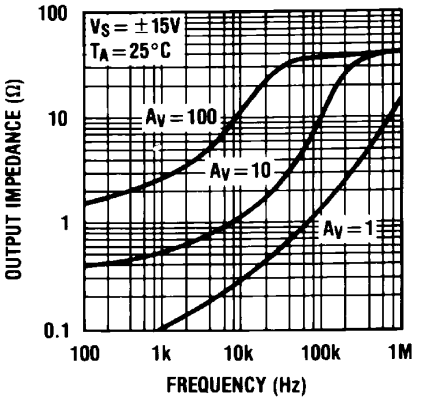
Output Impedance



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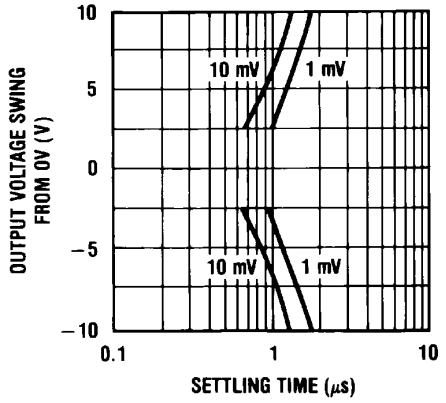
Inverter Settling Time



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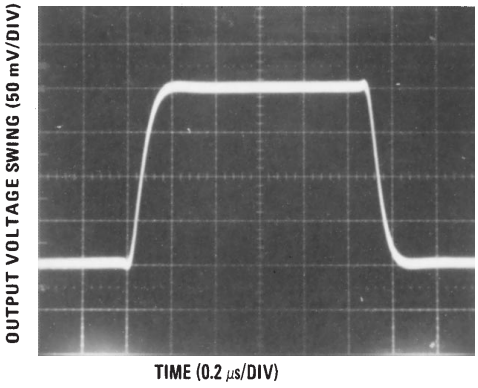
Pulse Response R_L=2 kΩ, C_L=10 pF

Small Signal Inverting



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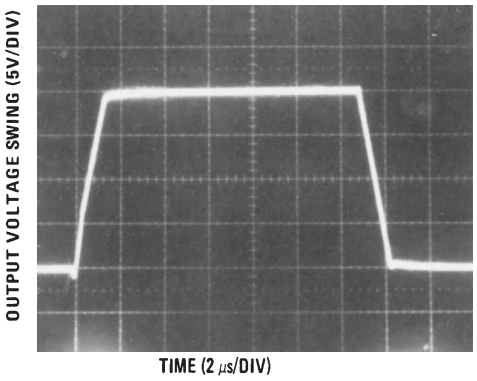
Large Signal Inverting



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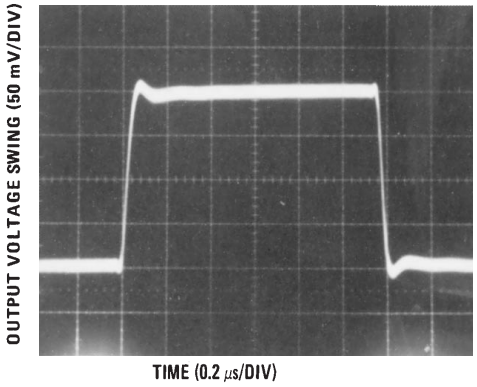
Small Signal Non-Inverting



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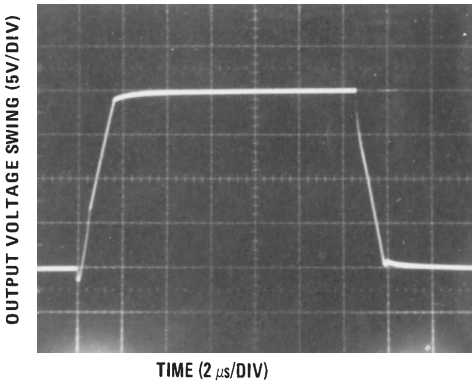
Large Signal Non-Inverting



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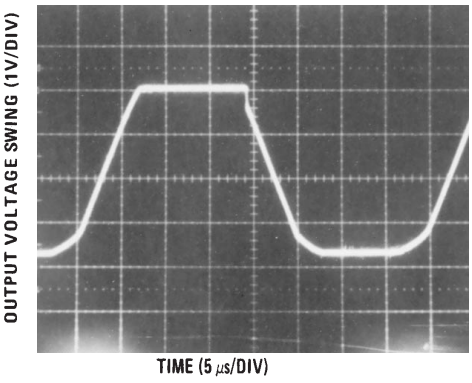
Current Limit (R_L=100Ω)



20129808

Application Hints

The LF147 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF147 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

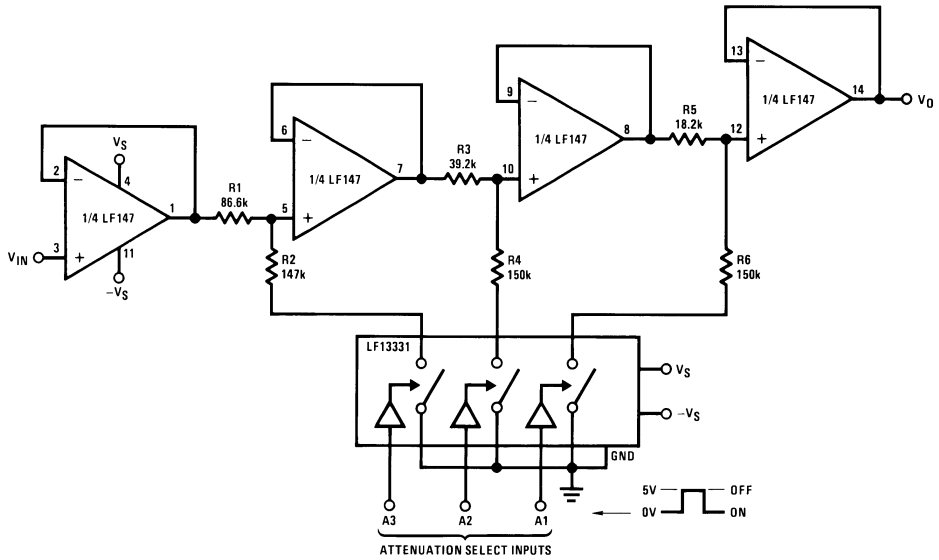
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Applications

Digitally Selectable Precision Attenuator



20129810

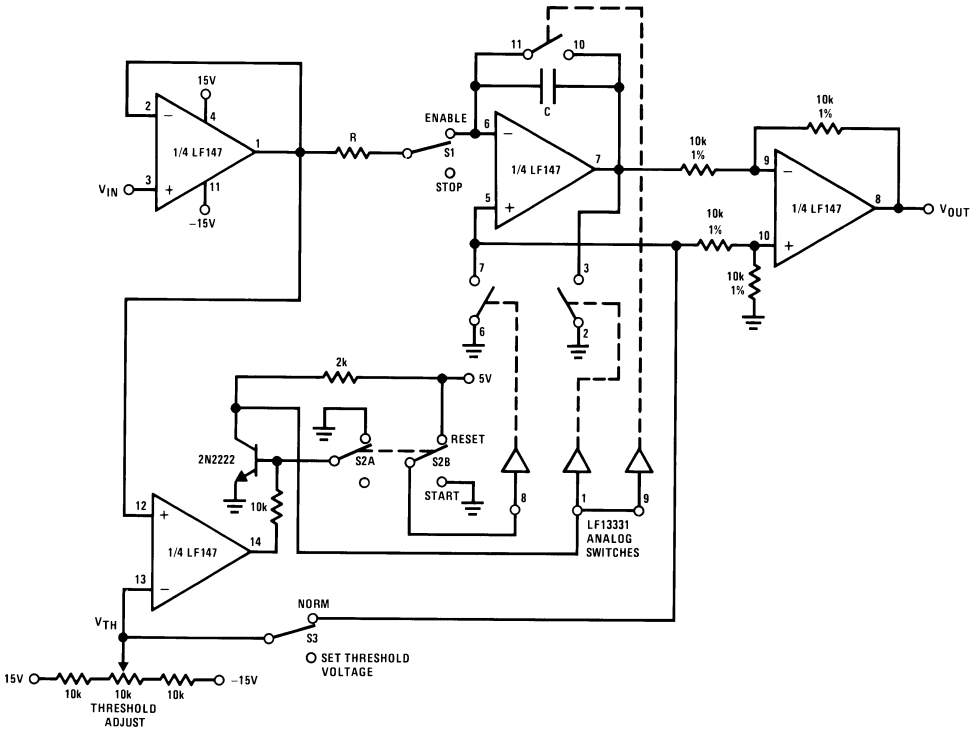
All resistors 1% tolerance

- Accuracy of better than 0.4% with standard 1% value resistors
  No offset adjustment necessary
- Expandable to any number of stages
- Very high input impedance

A1	A2	A3	V_O Attenuation
0	0	0	0
0	0	1	−1 dB
0	1	0	−2 dB
0	1	1	−3 dB
1	0	0	−4 dB
1	0	1	−5 dB
1	1	0	−6 dB
1	1	1	−7 dB

Typical Applications (Continued)

Long Time Integrator with Reset, Hold and Starting Threshold Adjustment



20129811

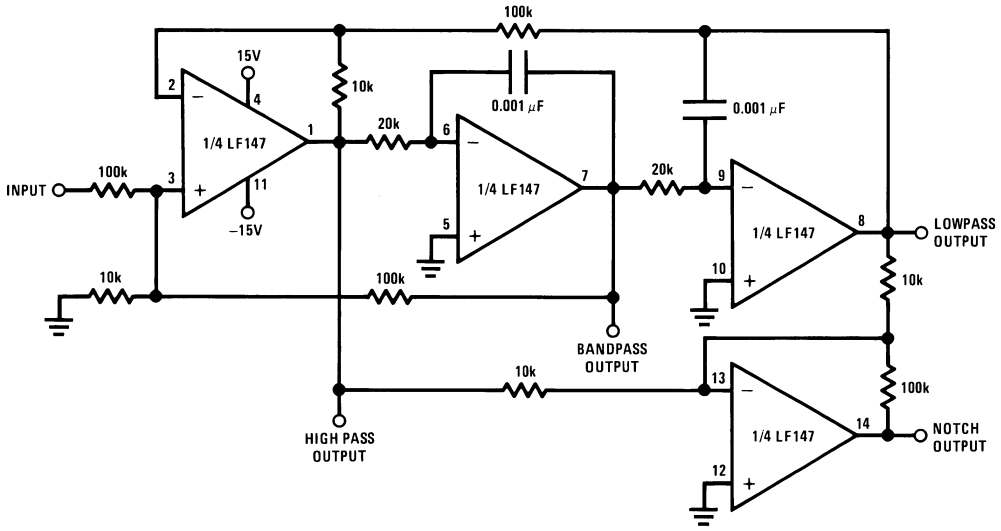
- V_O starts from zero and is equal to the integral of the input voltage with respect to the threshold voltage:

$$V_{OUT} = \frac{1}{RC}\int_0^t (V_{IN} - V_{TH})dt$$

- Output starts when $V_{IN} \geq V_{TH}$
- Switch S1 permits stopping and holding any output value
- Switch S2 resets system to zero

Typical Applications (Continued)

Universal State Variable Filter



20129812

For circuit shown:

f_O=3 kHz, f_{NOTCH}=9.5 kHz

Q=3.4

Passband gain:

Highpass — 0.1

Bandpass — 1

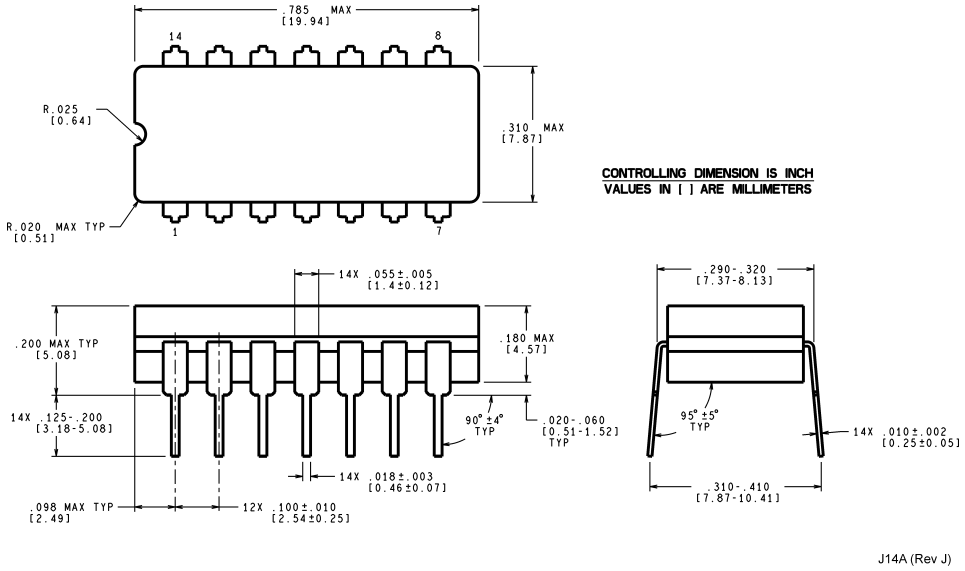
Lowpass — 1

Notch — 10

- f_0xQ≤200 kHz
- 10V peak sinusoidal output swing without slew limiting to 200 kHz
- See LM148 data sheet for design equations

Date Released	Revision	Section	Originator	Changes
04/18/05	A	New Release into corporate format	L. Lytle	1 MDS datasheets converted into one Corp. datasheet format. MJLF147–X rev 1B1 MDS will be archived

Physical Dimensions inches (millimeters) unless otherwise noted



J14A (Rev J)

Ceramic Dual-In-Line Package (J)
NS Package Number J14A

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Email: new.feedback@nsc.com
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National Semiconductor
Europe Customer Support Center
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
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National Semiconductor
Asia Pacific Customer
Support Center
Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560